CMOS Rail-to-Rail Input and Output Operational Amplifier

Check for Samples: SM73306

FEATURES

(Typical Unless Otherwise Noted)

- **Renewable Energy Grade**
- **Rail-to-Rail Input Common-Mode Voltage Range, Guaranteed Over Temperature**
- **Rail-to-Rail Output Swing Within 20 mV of Supply Rail, 100 kΩ Load**
- **Operates from 5V to 15V Supply**
- **Excellent CMRR and PSRR 8 dB**
- **Ultra Low Input Current 150 fA**
- **High Voltage Gain (R_L = 100 kΩ) 120 dB**
- **Low Supply Current (@ V_S = 5V) 500 µA/Amplifier**
- **Low Offset Voltage Drift 1.0 µV/°C**

APPLICATIONS

- **Automotive Transducer Amplifier**
- **Pressure Sensor**
- **Oxygen Sensor**
- **Temperature Sensor**
- **Speed Sensor**

DESCRIPTION

The SM73306 amplifier was specifically developed for single supply applications that operate from −40°C to +125°C. This wide temperature range makes it well-suited for photovoltaic systems. A unique design topology enables the SM73306 common-mode voltage range to accommodate input signals beyond the rails. This eliminates non-linear output errors due to input signals exceeding a traditionally limited common-mode voltage range. The SM73306 signal range has a high CMRR of 82 dB for excellent accuracy in non-inverting circuit configurations.

The SM73306 rail-to-rail input is complemented by rail-to-rail output swing. This assures maximum dynamic signal range which is particularly important in 5V systems.

Ultra-low input current of 150 fA and 120 dB open loop gain provide high accuracy and direct interfacing with high impedance sources.

Connection Diagram

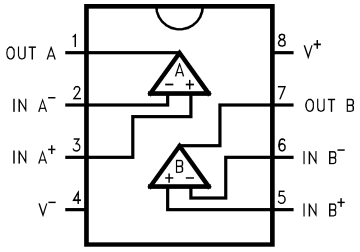


Figure 1. 8-Pin SOIC
Package Number D0008A
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	2000V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin	±5 mA
Current at Output Pin (4)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (5)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Human body model, 1.5 kΩ in series with 100 pF.
(4) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Operating Conditions (1)

Supply Voltage	$2.5V \le V^+ \le 15.5V$
Junction Temperature Range	$-40°C \le T_J \le +125°C$
Thermal Resistance (θ_{JA})	171°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{OS}	Input Offset Voltage		0.11	6.0 **6.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0		µV/°C
I_B	Input Bias Current	(3)	0.15	**200**	pA max
I_{OS}	Input Offset Current	(3)	0.075	**100**	pA max
R_{IN}	Input Resistance		>10		Tera Ω
C_{IN}	Common-Mode Input Capacitance		3		pF
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 15V$ $V^+ = 15V$	82	63 **58**	dB min
		$0V \le V_{CM} \le 5V$	82	63 **58**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	82	63 **58**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$	82	63 **58**	dB min

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) Guaranteed limits are dictated by tester limits and not device performance. Actual performance is reflected in the typical value.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V For CMRR ≥ 50 dB	V^- −0.3	−0.25 **0**	V max
			V^+ + 0.3	V^+ + 0.25 **V^+**	V min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ: Sourcing (4) Sinking	300 40		V/mV min
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to V^+/2	4.9	4.8 **4.7**	V min
			0.1	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to V^+/2	4.7	4.5 **4.24**	V min
			0.3	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to V^+/2	14.7	14.4 **14.0**	V min
			0.16	0.35 **0.5**	V max
		V^+ = 15V R_L = 600Ω to V^+/2	14.1	13.4 **13.0**	V min
			0.5	1.0 **1.5**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	25	16 **10**	mA min
		Sinking, V_O = 5V	22	11 **8**	
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **20**	
		Sinking, V_O = 5V (5)	30	30 **22**	
I_S	Supply Current	V^+ = +5V, V_O = V^+/2	1.0	1.75 **2.1**	mA max
		V^+ = +15V, V_O = V^+/2	1.3	1.95 **2.3**	mA max

(4) V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.
(5) Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (1)	Limit (2)	Units
SR	Slew Rate	(3)	1.3	0.7 **0.5**	Vμs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5		MHz
φ_m	Phase Margin		50		Deg
G_m	Gain Margin		15		dB
	Amp-to-Amp Isolation	(4)	150		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	37		nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.06		pA$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −2 R_L = 10 kΩ, V_O = −4.1 V_{PP}	0.01		%
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01		

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
(4) Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Typical Performance Characteristics

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Supply Current vs Supply Voltage

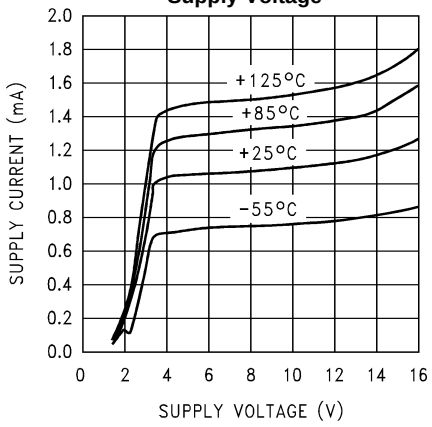


Figure 2.

Input Current vs Temperature

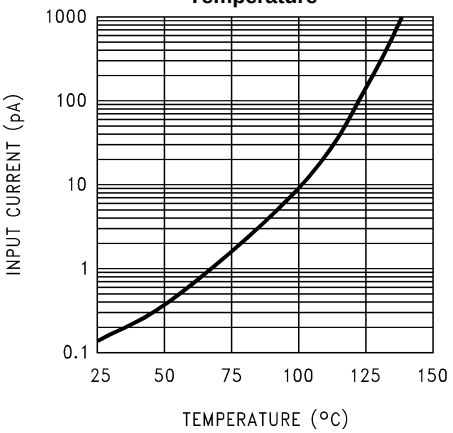


Figure 3.

Sourcing Current vs Output Voltage

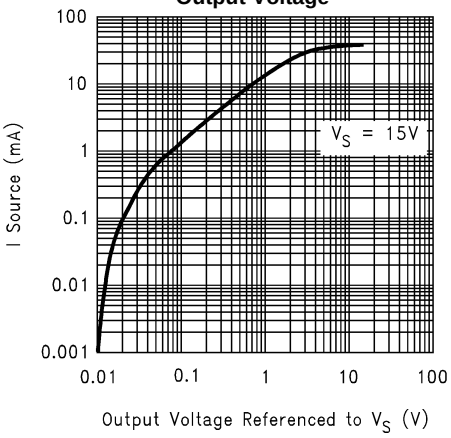


Figure 4.

Sourcing Current vs Output Voltage

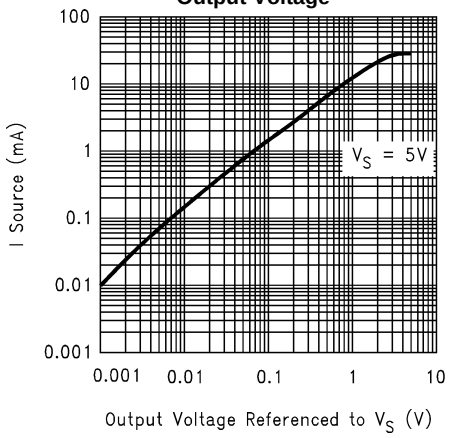


Figure 5.

Sourcing Current vs Output Voltage

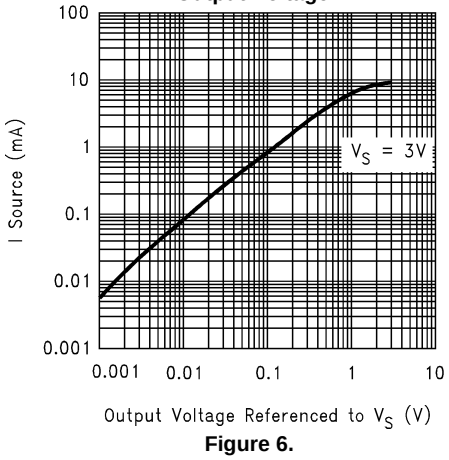


Figure 6.

Sinking Current vs Output Voltage

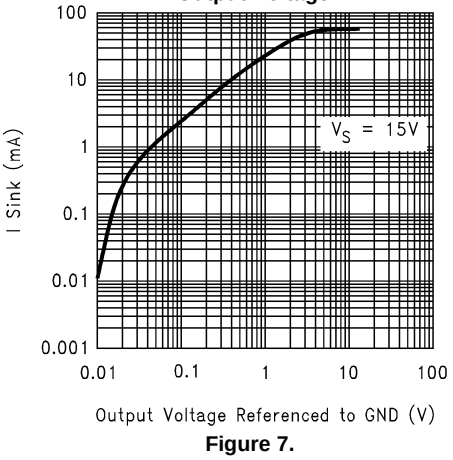


Figure 7.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Sinking Current vs Output Voltage

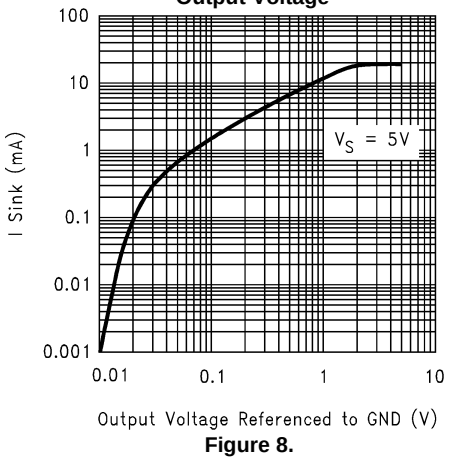


Figure 8.

Sinking Current vs Output Voltage

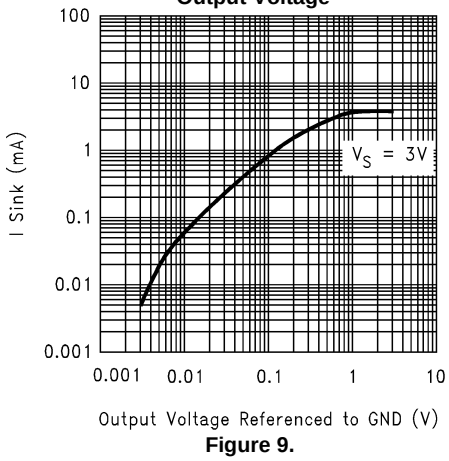


Figure 9.

Output Voltage Swing vs Supply Voltage

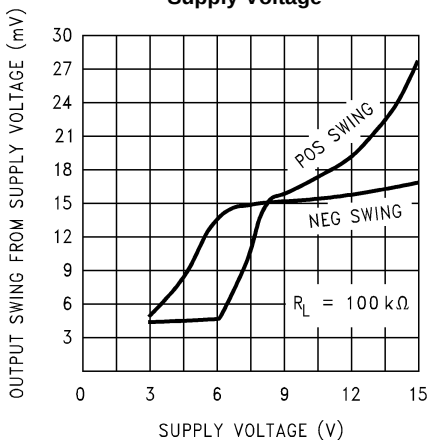


Figure 10.

Input Voltage Noise vs Frequency

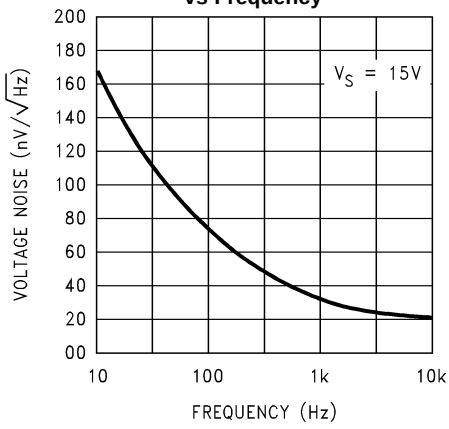


Figure 11.

Input Voltage Noise vs Input Voltage

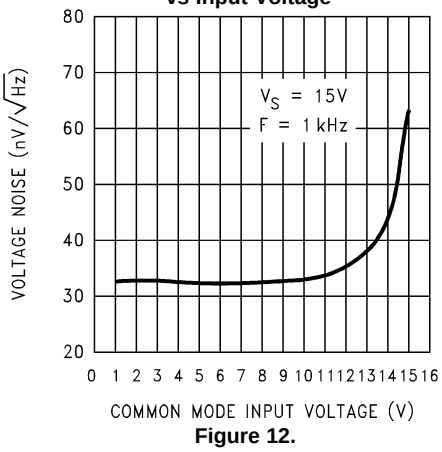


Figure 12.

Input Voltage Noise vs Input Voltage

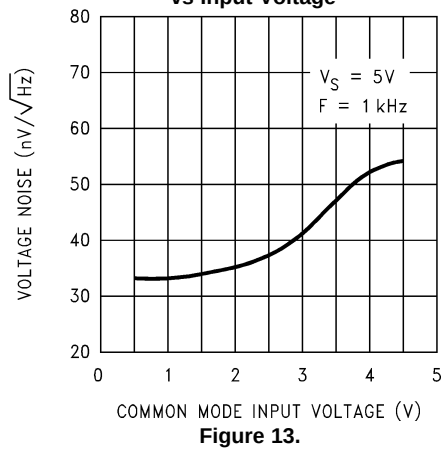


Figure 13.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage Noise vs Input Voltage

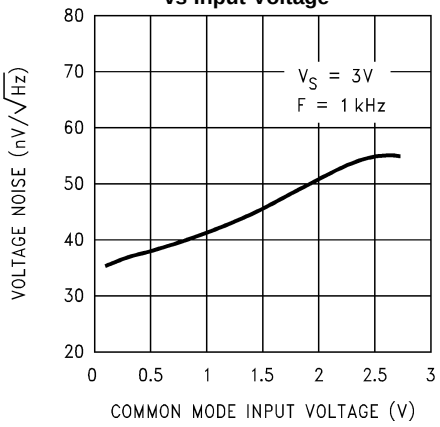


Figure 14.

Crosstalk Rejection vs Frequency

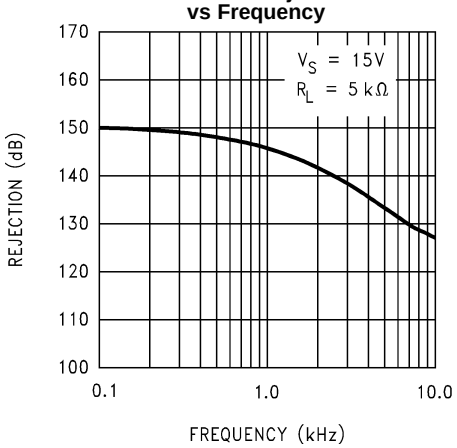


Figure 15.

Crosstalk Rejection vs Frequency

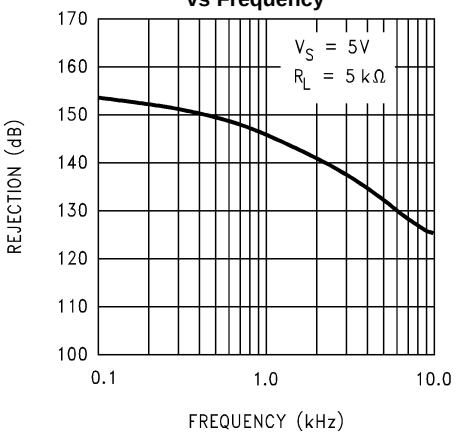


Figure 16.

Positive PSRR vs Frequency

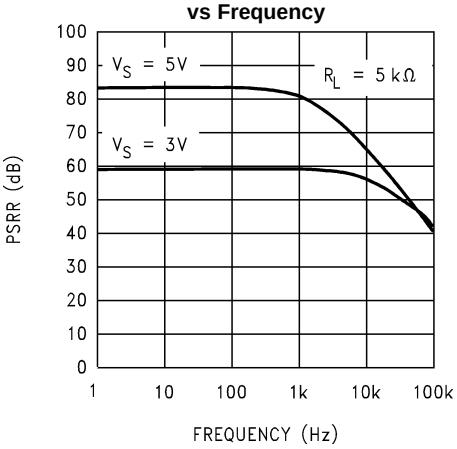


Figure 17.

Negative PSRR vs Frequency

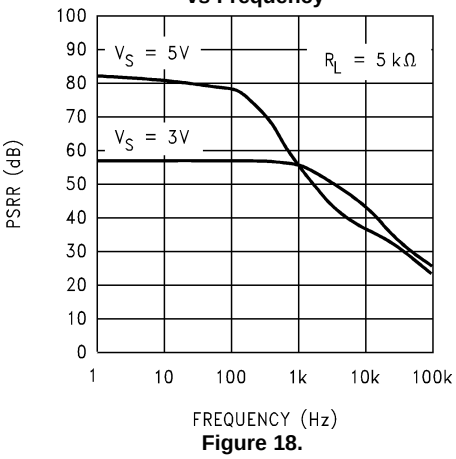


Figure 18.

CMRR vs Frequency

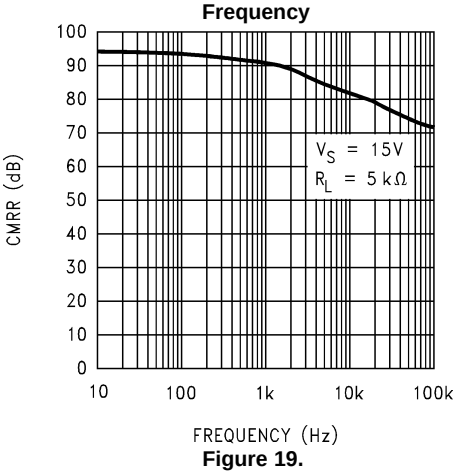


Figure 19.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

CMRR vs Input Voltage

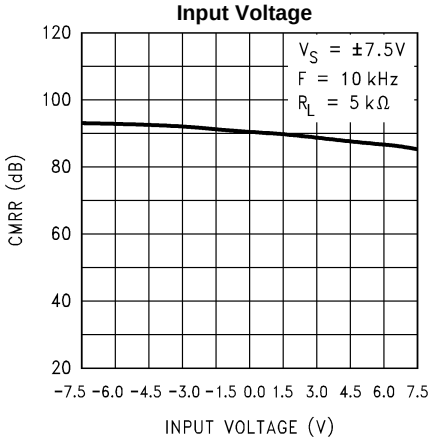


Figure 20.

CMRR vs Input Voltage

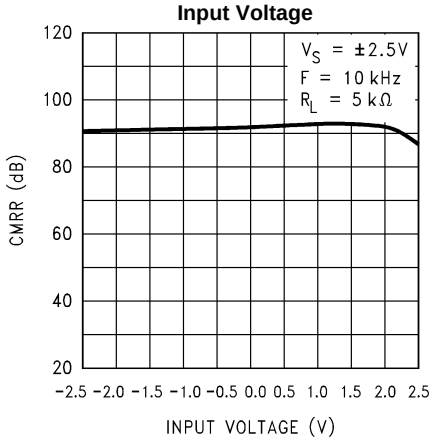


Figure 21.

CMRR vs Input Voltage

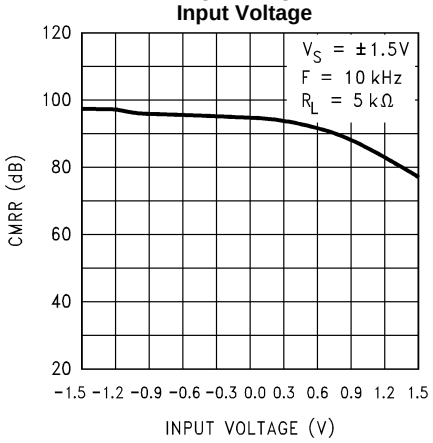


Figure 22.

ΔV_{OS} vs CMR

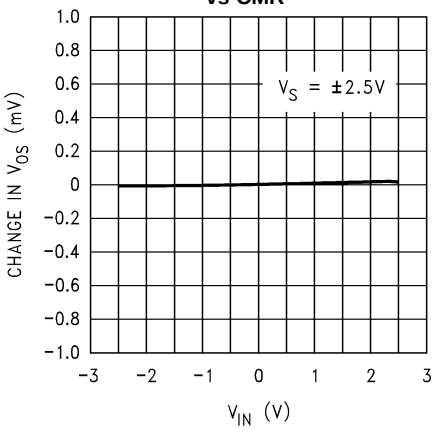


Figure 23.

ΔV_{OS} vs CMR

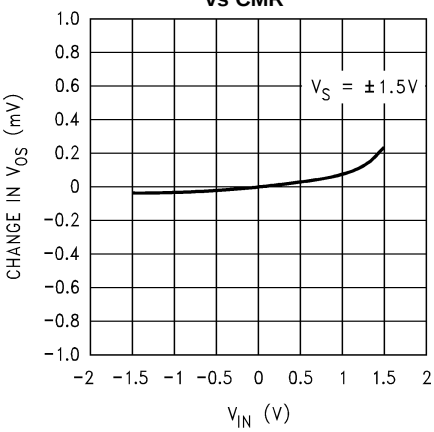


Figure 24.

Input Voltage vs Output Voltage

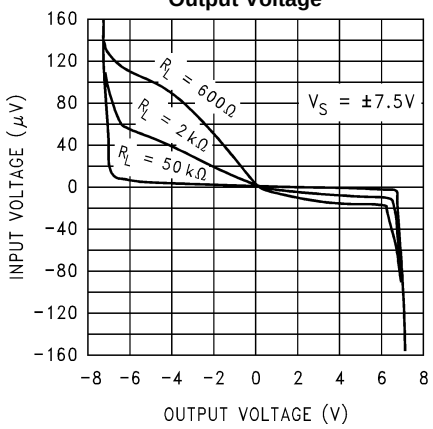


Figure 25.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Input Voltage vs Output Voltage

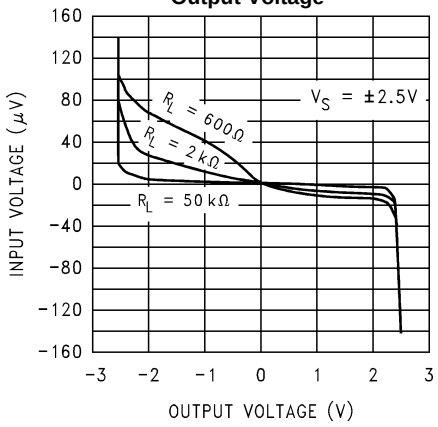


Figure 26.

Open Loop Frequency Response

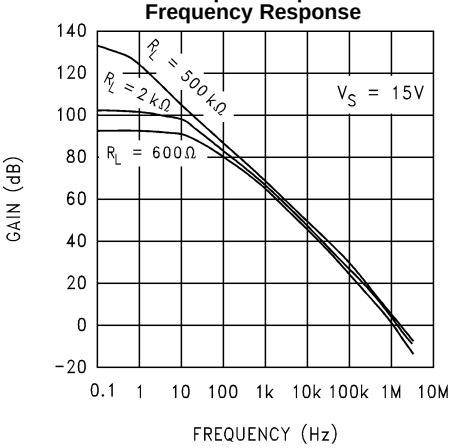


Figure 27.

Open Loop Frequency Response

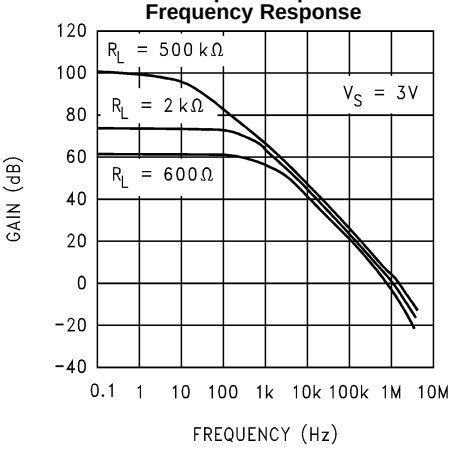


Figure 28.

Open Loop Frequency Response vs Temperature

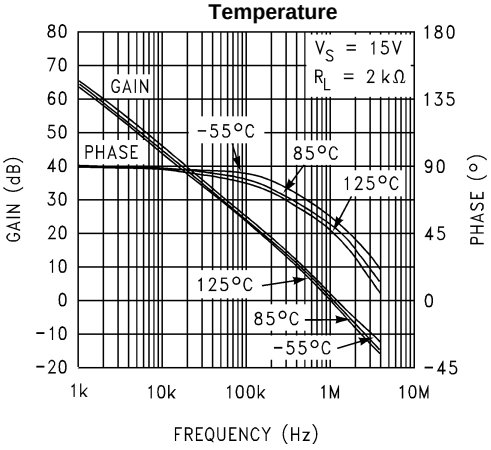


Figure 29.

Maximum Output Swing vs Frequency

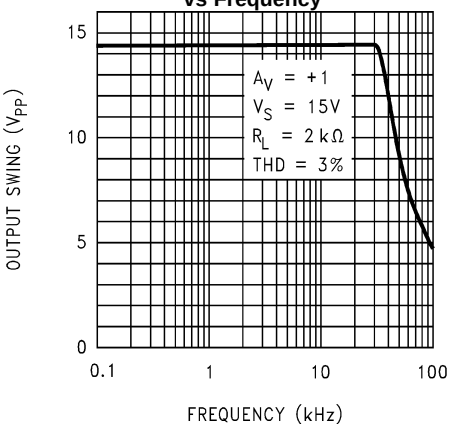


Figure 30.

Gain and Phase vs Capacitive Load

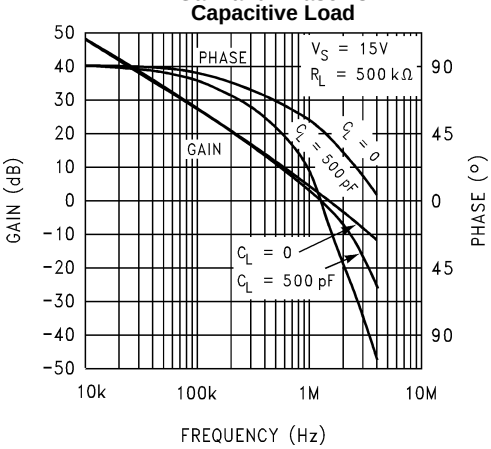


Figure 31.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Gain and Phase vs Capacitive Load

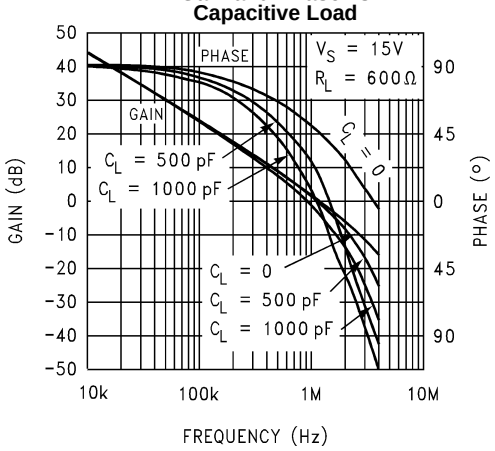


Figure 32.

Open Loop Output Impedance vs Frequency

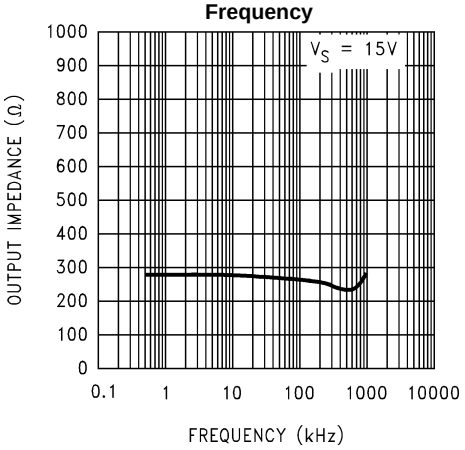


Figure 33.

Open Loop Output Impedance vs Frequency

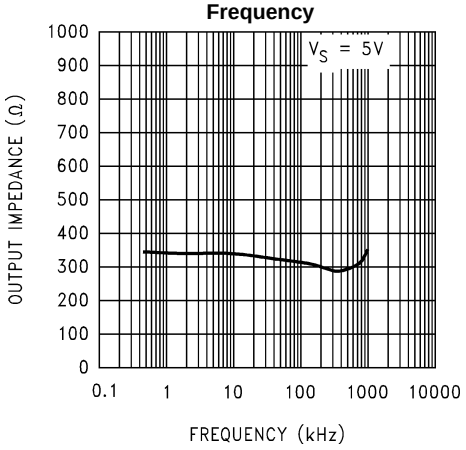


Figure 34.

Slew Rate vs Supply Voltage

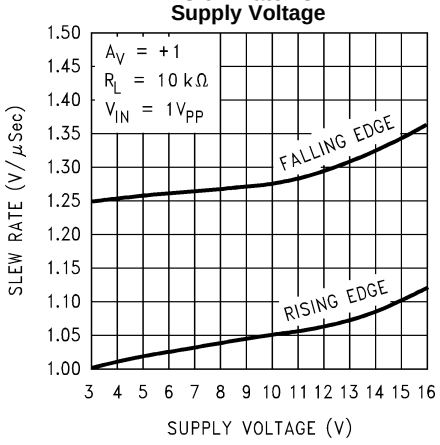


Figure 35.

Non-Inverting Large Signal Pulse Response

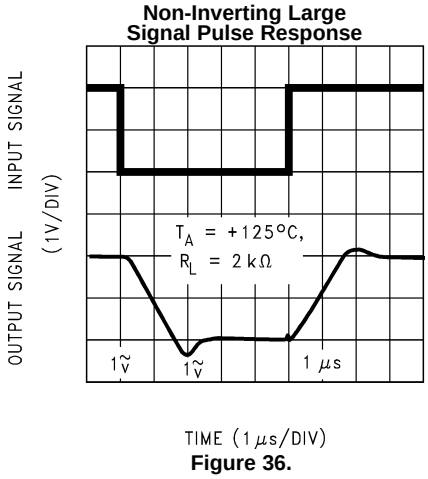


Figure 36.

Non-Inverting Large Signal Pulse Response

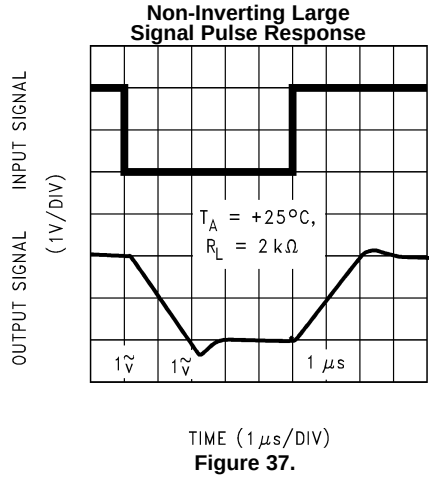


Figure 37.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Non-Inverting Large Signal Pulse Response

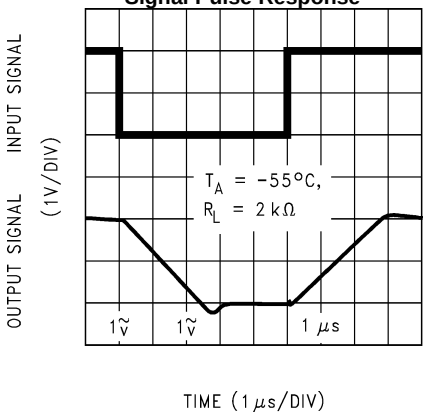


Figure 38.

Non-Inverting Small Signal Pulse Response

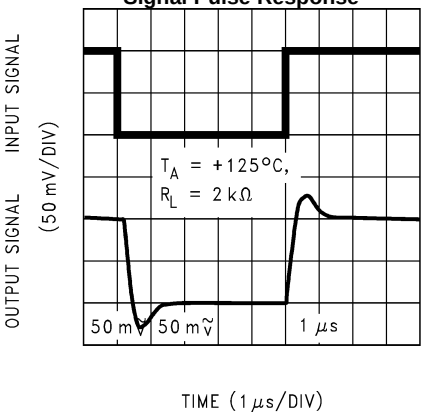


Figure 39.

Non-Inverting Small Signal Pulse Response

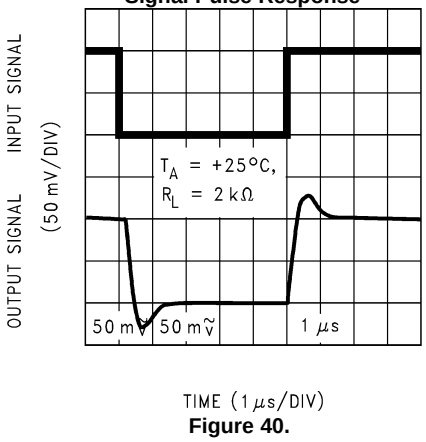


Figure 40.

Non-Inverting Small Signal Pulse Response

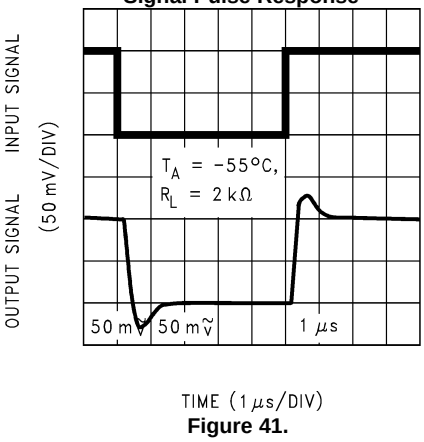


Figure 41.

Inverting Large Signal Pulse Response

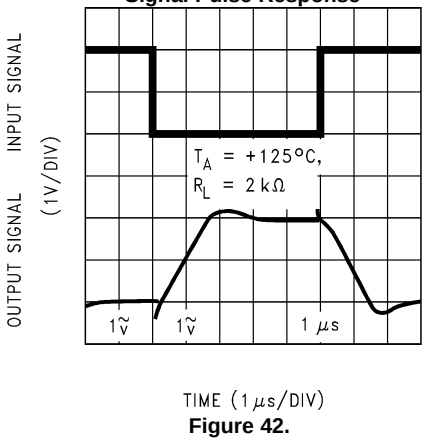


Figure 42.

Inverting Large Signal Pulse Response

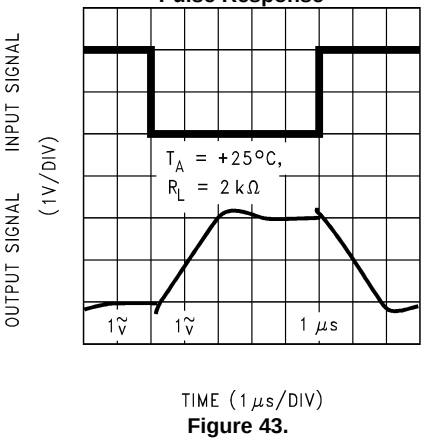


Figure 43.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

Inverting Large Signal Pulse Response

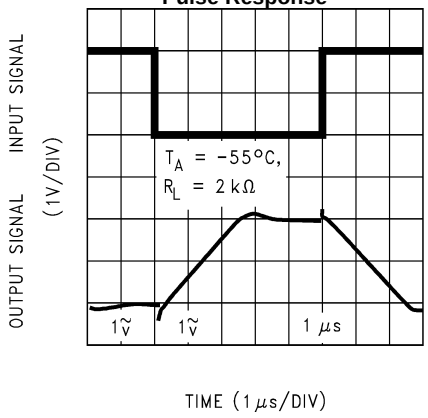


Figure 44.

Inverting Small Signal Pulse Response

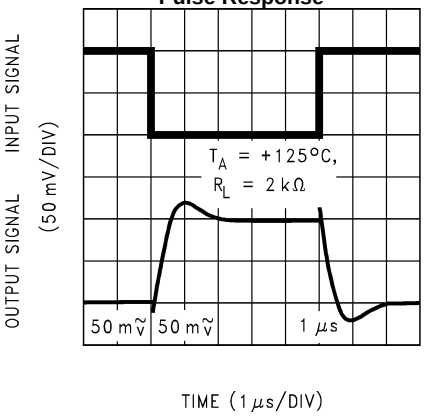


Figure 45.

Inverting Small Signal Pulse Response

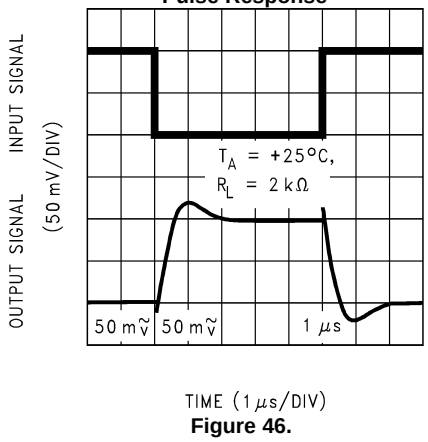


Figure 46.

Inverting Small Signal Pulse Response

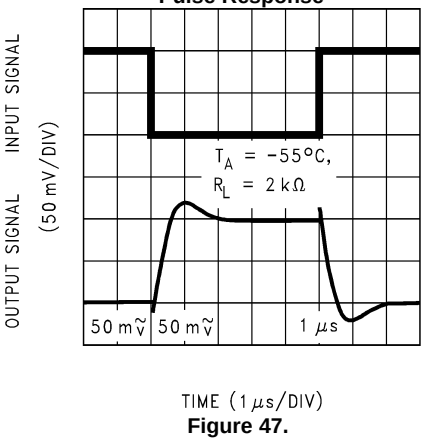


Figure 47.

Stability vs Capacitive Load

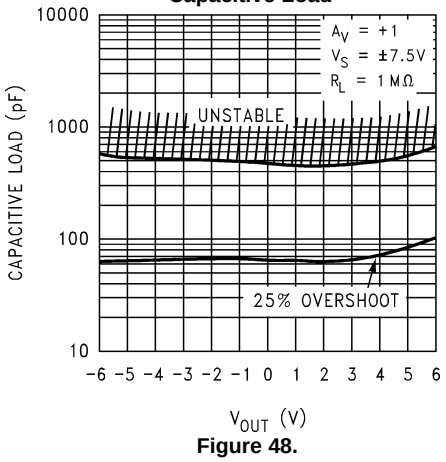


Figure 48.

Stability vs Capacitive Load

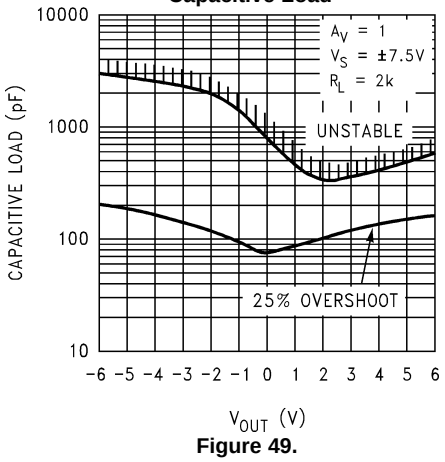


Figure 49.

Typical Performance Characteristics (continued)

V_S = +15V, Single Supply, T_A = 25°C unless otherwise specified

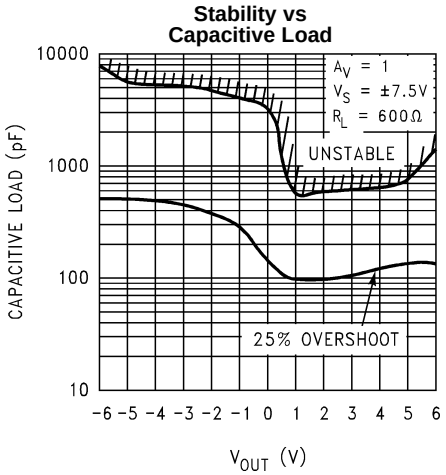


Figure 50.

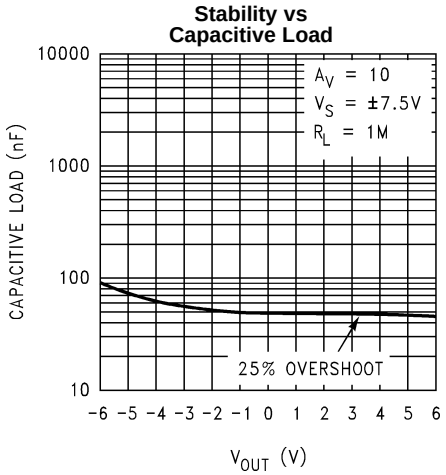


Figure 51.

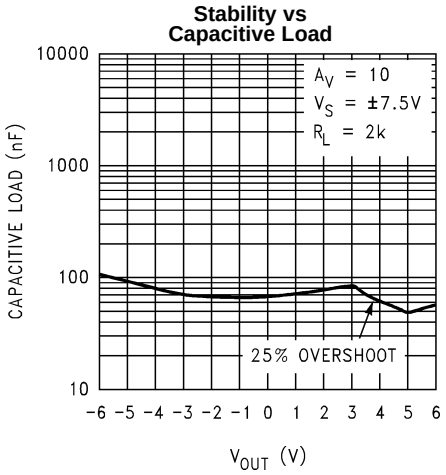


Figure 52.

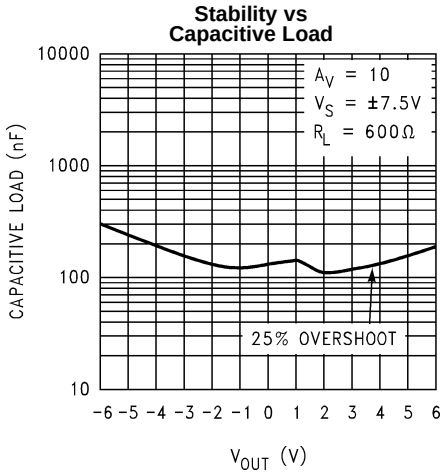


Figure 53.

APPLICATION HINTS

INPUT COMMON-MODE VOLTAGE RANGE

Unlike Bi-FET amplifier designs, the SM73306 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 54 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

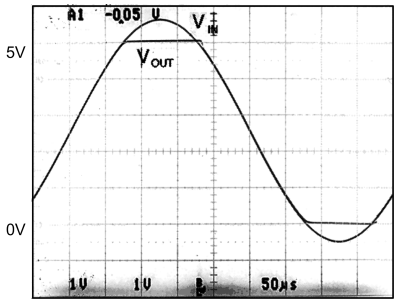


Figure 54. An Input Voltage Signal Exceeds the SM73306 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 55, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

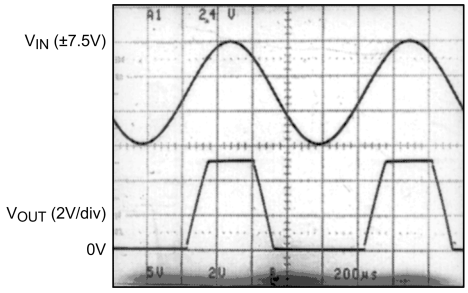


Figure 55. A ±7.5V Input Signal Greatly Exceeds the 5V Supply in Figure 56 Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in Figure 56.

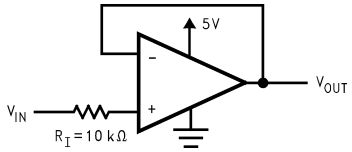


Figure 56. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

RAIL-TO-RAIL OUTPUT

The approximate output resistance of the SM73306 is 110Ω sourcing and 80Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be esitmated as a function of load.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the SM73306.

Although the SM73306 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the SM73306 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK).

The effect of input capacitance can be compensated for by adding a capacitor, C_f, around the feedback resistors (as in Figure 54) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1\, C_{IN} \leq R_2\, C_f \quad (2)$$

Since it is often difficult to know the exact value of C_{IN}, C_f can be experimentally adjusted so that the desired pulse response is achieved.

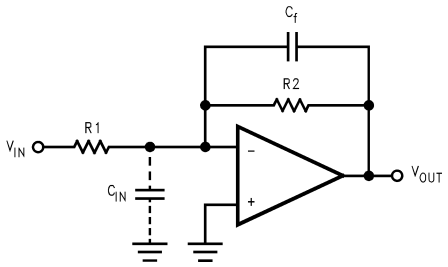


Figure 57. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Performance Characteristics).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 58.

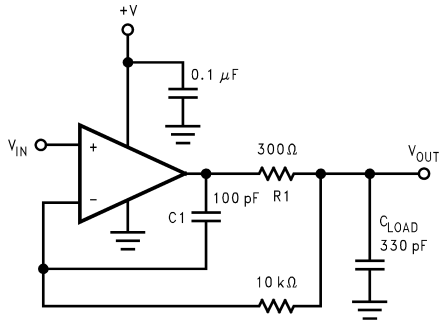


Figure 58. SM73306 Noninverting Amplifier, Compensated to Handle Capacitive Loads

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the SM73306, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the SM73306's inputs and the terminals of components connected to the op-amp's inputs, as in Figure 59. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 33 times degradation from the SM73306's actual performance. If a guard ring is used and held within 5 mV of the inputs, then the same resistance of $10^{12}\Omega$ will only cause 0.05 pA of leakage current. See Figure 60 for typical connections of guard rings for standard op-amp configurations.

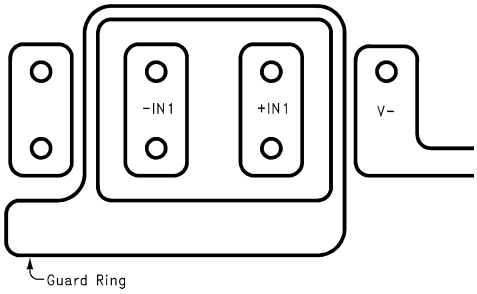


Figure 59. Examples of Guard Ring in PC Board Layout

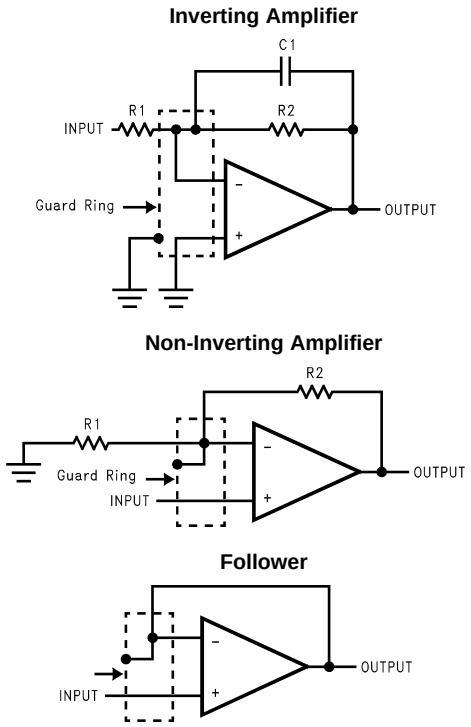
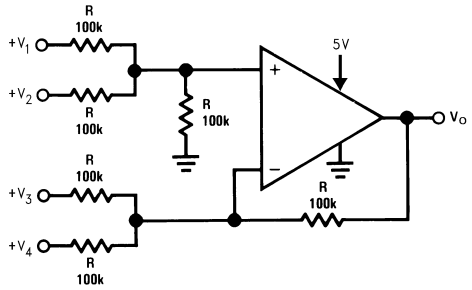


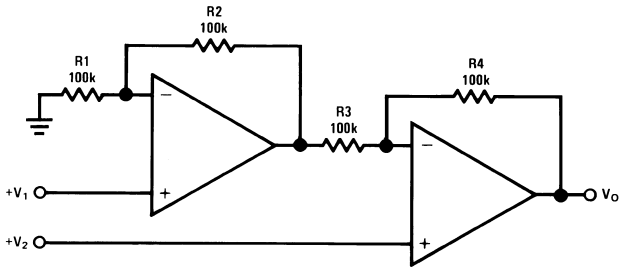
Figure 60. Typical Connections of Guard Rings

Application Circuits



Where: $V_0 = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2 \geq (V_3 + V_4)$ to keep $V_0 > 0V_{DC}$

Figure 61. DC Summing Amplifier ($V_{IN} \geq 0V_{DC}$ and $V_O \geq V_{DC}$



For

$$\frac{R1}{R2} = \frac{R4}{R3}$$

(CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$$

As shown: $V_O = 2(V_2 - V_1)$

Figure 62. High Input Z, DC Differential Amplifier

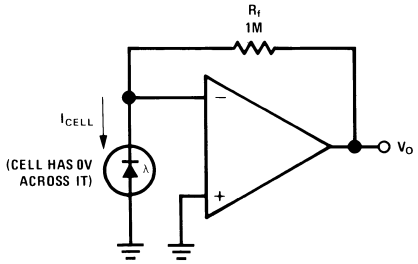
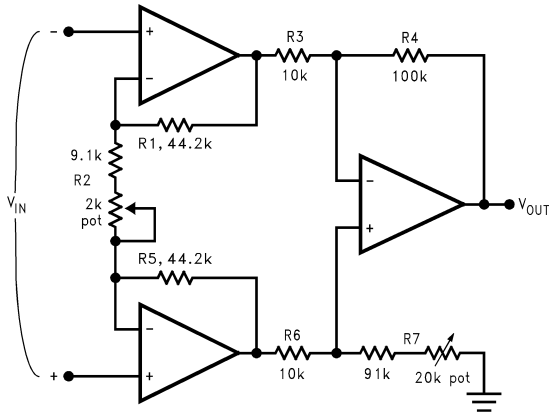


Figure 63. Photo Voltaic-Cell Amplifier

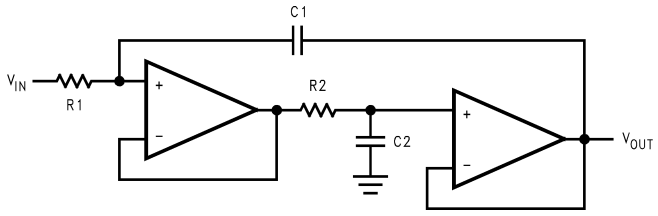


If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown (R_2 = 9.3k).

Figure 64. Instrumentation Amplifier



$$R1 = R2,\ C1 = C2;\ f = \frac{1}{2\pi R1C1};\ \text{Damping Factor} = \tfrac{1}{2}\sqrt{\frac{C2}{C1}}\sqrt{\frac{R2}{R1}}$$

Figure 65. Rail-to-Rail Single Supply Low Pass Filter

This low-pass filter circuit can be used as an anti-aliasing filter with the same supply as the A/D converter. Filter designs can also take advantage of the SM73306 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

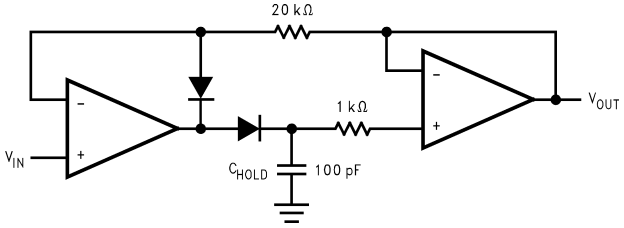
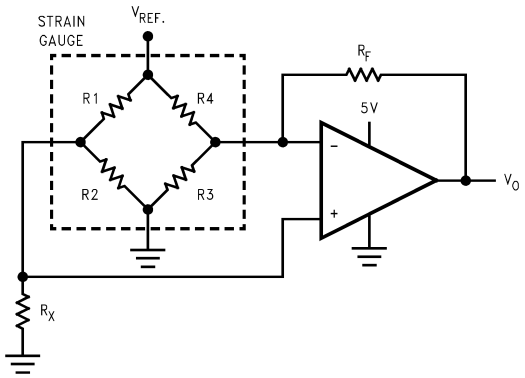


Figure 66. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

Dielectric absorption and leakage is minimized by using a polystyrene or polypropylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. Select low-leakage current diodes to minimize drooping.



$R_f = Rx$
$R_f >> R1, R2, R3, \text{and } R4$

$$V_O = \left(\frac{R2}{R1 + R2} - \frac{R3}{R4 + R3}\right) \frac{R_f (R3 + R4)}{R3\,R4} V_{REF}$$

Figure 67. Pressure Sensor

In a manifold absolute pressure sensor application, a strain gauge is mounted on the intake manifold in the engine unit. Manifold pressure causes the sensing resistors, R1, R2, R3 and R4 to change. The resistors change in a way such that R2 and R4 increase by the same amount R1 and R3 decrease. This causes a differential voltage between the input of the amplifier. The gain of the amplifier is adjusted by R_f.

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