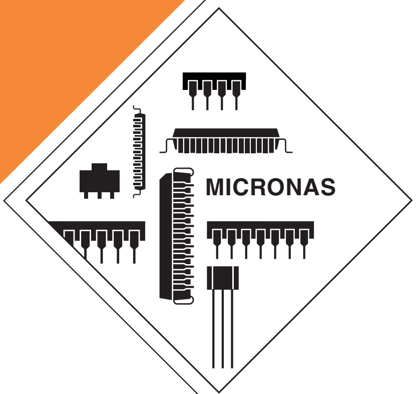

DATA SHEET

SDA 9489X, SDA 9589X
High-end
Picture-In-Picture ICs

Version B31

Edition March 15, 2004
6251-562-1DS

MICRONAS

Contents

Contents, continued

SDA 9489X, SDA 9589X
High-end Picture-In-Picture ICs

Release Note: Revision bars indicate significant changes to the previous edition.

1. General Description

SDA 9489x "PIP IV Advanced" and SDA 9589x "SOPHISTICUS" belong to a new generation of Picture-in-Picture (PIP) processors that combine high-quality digital PIP signal processing, digital multistandard color decoding and AD/DA conversion on a single chip. Both devices are equipped with CVBS and Y/C input interfaces. In addition the SDA 9589x is also able to process YUV input signals for displaying high quality video signals e.g. coming from a DVD source.

The integrated digital color decoder is able to decode all analog TV standards (PAL, NTSC and SECAM) and detects the standard automatically. Therefore the IC is suited for world-wide use.

A picture reduction from 1/4 to 1/81 of original size selectable in fine steps is possible. The transfer functions of the decimation filters are optimally matched to the selected picture size reduction and can furthermore be adjusted to the viewer's requirements by a selectable peaking. A maximum of 324 luminance and 2x81 chrominance pixels per line are stored in the memory. The PIP supports split-screen applications as well as multi-PIP display.

1.1. Features

– Single chip solution
  - AD-conversion for CVBS or Y/C or YUV (SDA 9589x only), multistandard color decoding, PLL for synchronization of inset channel, decimation filtering, embedded memory, RGB-matrix, DA-conversion, RGB/YUV switch, data-slicer and clock generation integrated on chip

– Analog inputs
  - 3x CVBS or 1x CVBS and 1x Y/C or 1xYUV alternatively (SDA 9589x only)
  - Clamping of each input
  - All ADCs with 8 bit amplitude resolution
  - Automatic Gain Control (AGC) for Y and CVBS

– Inset Synchronization
  - Multiple time constants for reliable synchronization
  - Automatic recognition of 625 lines/525 lines standard

– Color Decoder
  - PAL-B/G, PAL-M, PAL-N (Argentina), PAL60, NTSC-M, NTSC4.4 and SECAM
  - Adjustable color saturation
  - Hue control for NTSC
  - Automatic Chroma Control (-24 dB ... +6 dB)
  - Automatic recognition of chroma standards: different search strategies selectable
  - Single crystal for all standards
  - IF-characteristic compensation filter

– Decimation
  - PIP sizes between 1/81 and 1/4 adjustable with steps of 2 lines and 4 pixel
  - Resolution up to 324 luminance and 2x81 chrominance pixels per inset line
  - Horizontal and vertical filtering dependent on picture size
  - Automatic zoom in/out possible with three speeds

– Display Features
  - 7 bit per pixel stored in memory
  - Field and joint-line free frame mode display (even at 100/120 Hz AABB with picture sizes ≤1/9)
  - Two "split-screen" modes with horizontal decimation of 2 and vertical of 1.5 or 1.0 (1.0 with single-scan 50/60 Hz display only)
  - POP display
  - Up to 12 pictures of 1/36th size (11 still and 1 moving)
  - Up to 6 pictures of 1/16th size (5 still and 1 moving)
  - Up to 3 pictures of 1/9th size (2 still and 1 moving)
  - Display on VGA and SVGA screen (f_H limited to 40 kHz)
  - 8 different read frequencies for 16:9 compatibility
  - Line doubling mode for progressive scan applications
  - Freeze picture
  - Coarse positioning at 4 corners of the parent picture
  - Fine positioning at steps of 4 pixels and 2 lines
  - Wipe in / out programmable with 3 time periods

– Output signal processing
  - 7 Bit DAC
  - RGB or YUV switch: insertion of an external source without PIP processing
  - Digital interpolation for anti-imaging
  - Adjustable transient improvement for luma (peaking)
  - Contrast, Brightness and Pedestal Level adjustable
  - Analog outputs: Y, +(B-Y), +(R-Y), or Y, -(B-Y), -(R-Y) or RGB
  - Three RGB matrices available: NTSC (Japan), NTSC(USA) or EBU

  - 64 different background colors and 4096 different frame colors
  - Plain or 3D frame with variable width and height
- Data Slicing
  - Slicing of closed-caption (CC) or wide-screen-signaling (WSS) data
  - Violence blocking capability (V-chip)
  - Several filter for XDS data extraction
- On-screen display
  - 64 characters programmable
  - 5 characters displayed in every PIP picture or 3 rows of 20 characters each
  - 4 different character luminance values or frame color
  - 4 background luminance values or (semi-) transparent mode
- I²C-Bus control (400 kHz)
- High stability clock generation
- SOIC28-1 package (SMD)
- Full SDA 9488x and SDA 9588x backward compatibility
- SDA 9388X/SDA 9389X pinout compatibility
- 3.3 V supply voltage (5 V input capable)

1.2. Block Diagram

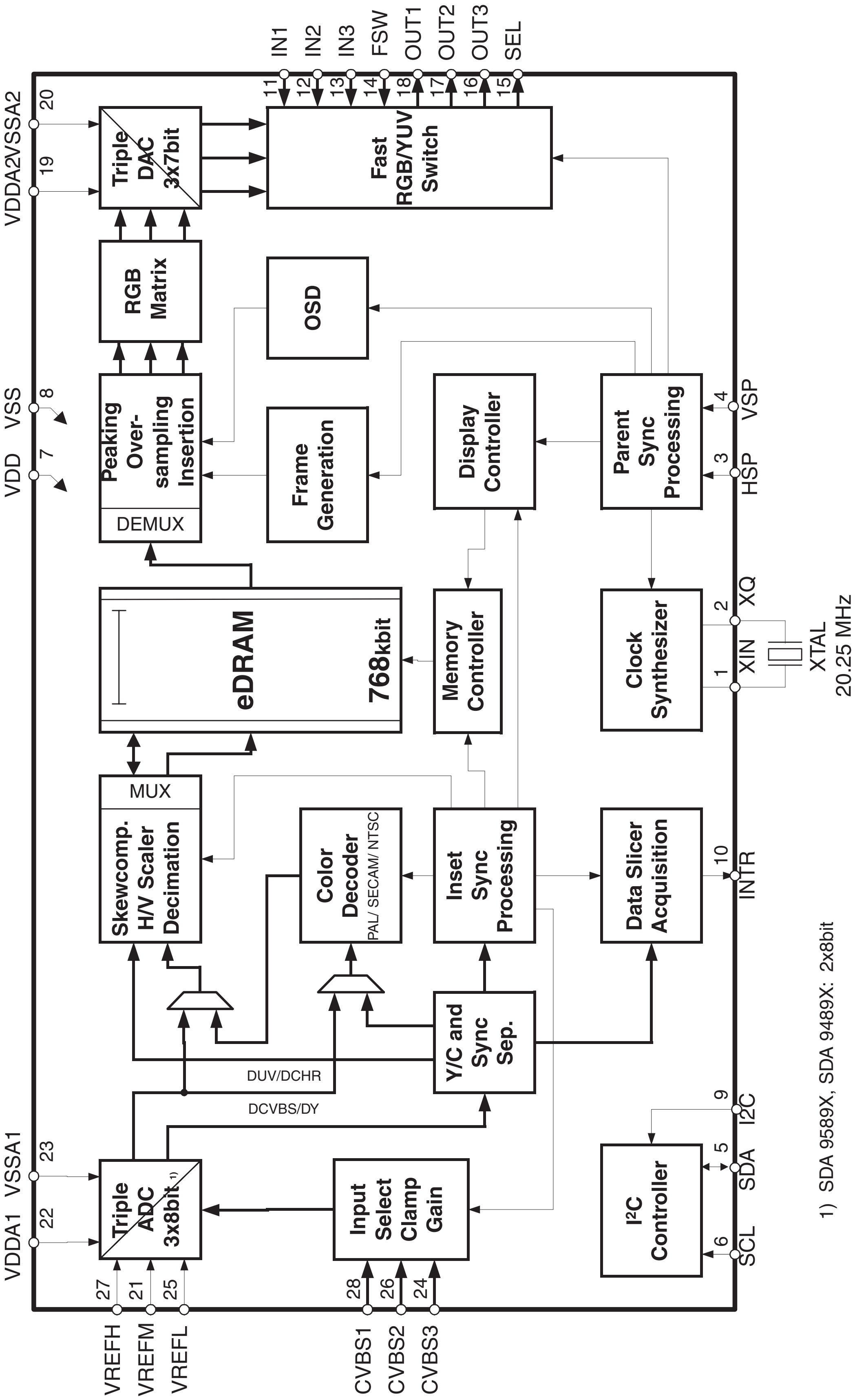

Fig. 1–1: Block Diagram

2. Functional Description

2.1. Analog Frontend

2.1.1. Input Selection

An analog inset CVBS signal can be fed to the inputs CVBS1-3 of SDA 9489x/SDA 9589x. Each of these sources is selectable via I²C bus (**CVBSEL**). CVBS2 and CVBS3 can be used as separate Y/C inputs. At SDA 9589x YUV sources can be connected to CVBS1, CVBS2 and CVBS3 provided YUV operation being enabled (**YUVSEL**). Using an external switch SDA 9589x can operate in applications with both YUV and CVBS signals. See Table 2–1

2.1.2. AD-Conversion

All signal are clamped and AD-converted with an amplitude resolution of 8 bit. CVBS and Y signals are clamped to the sync bottom or backporch, selectable by ***CLMSTGY***. U/V and C signals are always clamped to their mid-level during blanking.

The clamping pulse can be shifted in position (**CLMPIST**) and length (**CLMPID**) to adjust to the specific application. The ADCs are driven by a 20.25 MHz free running crystal clock which is not related to the incoming CVBS signal.

To avoid aliasing by sub-sampling the CVBS signal and the Y/C signals should be band-limited to 10 MHz. In the same manner the U/V signal frequency spectrum should not exceed 5 MHz. The digital filtering suppresses all frequencies above the usable spectrum.

2.1.3. Automatic Gain Control

To accommodate to different CVBS input voltages an automatic gain control has been implemented. The chip works correctly for input voltages in the range from 0.5 to 1.5 V_{pp}. For best signal-to-noise ratio, the maximum CVBS amplitude is recommended if available. The AGC behavior can be chosen out of four possibilities (**AGCMDE**).

The sync height serves as reference for the gain control in the typical application. When using overflow detection only, the gain is set to maximum and is reduced whenever an overflow occurs. This procedure will be executed again when a channel change is detected or the gain control is manually reset by **AGCRES**.

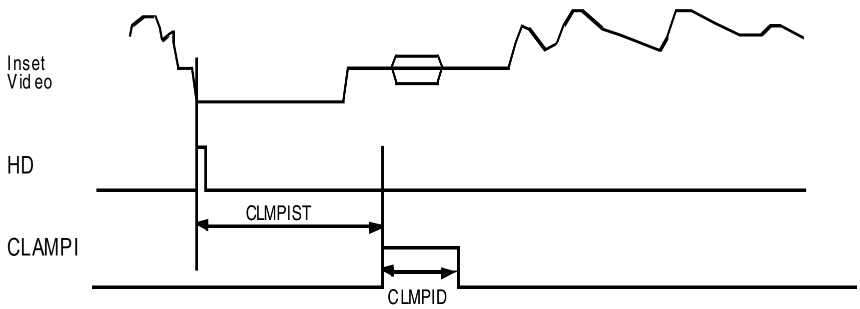

Fig. 2–1: Clamping Timing

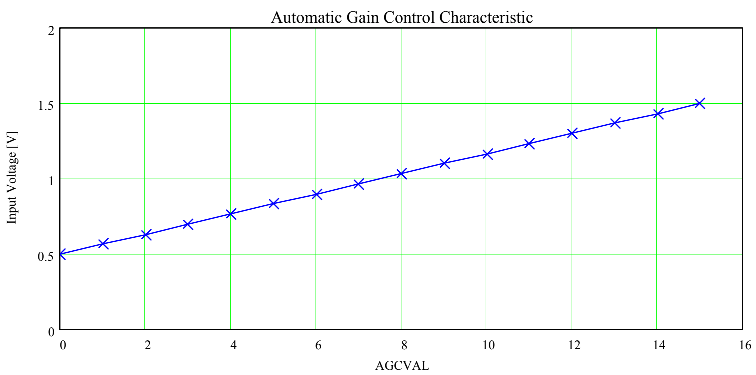

Fig. 2–2: AGC Characteristic

Table 2–1: Input selection

CVBSEL		YUVSEL	Input			Remark
D1	**D0**		**CVBS1**	**CVBS2**	**CVBS3**	
0	0	0	CVBS			
0	1	0		CVBS		
1	0	0		Y (VBS)	C	Y/C mode
1	1	0			CVBS	
X	X	1	Y (VBS)	U (CB)	V (CR)	YUV mode (only SDA 9589x)

2.1.4. Signal Magnitudes

The nominal CVBS signal with 75 % color has a magnitude of 1 V_{pp}. The upper headroom is left to permit signals with 100 % color resulting in 1.23 V_{pp}. The Y signal must always contain the sync part. Its levels correspond to the CVBS levels except for the missing color and burst. After A/D conversion the video part is clamped to its black value and is amplified to 224 digital steps. The nominal signal levels ensure correct brightness and saturation. The YUV signal levels conform to the ITU 601 recommendation.

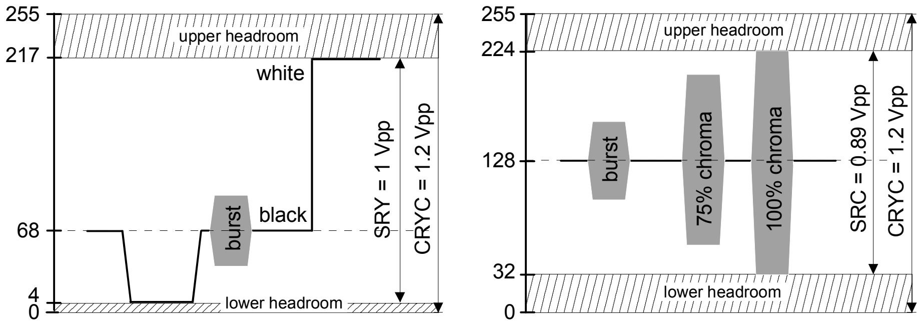

Fig. 2–3: CVBS/Y and Chroma ADC Input Signal Range

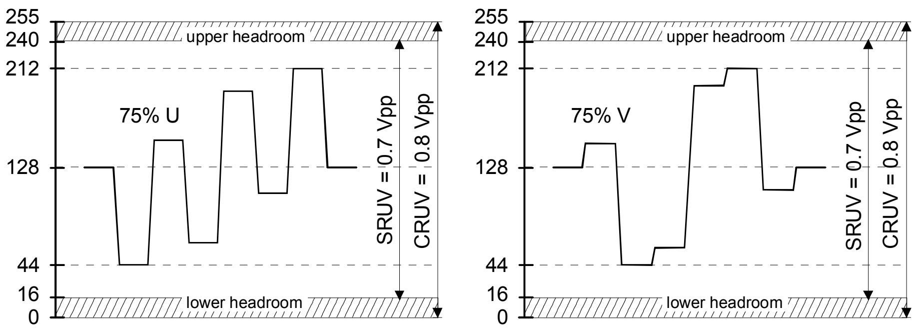

Fig. 2–4: UV Input Signal Range

Table 2–2: ADC conversion range and required input signal voltage

AGCVAL				Conversion Range CRYC	Signal Range SRY	Signal Range SRC	Conversion Range CRUV	Signal Range SRUV
D3	D2	D1	D0					
0	0	0	0	0.5 V_{pp}	0.42 V_{pp}			
			...	...	...			
1	0	0	0	1.2 V_{pp}	1.0 V_{pp}	0.89 V_{pp}	0.8 V_{pp}	0.7 V_{pp}
			...	...	...			
1	1	1	1	1.5 V_{pp}	1.25 V_{pp}			

2.2. Inset Synchronization

Horizontal and vertical sync pulses are separated after elimination of the high frequency components of the CVBS signal by a low pass filter. Horizontal sync pulses are generated by a digital phase-locked-loop (DPLL). Its time constant is adjustable between fast and slow behavior in four steps (**PLLITC**) to consider different input sources (e.g. VCR). Noisy input signals become more stable when a noise-reduction is enabled (**NSRED**). Additionally weak input signals from a satellite dish (“fishes”) become more stable when **SATNR** is enabled. Both should be enabled to have best available performance. A vertical flywheel mode improves vertical sync separation for weak signals (**VFLYWHL, VFLYWHLMD**). Additionally, V-syncs may be gated by **VTHRL50/60** and **VTHRH50/60** to reject invalid V-syncs. Dependent on detected line standard, the **VTHRx50** or **VTHRx60** setting is used. 50 Hz or 60 Hz operation for sync separation may be forced separately or selected to work automatically (**FLNSTRD**). When **NOSIGB** is enabled, a colored background is shown instead of the picture when PIP is out of (horizontal) synchronization. The detected line standard is indicated by **SYNCSTAT**.

2.3. Chroma Decoding and Standard Identification

The system is able to decode NTSC and PAL signals with a subcarrier of 3.58 MHz and 4.43 MHz (PAL B/M/N/60, NTSC M/4.4) as well as SECAM signals with 4.05/4.2 MHz subcarrier. The system may be forced to a certain standard, or an automatic standard detection can be used (**CSTAND**). For automatic standard detection, some standards which are not likely to be received can be ignored to improve the detection process.

Depending on the detected line standard (525 or 625 lines) the color standard detection circuit searches for 60 Hz signals (NTSC-M/PAL-M/PAL 60/NTSC44) or 50 Hz signals (PAL-B/SECAM/PAL-N) respectively. Within each line standard, the standard is detected by consequently switching from one to another. This standard detection process can be set to slow or fast behavior (**LOCKSP**). In slow behavior, 25 fields are used to detect the standard, whereas 15 fields are used in fast behavior. If unsuccessful within this time period the system tries to detect another standard.For SECAM detection, a choice between different recognition levels is possible (**SCMIDL, SECACCL, SECDIV**) and the evaluated burst position is selectable (**BGPOS**).

For getting the chrominance information the digitized video signal is multiplied with the regenerated color subcarrier once in-phase and once phase-shifted by 90°. After lowpass filtering digital UV is available for PAL and NTSC. The subcarrier is regenerated by a digital PLL. At SECAM operation the PLL runs free and generates the line-wise alternating subcarriers. A CORDIC structure demodulates the frequency-modulated UV signals. The following SECAM de-emphasis filter characteristic is adjustable **(DEEMP)**.
The chroma signal can be filtered before demodulation by means of a selectable IF-prefilter (**IFCOMP**).

Table 2–3: Considered color standards for automatic standard detection

CSTANDEX		NTSC-M	PAL60	PAL-N	PAL-M	PAL-B	SECAM	NTSC 44
D1	D0							
0	0	✓	✓			✓	✓	✓
0	1	✓		✓	✓			
1	0		✓			✓	✓	✓
1	1	✓				✓	✓	

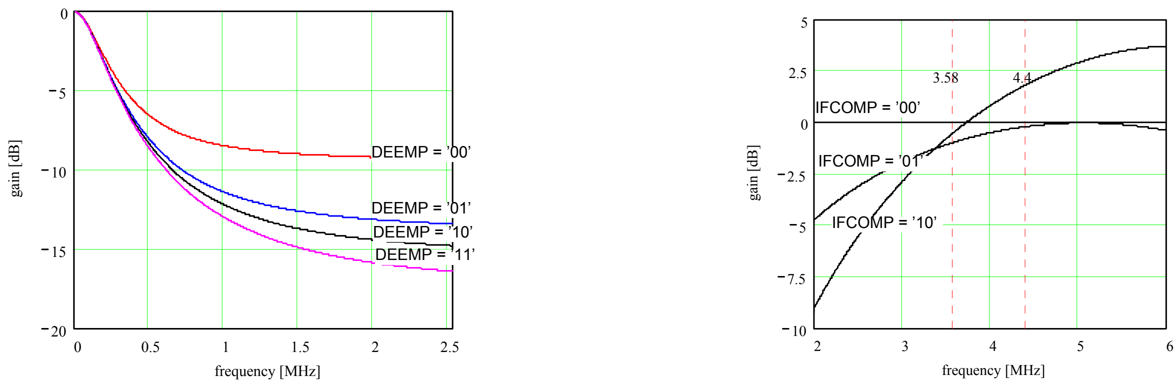

Fig. 2–5: SECAM De-emphasis Filter Characteristic and IF-compensation Filter Characteristic

The Hue Control (**HUE**) influences the phase of the demodulation subcarrier between -44.8° and 43.4° in steps of 1.4°. This is provided for NTSC only and adjustment is ineffective for PAL and SECAM signals.

The reference for the subcarrier generation is a crystal stable clock of 20.25000 MHz. In order to avoid color standard detection problems, the maximum deviation of this frequency should not exceed 100 ppm. For a good PLL locking behavior a maximum deviation of 40 ppm is recommended. A small frequency adjustment (-150 ... +310 ppm) is possible for using a crystal with small frequency deviations (**SCADJ**). For test purposes, **CPLL** allows to open the loop of the chroma PLL.

For deviations in the chroma signal up to 30 dB, a stable output amplitude after chroma decoding is achieved due to the ACC (Automatic Chroma Control). If the chroma signal (color burst) is below a selectable threshold (**CKILL**), the color will be switched off. Alternatively the color-killer can be bypassed and the color can be switched on or off under all conditions (**COLON**). By setting **ACCFIX**, the automatic chroma control is disabled and set to a default value.

The bandwidth of the chroma filter is adjustable via **CHRBW**. The bandwidth depends on whether the decoder is in SECAM operation or not. A change in **CHRBW** does not result in a chrominance position shift on the screen.

CKSTAT can be read out and gives information whether the color is switched on or off. **STDET** indicates the detected color standard. Additionally **PALID** and **PALDET** signal whether a PAL signal is applied.

Table 2–4: Color-killer adjustment

CKILL		COLON	Color Killed at Camping of
D1	D0		
0	0	0	30 dB
0	1	0	18 dB
1	1	0	24 dB
1	1	0	Color always off
X	X	1	Color always on

2.4. Comb Filtering

Depending on the selected picture size and color standard, a comb filtering is performed for luminance and chrominance. A comb filter uses the spectral interleaving of the encoded luminance and chrominance to separate both without cross artifacts. Thus cross-color and cross-luminance are suppressed effectively. For NTSC sources, a comb filtering is performed for all picture sizes. Due to reduced bandwidth in horizontal and vertical direction a strong reduction of cross artifacts can be achieved for PAL signals. The same applies for the luminance signal of SECAM signals.

2.5. Luminance Processing

The A/D-converted CVBS (or Y) signal is digitally clamped to back porch. Depending on the transmitted standard and operational area, an offset between black- and blanking level can be found in the incoming signal (“7.5 IRE”). As for some applications a black offset is not desired, controlling may be done using **LMOFST**. The positive or negative offset is added to the Y signal before scaling.

The color carrier is removed out of a CVBS signal by means of a notch filter. It is set to the corresponding color carrier (3.58 or 4.4 MHz) only if the standard is detected permanently. This prevents the luminance sharpness of being changed within the standard search process. For Y signals the notch is disabled. A special peaking can be applied to the notch-filter (**NADJ**) to make it steeper. For a fine adjustment of delay compensation between luminance and chrominance, **YCDEL** allows a luminance shifting in 16 steps of 50 ns.

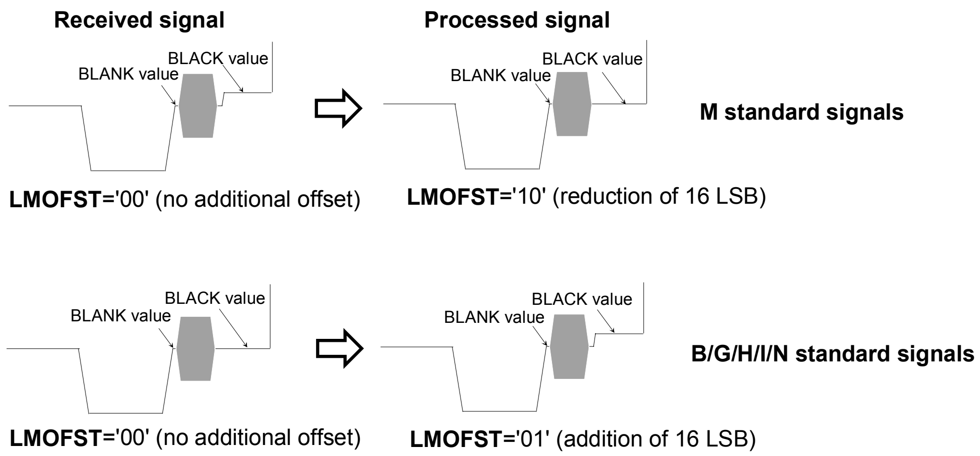

Fig. 2–6: Black Level Correction of Luminance Signal

2.6. Decimation

2.6.1. Single PIP Mode

Luminance and chrominance signals are filtered in horizontal and vertical direction. The coarse horizontal and vertical picture size (1/2, 1/3, 1/4, 1/6) is independently programmable with **SIZEHOR** and **SIZEVER**. A fine adjustment in steps of 4 pixel and 2 lines is possible by **HSHRINK** and **VSHRINK**, which allows correct aspect ratio for multistandard applications (50/60 Hz mixed mode, (S)VGA).

For main decimation factors, the stored number of pixel and lines are listed in the following tables.

Table 2–5: Number of stored pixel per line dependent on SIZEHOR

SIZEHOR		Horizontal Scaling	PIP Pixel per Line		
D1	D0		Y	(B-Y)	(R-Y)
0	0	2:1	324	81	81
0	1	3:1	216	54	54
1	0	4:1	160	40	40
1	1	6:1	108	27	27

Table 2–6: Number of stored lines per field

SIZEVER		Vertical Scaling	PIP Lines	
D1	D0		625 Lines Source	525 Lines Source
0	0	2:1	132	108
0	1	3:1	88	72
1	0	4:1	66	54
1	1	6:1	44	36

2.6.2. Continuous Zoom

The continuos zoom feature changes the picture size rapidly in an animated manner. It is available in single-PIP mode for picture sizes smaller or equal 1/4 of the undecimated picture.

There are three possibilities of using the zoom feature:

– The PIP is zoomed via **HSHRINK** and **VSHRINK** manually. This requires an I^2C protocol each time the picture size should change. **CZMEN** should be used to synchronize the update of **HSHRNK/ VSHRNK** with **SIZEHOR/SIZEVER**.

– A different way is to make usage of the *automatic* zooming. The zoom speed can be controlled by **CZMSP**. When switching PIP on or off by using **PIPON**, the PIP zooms automatically to the selected picture size or disappears at size of 1/81.

– A zooming between two picture sizes can be performed by changing the **HSHRINK**, **VSHRINK, SIZEHOR, SIZEVER** values when **CZMEN** is enabled. Then the new picture size is obtained by zooming and not taken immediately.

Automatic zooming is only possible in *frame mode*. Being in *field mode*, the picture size remains stable until frame mode occurs or until the internal counter reaches the desired picture size. Then the size changes immediately. Equal to the wipe process, the zooming direction depends on the coarse position (**CPOS).**

HSHRNK	SIZEHOR	Decimation Factor	stored Pixel
0	0	2,00	324
1	0	2,02	320
2	0	2,05	316
3	0	2,08	312
4	0	2,10	308
5	0	2,13	304
6	0	2,16	300
7	0	2,19	296
8	0	2,22	292
9	0	2,25	288
10	0	2,28	284
11	0	2,31	280
12	0	2,35	276
13	0	2,38	272
14	0	2,41	268
15	0	2,45	264
16	0	2,49	260
17	0	2,53	256
18	0	2,57	252
19	0	2,61	248
20	0	2,66	244
21	0	2,70	240
22	0	2,74	236
23	0	2,80	232
24	0	2,84	228
25	0	2,89	224
26	0	2,95	220

HSHRNK	SIZEHOR	Decimation factor	stored Pixel
0	1	3,00	216
1	1	3,04	212
2	1	3,11	208
3	1	3,17	204
4	1	3,23	200
5	1	3,29	196
6	1	3,37	192
7	1	3,44	188
8	1	3,51	184
9	1	3,60	180
10	1	3,67	176
11	1	3,76	172
12	1	3,84	168
13	1	3,94	164
0	2	4,05	160
1	2	4,16	156
2	2	4,27	152
3	2	4,38	148
4	2	4,50	144
5	2	4,63	140
6	2	4,77	136
7	2	4,91	132
8	2	5,06	128
9	2	5,22	124
10	2	5,41	120
11	2	5,59	116
12	2	5,78	112

HSHRNK	SIZEHOR	Decimation factor	stored Pixel
0	3	6,00	108
1	3	6,23	104
2	3	6,48	100
3	3	6,75	96
4	3	7,04	92
5	3	7,35	88
6	3	7,70	84
7	3	8,10	80
8	3	8,52	76
9	3	8,99	72
10	3	9,51	68
11	3	10,12	64
12	3	10,64	60

Fig. 2–7: Number of Stored Pixel per Line Dependent on HSHRNK

		625 lines		525 lines	
VSHRNK	SIZEVER	Decimation Factor	Lines	Decimation Factor	Lines
0	0	2	132	2	108
1	0	2,03	130	2,03	106
2	0	2,06	128	2,08	104
3	0	2,09	126	2,13	102
4	0	2,13	124	2,16	100
5	0	2,16	122	2,2	98
6	0	2,2	120	2,25	96
7	0	2,23	118	2,3	94
8	0	2,28	116	2,34	92
9	0	2,31	114	2,41	90
10	0	2,36	112	2,45	88
11	0	2,41	110	2,52	86
12	0	2,44	108	2,58	84
13	0	2,48	106	2,64	82
14	0	2,53	104	2,7	80
15	0	2,59	102	2,77	78
16	0	2,64	100	2,84	76
17	0	2,69	98	2,92	74
18	0	2,75	96		
19	0	2,81	94		
20	0	2,88	92		
21	0	2,94	90		
0	1	3	88	3	72
1	1	3,07	86	3,09	70
2	1	3,14	84	3,19	68
3	1	3,21	82	3,28	66
4	1	3,3	80	3,38	64
5	1	3,38	78	3,49	62
6	1	3,47	76	3,61	60
7	1	3,56	74	3,73	58
8	1	3,66	72	3,87	56
9	1	3,77	70		
10	1	3,89	68		

		625 lines		525 lines	
VSHRNK	SIZEVER	Decimation Factor	Lines	Decimation Factor	Lines
0	2	4	66	4,01	54
1	2	4,13	64	4,15	52
2	2	4,25	62	4,31	50
3	2	4,41	60	4,5	48
4	2	4,56	58	4,69	46
5	2	4,72	56	4,9	44
6	2	4,88	54	5,13	42
7	2	5,06	52	5,39	40
8	2	5,28	50	5,7	38
9	2	5,5	48		
10	2	5,75	46		
0	3	6	44	6	36
1	3	6,28	42	6,38	34
2	3	6,61	40	6,75	32
3	3	6,94	38	7,22	30
4	3	7,31	36	7,73	28
5	3	7,78	34	8,3	26
6	3	8,25	32	9	24
7	3	8,81	30	9,8	22
8	3	9,42	28	10,78	20
9	3	10,17	26		
10	3	11,02	24		

Fig. 2–8: Number of Stored Lines per Field Dependent on VSHRNK

2.6.3. Horizontal And Vertical Fine Positioning

All picture sizes are pre-centered inside the frame. In addition, if necessary the vertical and horizontal acquisition area can be shifted by **VFP** for vertical and **HFP** for horizontal direction.

2.6.4. Multi Display Mode

SDA 9589x and SDA 9489x offer the feature to display a sub-picture more than once. The picture size and arrangement depends on the display mode (**DISPMOD**) and not on **SIZEHOR** or **SIZEVER**. Hence variable scaling is not possible in these modes.

The display modes are shown in the appendix. The sizes of the partial pictures are listed in Table 2.7.

2.6.5. Split Screen

For split screen applications two selectable "double window" modes in which one half of the picture is generated by the "Sophisticus"/"PIP IV Advanced" can be used. The split screen mode can be selected by two possible combinations of **DISPMOD**.

The D1.5 mode is suited for displaying split screen on 16:9 tubes keeping the aspect ratio. The DW1 format covers the full height of the screen. The DW1 format is only suited for 50/60 Hz single-scan applications and is not suited for 100 Hz or "progressive" displays.

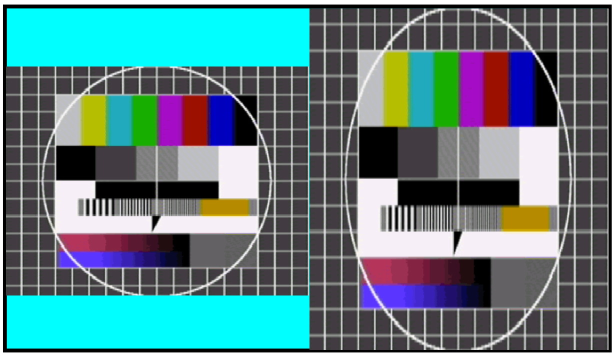

Fig. 2–9: Double Window Mode 1.5 (Left Picture) and Mode 1 (Right Picture)

Table 2–7: Multi-display modes

Display Mode	DISPMOD		Size	Picture Configuration	Pixel	Lines	
	D1	D0				625	525
1	0	0	SIZEHOR/SIZEVER HSRHNK/VSHRNK	Single PIP mode	324 - 60	132 - 24	108 - 20
2	0	1	3 X1/9	One upon another (same content)	216	264	216
3	1	0	4 X 1/16	One upon another (same content)	156	264	216

2.6.6. Multi-PIP Mode

Table 2–8: Maximum number of pictures in multi-PIP mode

Picture Sizes	Maximum Number of Pictures (Including One Live Picture)
1/9	3
1/16	6
1/36	12

There is a great variety of multi-PIP modes available. Up to 11 different still pictures and one moving picture can be shown. This is useful to give an overview over broadcasted programmes (e.g. tuner-scan) or for supervising purposes. For multi-PIP modes only three fixed picture sizes are available (1/9, 1/16 or 1/36). The picture size and arrangement depends on the display mode (**DISPMOD**) and not on **SIZEHOR** or **SIZEVER**. Variable scaling is thus not possible in these modes. Because of limited memory capacity, the number of frozen multi-pictures is limited dependent on picture size to the number shown in Table 2–8

The partial picture that is written is addressed via **WRPOS**. With **INFRM**, a frame for separation of every PIP can be selected. This is adjustable to single or dual PIP mode (**INFRMOD**). The current updated picture can be highlighted with **PIPHLT**. To avoid garbage pictures after switching from one mode to another the selected picture can be blanked with **PIPBLK**. **MPIPBG** defines wether the picture will be blanked with black or with the adjusted background color.

For compatibility reasons to other devices, the **DISPMOD** register is split into two segments. If a display mode is chosen that is not implemented, the PIP insertion is switched off automatically (**PIPON** = ’0’). The sizes of the partial pictures correspond to the sizes of the inset pictures of the single PIP modes.

Table 2–9: Display Modes

Display Mode	DISPMOD					Size	Picture Configuration	Pixel	Lines	
	D6	D5	D4	D3	D2				625	525
4	0	0	0	0	1	2 X 1/9,	One upon another	216	176	144
5	0	0	0	1	0	2 X 1/9,	Side by side	432	88	72
6	0	0	0	1	1	3 X 1/9,	Side by side	648	88	72
7	0	0	1	0	0	3 X 1/9	One upon another	216	264	216
8	0	0	1	0	1	4 X 1/16	Side by side	624	66	54
9	0	0	1	1	0	6 X 1/16	Inverted U shaped	624	132	108
10	0	0	1	1	1	6 X 1/16	U shaped	624	132	108
11	0	1	0	0	0	4 X 1/16	2 rows of 2 pictures	312	132	108
12	0	1	0	0	1	4 X 1/16	One upon another	156	264	216
13	0	1	0	1	0	12 X 1/36	6 rows of 2 pictures	216	264	216
14	0	1	0	1	1	12 X 1/36	2 rows of 6 pictures	648	88	72
15	0	1	1	0	0	9 X 1/36	3 rows of 3 pictures	324	132	108
16	0	1	1	0	1	12 X 1/36	3 rows of 4 pictures	432	132	108
17	0	1	1	1	0	11 X 1/36	Angular of 11 pictures	648	264	216
18	0	1	1	1	1	9 X 1/36	Angular of 9 pictures	540	220	180
19	1	0	0	0	0	1X1/3	Double Window (V=1.5)	324	176	144
20	1	0	0	0	1	1X1/2	Double Window (V=1)[1)]	324	264	216
21	1	0	0	1	0		OSD only			
	All other						PIP off (PIPON=0)			

[1)] Single-scan display only

2.7. Display Control

The on-chip memory capacity is 768 kBits. Provided that the same standard (50 or 60 Hz) video sources are applied to inset and parent channel, joint-line free frame mode display is possible. This means that every incoming field is processed and displayed by the SDA 9589x/SDA 9489x processors. The result is a high vertical and time resolution. For this purpose the standard is analyzed internally and frame mode display is blocked automatically, if the described restrictions are not fulfilled. Then only every second incoming field is shown (field mode). Field mode normally shows joint-lines. This is caused by an update of the memory during read out. The result is that one part of the picture contains new picture information and the other part contains one earlier written field. The switching from or to frame mode is free of artifacts.

Activation of frame-mode display is blocked automatically if at least one of the following conditions is not fulfilled:

– Inset and parent channel have the same field repetition frequency. This means that frame mode is possible only for 50 Hz inset and parent sources or 60 Hz inset and parent sources.
– Interlace signal is detected for inset and parent channel. For progressive scan or (S)VGA display therefore only field mode is possible. For some VCRs in trick mode, often no interlace is detected also.
– The number of lines is within a predefined range for inset (**FMACTI**) or parent (**FMACTP**) channel (assuming standard signals according to ITU)

The system may be forced to field mode by means of **FIESEL.** Either first or second field is selectable. “One of both” takes every second field independent of the field number. This is meant for sources generating only one field (e.g. video-games).

For progressive scan conversion systems and HDTV/(S)VGA displays a line doubling mode is available (**PROGEN**). Every line of the inset picture is read twice.

Memory writing is stopped by **FREEZE** bit. The field stored in the memory is then continuously read. As the picture decimation takes place before storing, the picture size of a frozen picture can not be changed.

Synchronization of memory reading with the parent channel is achieved by processing the parent horizontal and vertical synchronization signals connected to the pin HSP for horizontal synchronization and pin VSP for vertical synchronization. **HSPINV** or **VSPINV** respectively allow an inversion of the expected signal polarity.

Table 2–10: Required number of lines for frame mode display

FMACTP	Parent Standard	Number of Lines per Field	FMACTI	Inset Standard	Number of Lines per Field
0	50 Hz	310...315	0	50 Hz	310...315
1	50 Hz	290...325	1	50 Hz	290...325
0	60 Hz	260...265	0	60 Hz	260...265
1	60 Hz	250...275	1	60 Hz	250...275

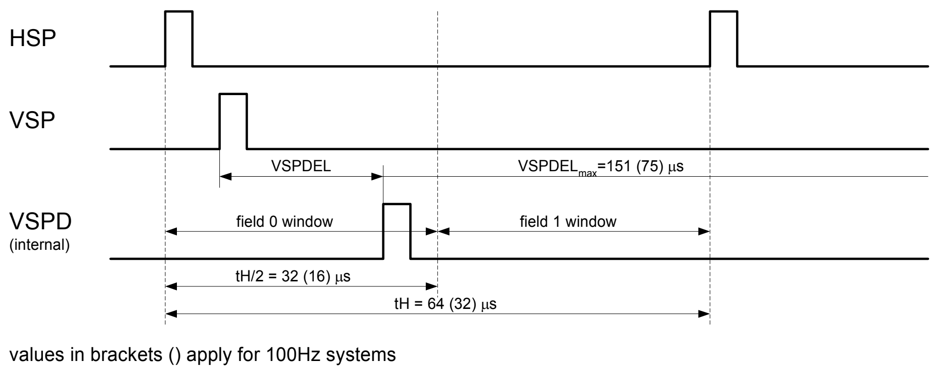

Fig. 2–10: Field Detection and Phase Adjustment of Vertical Pulse (VSP)

Depending on the phase between inset and parent signals a correction of the display raster for the read out data is performed. As the external VSP and HSP signals may come from different devices with different delay paths, the phase between V-sync and H-sync is adjustable (**VSPDEL**). An incorrect setting of **VSPDEL** may result in wrong or unreliable field detection of parent channel.

Normally a noise reduction of the incoming parent vertical pulse is performed. With this function missing vertical pulses are compensated. The circuit works for 50/60 Hz applications as well as progressive and 100/120 Hz application. (S)VGA signals are supposed to be very stable and therefore not supported by the noise suppression. By means of **VSPNSRQ,** vertical noise suppression is switched off.

A great variety of combinations of inset and parent frequencies are possible. The following table shows some constellations.

Table 2–11: Available features with varying inset and parent standards

Inset Frequency[1]	**Parent Frequency**[1] **(HSP/VSP)**	**Frame Mode**	**Correct Aspect Ratio (Single PIP)**	**Correct Aspect Ratio (Multi Display)**	**Vertical Noise Suppression Selectable**
50	50i	✓	✓	✓	✓
50	60i		✓		✓
60	50i		✓		✓
60	60i	✓	✓	✓	✓
50	50p		✓	✓	✓
50	60p		✓		✓
60	50p		✓		✓
60	60p		✓	✓	✓
50	100i	✓[1]	✓	✓	✓
50	120i		✓		✓
60	100i		✓		✓
60	120i	✓[2]	✓	✓	✓
50	(S)VGA		✓	✓[1]	
60	(S)VGA		✓	✓[3]	

1) Standard signals supposed
2) AABB only and picture size smaller than 1/9
3) Valid for some parent frequencies. Please refer to Section 2.7.2.

2.7.1. 100 Hz Frame Mode

If the picture size is smaller or equal than 1/9 PIP a true frame mode display for 100 Hz parent standard with a double field repetition rate is possible (display raster ααββ only). The picture size is indicated by the horizontal and vertical decimation factors that must be equal or below 1/3 of undecimated picture size in both directions. This guarantees enough memory for a joint-line free picture with full vertical resolution. For bigger pictures only field mode is supported. The 100 Hz frame mode is activated if **READD**='1' for the above mentioned picture sizes. For an acceptable quality without line flicker or motion artifacts only the mode ααββ is supported for HSP and VSP. If the sequence αβαβ is detected, the field mode will be activated again. Continuos switching between these modes is possible, resulting in continuos switching between field- and frame mode.

2.7.2. Mixed Standard Applications and (S)VGA Support

SDA 9589x and SDA 9489x allow multiple scan rates for the use in desktop video applications, VGA compatible or 100 Hz TV sets. All features are provided in "normal" operating modes at auto detected 50 Hz and 60 Hz parent and inset standards. $2f_H$ modes (100/120 Hz and progressive) are supported by line frequency- and pixel clock doubling and are not detected automatically. Even on a 16:9 picture tube correct aspect ratio can be displayed by selecting the suitable parent clock. The video synthesizer generates also a special pixel clock for VGA display (see chapter 5.5.9 for details). As (S)VGA consists of a variety of scan rates the correct aspect ratio is not adjustable for all modes with the parent clock (**HZOOM**) because of the limited count of frequencies. For single PIP only, correct aspect ratio is maintained by the vertical and horizontal scaler (**HSHRINK** and **VSHRINK**).

Table 2–12: Examples of supported parent signals

Remark (N_{apel} x N_{aline} @ f_V)	f_H (kHz)	T_H (µs)	T_{Hact} (µs)	Lines/ Active	f_{dot} (MHz)	Scan	Correct Aspect Ratio
720 x 576@50 Hz (TV)	15.6	64.0	52.0	625/576	13.5	Interlace	✓
702 x 488@60 Hz (TV)	15.7	63.6	52.7	525/488	13.5	Interlace	✓
720 x 576@100 Hz (TV 100 Hz)	31.2	32.0	26.0	625/576	27	Interlace	✓
702 x 488@120 Hz (TV 120 Hz)	31.2	31.8	26.4	525/488	27	Interlace	✓
720 x 576@50 Hz (TV progressive)	31.2	32.0	26.0	625/576	27	Progressive	✓
702 x 488@60 Hz (TV progressive)	31.2	31.8	26.4	525/488	27	Progressive	✓
640 x 480@60 Hz (VGA)	31.5	31.8	25.4	525/480	25.2	Progressive	✓
640 x 480@72 Hz (VGA)	37.9	26.4	20.3	520/480	31.5	Progressive	✓
640 x 480@75 Hz (VGA)	37.5	26.7	20.3	500/480	31.5	Progressive	✓
800 x 600@56 Hz (SVGA)	35.2	28.4	22.2	625/600	36.0	Progressive	✓
800 x 600@60 Hz (SVGA)	37.9	26.4	20.0	625/600	40.0	Progressive	
800 x 600@72 Hz (SVGA)	48.1	20.8	16.0	666/600	50.0	Progressive	
800 x 600@75 Hz (SVGA)	46.9	21.3	16.2	625/600	49.5	Progressive	
800 x 600@85 Hz (SVGA)	53.7	18.6	14.2	631/600	56.3	Progressive	
1024 x 768@43 Hz (SVGA)	35.5	28.2	22.8	817/768	44.9	Interlace	

It is possible to display (S)VGA sources for parent display, as long as the horizontal frequency is lower than 40 kHz and the signal does not contain more than 1023 lines. For progressive scan mode, **PROGEN** must be set. Additionally *field-mode* should be forced to prevent not allowed *frame-mode* displaying (**FIESEL**). As the (S)VGA normally does not fit to the display raster generated in the vertical noise suppression, **VSPNSRQ** should be disabled. (S)VGA signals for inset channel are not supported.

Table 2–13: Selection of display field repetition

PROGEN	READD	Expected Input Signal
0	0	50 or 60 Hz Signal Interlace
0	1	100 or 120 Hz Signals Interlace
1	0	(Reserved)
1	1	50 or 60 Hz or (S)VGA Signal Progressive

2.7.3. Display Standard

For a single-PIP, the number of displayed lines depends on the selected picture size and on the signal standard. For multi picture display, the number of displayed lines depends on the selected picture size and on the signal standard of the parent signal. Additionally, a standard can be forced by **DISPSTD**. See Table 2–14.

If a 625 lines picture is shown with a 525 lines parent signal, some lines are missing on top and bottom of picture. If a 525 lines picture is shown with a 625 lines display standard, missing lines at top and bottom are filled with background color or black depending on **MPIPBG**.See Fig. 2–11.

Table 2–14: Display standard selection

DISPSTD		DISP MOD	Display Standard
D1	D0		
0	0	0	PIP depends on detected inset standard (single PIP)
0	0	>0	PIP depends on detected parent standard (multi display)
0	1	x	PIP display is always in 625 lines mode

Table 2–14: Display standard selection, continued

DISPSTD		DISP MOD	Display Standard
D1	D0		
1	0	x	PIP display is always in 525 lines mode
1	1	x	Freeze last detected display standard and size

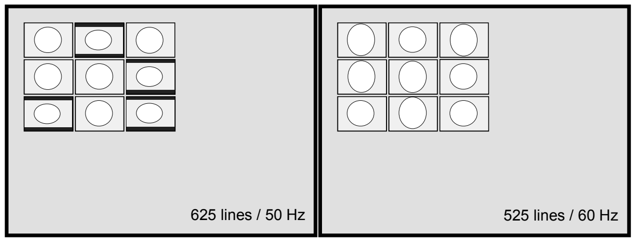

Fig. 2–11: 50 and 60 Hz Multi PIP Display on 50 Hz and 60 Hz Display

2.7.4. Picture Positioning

The display position of the inset picture is programmable to the 4 corners of the parent picture (**CPOS**). From there PIP can be moved to the middle of the TV Picture with **POSHOR** and **POSVER**. The corner positions can be centered coarsely on the screen with **POSOFH** and **POSOFV**. Depending on coarse position, one PIP corner remains stable when changing the picture size.

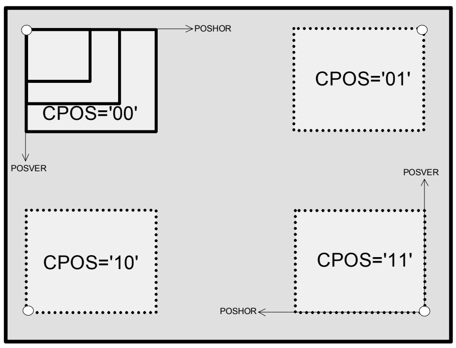

Fig. 2–12: Coarse Positioning

There are 256 horizontal locations (4 pixel increments) and 256 vertical locations (2 line increments). The pixel width on the screen depends on the selected **HZOOM** factor. Even POP-positions (Picture Outside Picture) in 16:9 applications are possible.

Table 2–15: Coarse positioning

CPOS		Coarse Position	Reference Corner of PiP	Increasing POSVER	Increasing POSHOR
D1	D0				
0	0	Upper left	Upper left	Down	Right
0	1	Upper right	Upper right	Down	Left
1	0	Lower left	Lower left	Up	Right
1	1	Lower right	Lower right	Up	Left

2.7.5. Wipe In/Wipe Out

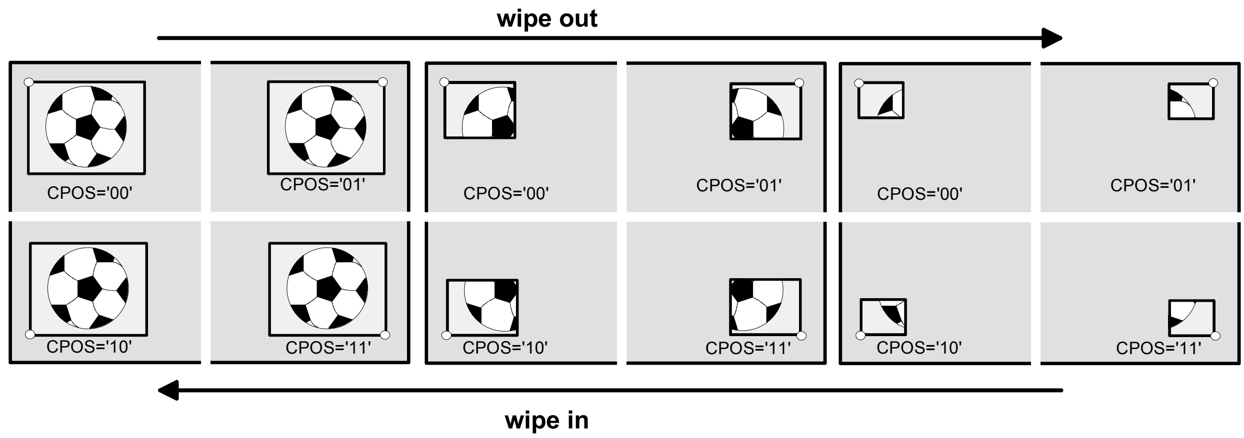

Fig. 2–13: Wipe Display

With the wipe in/wipe out function it is possible to let appear or disappear the complete inset picture starting or ending at the corner of the inset picture position defined by **CPOS**. Thereby the size of the visible picture-part is continuously increased and decreased respectively. During this procedure the frame is shown with its chosen widths. 3 different wipe in/out time periods or “no wipe” are programmable via **WIPESP**. The wipe algorithm always works in horizontal and vertical direction.

If **WIPESP** is set accordingly, **PIPON** controls the wipe operation. When **PIPON** changes the wipe operation starts. During this period, the readable **PIPSTAT** indicates the ongoing wipe-process. A transition of **PIPON** from ’0’ to ’1’ triggers the wipe-in. The wipe-in process stops when the picture reaches its programmed size. When **PIPON** changes from ’1’ to ’0’ the wipe-out starts. The wipe-out is finished when the PIP picture vanishes. Even for multi-picture display wipe operation is possible. A change of **PIPON** or **WIPESP** during wipe operation has only an effect after the wipe operation has been finished.

2.8. Output Signal Processing

2.8.1. Luminance Peaking

To improve picture sharpness, a peaking filter which amplifies higher frequencies of the input signal is implemented. The amount of peaking can be varied in seven steps by **YPEAK**. The setting '000' switches off the peaking. The value '011' is recommended as this value provides a good compromise between sharpness impression and annoying aliasing. The characteristic for all possible settings is shown in fig. (2–14). The emphasized frequency depends on the adjusted decimation. The gain maximum is always located before the band-limit ensuring optimal picture impression. Peaking can be additionally increased by **PKBOOST**.

Coring should be switched on by **YCOR** to reduce noise, which is also amplified when peaking is enabled. As the coring stage is in front of the peaking filter, 1 LSB noise will not be peaked.

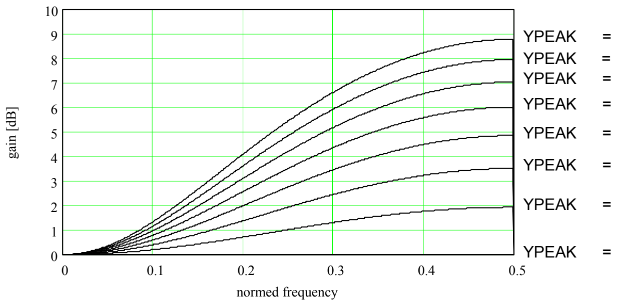

Fig. 2–14: Characteristics of Selectable Peaking Factors (0.5 = band limit)

2.8.2. RGB Matrix

The chip contains three different matrices, one suited for EBU standards, one suited for NTSC-Japan and one suited for NTSC-USA, which are selected via **MAT**. The signal **OUTFOR** switches between YUV output or RGB output. The signal **UVPOLAR** inverts the U and V channels and results in Y-U-V output. The standard magnitudes and angles of the color-difference signals in the UV-plane are defined as shown in Table 2–16.

The color saturation can be adjusted with **SATADJ** register in 16 steps between 0 and 1.875. Values above 1.0 may clip the chrominance signals.

Table 2–16: RGB matrices characteristics

MAT		Magnitudes			Angles			Standard
D1	**D0**	**(B-Y)**	**(R-Y)**	**(G-Y)**	**(B-Y)**	**(R-Y)**	**(G-Y)**	
0	0	2.028	1.14	0.7	0	90	236	EBU
0	1	2.028	1.582	0.608	0	95	240	NTSC (Japan)
1	0	2.028	2.028	0.608	0	105	250	NTSC (USA)
1	1							(Reserved)

2.8.3. Frame Generation and Colored Background

With **FRSEL** a colored frame is added to the inset picture. The chip can display two different types of frames, one simple monochrome frame and a more sophisticated frame giving a three dimensional impression.

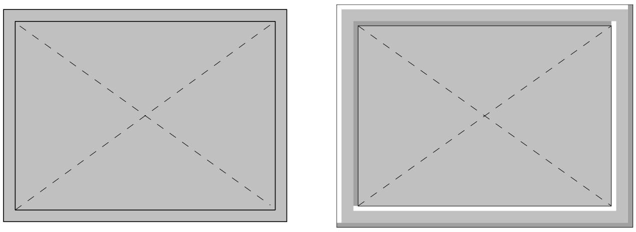

Fig. 2–15: Normal Frame and 3D Frame

The frame elements are always placed outside the inset picture, except for the inner shade of three dimensional frame or inner frame in multi-PIP mode. There is no shift of the inset picture position if the inset frame width is modified.

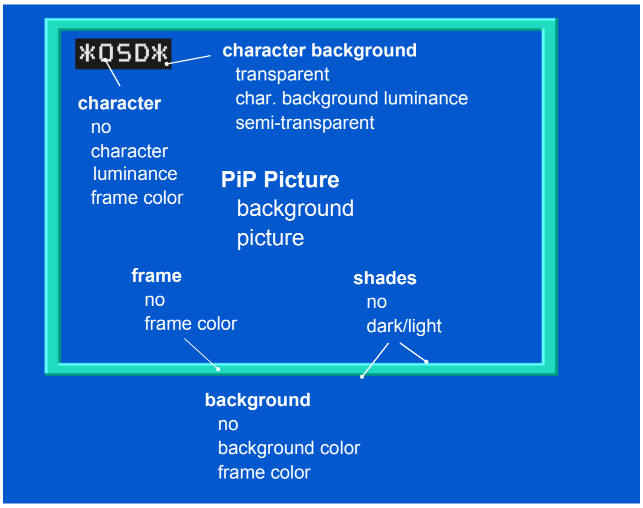

Fig. 2–16: Selectable Picture Configurations

4096 frame colors are programmable by **FRY**, **FRU**, and **FRV**, 4 bits for each component. Horizontal and vertical width of the frame are programmable independently by **FRWIDH** and **FRWIDV**. If desired, frame color is displayed over the whole PIP size or whole picture size of the main channel when **PIPBG** is set accordingly. 64 background colors are programmable by **BGY**, **BGU**, **BGV**, 2 bits for each component. Alternatively **BGFRC** sets the background to frame color.

2.8.4. 16:9 Inset Picture Support

To remove dark stripes at 16:9 inset pictures the vertical display area is shrinkable with **VPSRED**. The number of omitted lines depends on the vertical decimation factor.

Table 2–17: Number of lines without and with reduction of vertical picture size

Vertical Decimation Factor	Displayed Lines			
	50 Hz		60 Hz	
	Reduction			
	Without	With	Without	With
1	264	214	216	175
...				
6	44	35	36	29

.

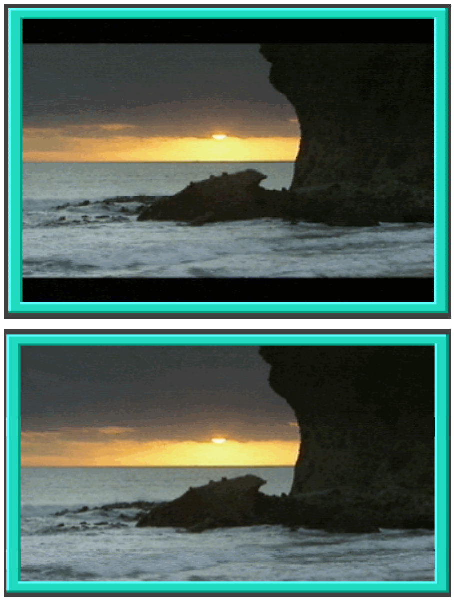

Fig. 2–17: 16:9 Inset Picture without and with Reduction of Vertical Picture Size

2.8.5. Parent Clock Generation

Table 2–18: Format conversion using HZOOM

Display Format	Inset Picture Format	Desired PIP Format	Required Parent Frequency	Value of HZOOM		
				D2	D1	D0
4:3	4:3	4:3	27	0	0	0
4:3	4:3	16:9	20.25	0	0	1
16:9	4:3	4:3	36	0	1	0
16:9	16:9	16:9	36	0	1	0

The phase of the output signals is locked to the rising edge of the horizontal sync pulse. The frequency varies in a certain range to ensure correct aspect ratio for 16:9 applications depending on **HZOOM**. The horizontal and vertical scaling can be used for all display frequencies.

2.8.6. Select Signal

For controlling an external RGB or YUV switch a select signal is supplied. The delay of this signal is programmable for adaptation to different external output signal processing devices (**SELDEL**).

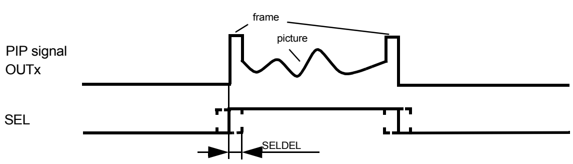

Fig. 2–18: Select Timing

2.8.7. Automatic Brightness Reduction

Displaying a bright PIP picture, the beam current-limitation of the parent system may become active. This may cause the parent picture to be influenced by the inset picture. Therefore a detection circuit reduces the brightness of the inset picture, when the average brightness is above a selectable threshold. After bright picture content has disappeared, the initial brightness reappears. The threshold is adjustable via **ABRTHD** and the speed via **ABRSPD**. Both settings have to be selected for parent system accordingly.

2.9. On Screen Display (OSD)

2.9.1. Display Format

The on screen display allows to insert a block of 5 characters into each of the PIP pictures. The characters are placed in a box (background) whose width is 64 pixels and height is 12 lines. This box is placed in the upper left corner of the PIP picture. 64 different characters are stored in a character ROM. Each character is defined by a pixel matrix consisting of 10 lines and 12 pixels per line. A doubling of the character's height and width is achieved by **CHRDHW**. The OSD starting position is not influenced.

OSD display is also possible if PIP is switched off (DISPMOD ='100011'). Now 3 lines of 20 characters each are displayed at the PIP position.

Fig. 2–19: Example of OSD-only Mode

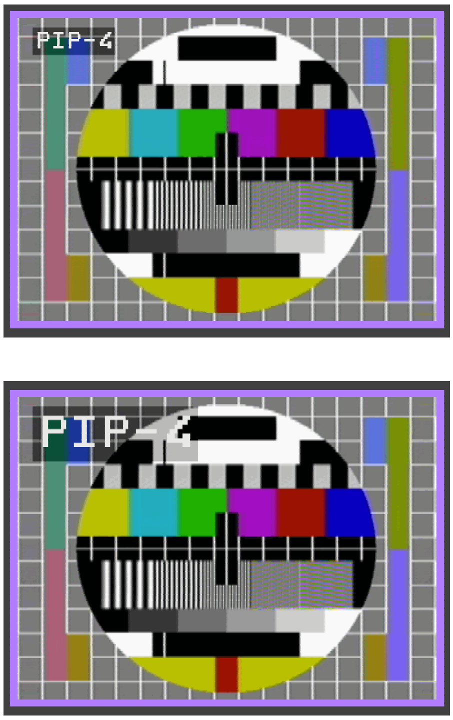

Fig. 2–20: Example of Transparent Mode (Normal and Double Size OSD)

2.9.2. Character Programming

The characters are programmed via I²C bus using a 7 bit code which is identical with the ASCII code except for some of the special characters. The codes are stored in a character RAM consisting of 60 cells. The character codes can be transmitted in two ways: Each character position can be addressed separately by its 7 bit address or the characters can be written consecutively starting at an arbitrarily chosen position. In this case the address is increased automatically. The 7 bit address consists of two parts: The 4 MSBs are used to chose one of the partial pictures and the 3 LSBs to select one of the 5 characters per block.

2.9.3. Character and Character Background Color

The character's color is either same as the frame color (**CHRFRC**) or the character appears with a grey value programmable with **CHRY**.

The character's background box is influenced by **CHRBGON** and **CHRBGY**. It can be made transparent so that behind the characters the inset picture becomes visible. Alternatively the semi-transparent mode can be chosen. At this mode the background box contains the original picture content with reduced luminance value. This mode offers a good trade-off between reduction of visible display area and character readability.

2.10. DA-Conversion and RGB / YUV Switch

SDA 9589x and SDA 9489x include three 7-bit DA-converters. Brightness **BRTADJ**, Contrast **CONADJ** and overall amplitude **PKLR**, **PKLG**, **PKLB** of the output signal are adjustable. External RGB or YUV signals can be connected to the inputs IN1...3. By forcing the FSW input to high-level these signals are switched to the outputs OUT1...3 while the internal signals are switched off. The FSW input signal is passed through to the SEL output. The setting of **RGBINS** determines wether an RGB insertion is possible and which source, the external picture or the PIP, gets priority. See Fig. 2–21.

The external RGB or YUV signals are each clamped to the reference levels of the DACs to force uniform black levels in each channel. The clamping needs careful adjustment especially for VGA applications. The position and the length of the blanking pulse as well as the clamping pulse are adjustable (**CLPPOS, CLPLEN)**. If **READD** is set to '1' (100 Hz mode), all pulses are shortened by one half. **HZOOM** influences the adjustment range of the clamping and blanking pulse because of the modified clock frequency, but the pulse length is kept nearly constant.

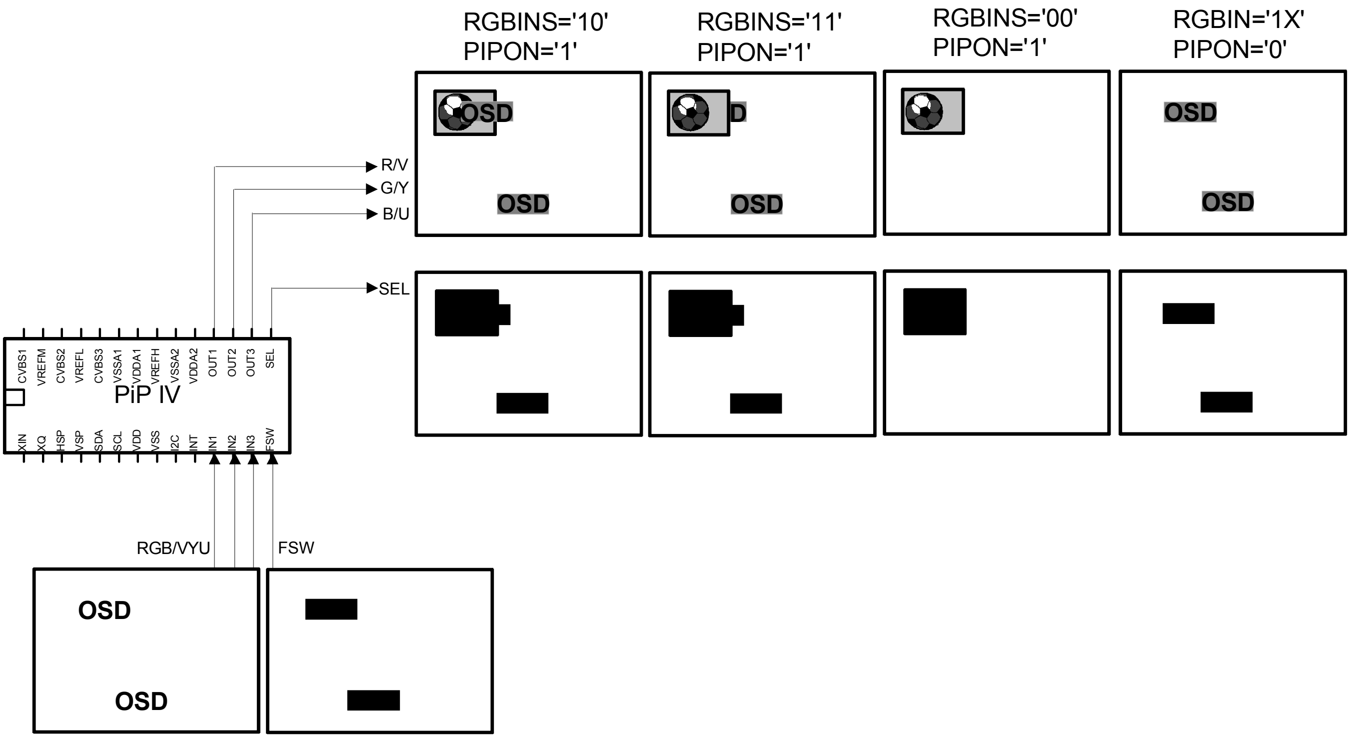

Fig. 2–21: Visualization of RGB/YUV Insertion

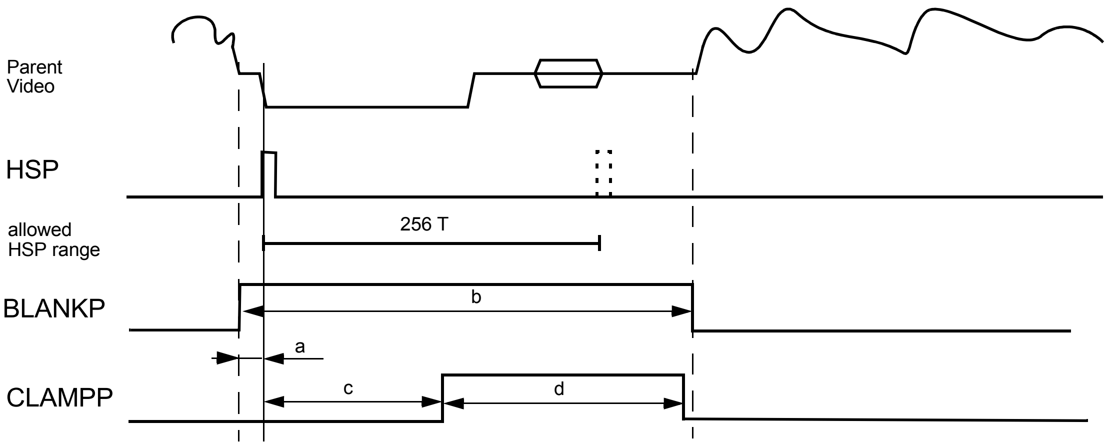

Fig. 2–22: PIP Horizontal Blanking Timing

Table 2–19: PIP horizontal blanking timing

READD	CLPDEL			CLPLEN		a (µs) Blanking Start	b (µs) Blanking Duration	c (µs) Clamping Start	d (µs) Clamping Duration
	D2	D1	D0	D1	D0				
0	0	0	0	0	0	-1.5	10.5	3	5
0	1	1	1	0	0	-11	10.5	-6.4	5
0	0	0	0	0	1	-1.5	7.9	2.2	3.8
0	1	1	1	0	1	-11.0	7.9	-7.3	3.8
1	0	0	0	0	0	-0.8	5.3	1.5	2.5
1	1	1	1	0	0	-5.5	5.3	-3.2	2.5
1	0	0	0	0	1	-0.8	4	1.1	1.9
1	1	1	1	0	1	-5.5	4	-3.6	1.9

2.10.1. Pedestal Level Adjustment

The pedestal level adjustment controlled by I²C signals **BLKLR**, **BLKLG**, **BLKLB** enables the correction of small offset errors, possibly appearing at the successive blanking stage of RGB processor. This adjustment has an effect on the setup level during the active line interval of each channel like the brightness adjustment but has an enhanced resolution of 0.5 LSB. The maximum possible offset amounts to 7.5 LSBs. In YUV mode (**OUTFOR** = '1') the action depends on the setting of **BLKINVR** and **BLKINVB**. If **BLKINVR** (**BLKINVB**) is active the offset applies to the blank level of the **RV** (**BU**) channel during the clamping interval for shifting the setup level to the negative direction. In RGB mode (**OUTFOR** = '0') **BLKINVR** and **BLKINVB** have no effect.

2.10.2. Contrast, Brightness and Peak Level Adjustment

The peak level adjustment modifies the magnitude of each channel separately. It should be used to adapt once the signal levels to the following stage. The contrast adjustment influences all three channels and allows a further increase of 30 % of the peak level magnitude. The effect of the brightness adjustment depends on the selected output mode (RGB/YUV). In YUV mode it changes the offset of the OUT2 (Y) signal only while in RGB mode it changes the offset of all three channels at the same time. The brightness increase is up to 20 %.

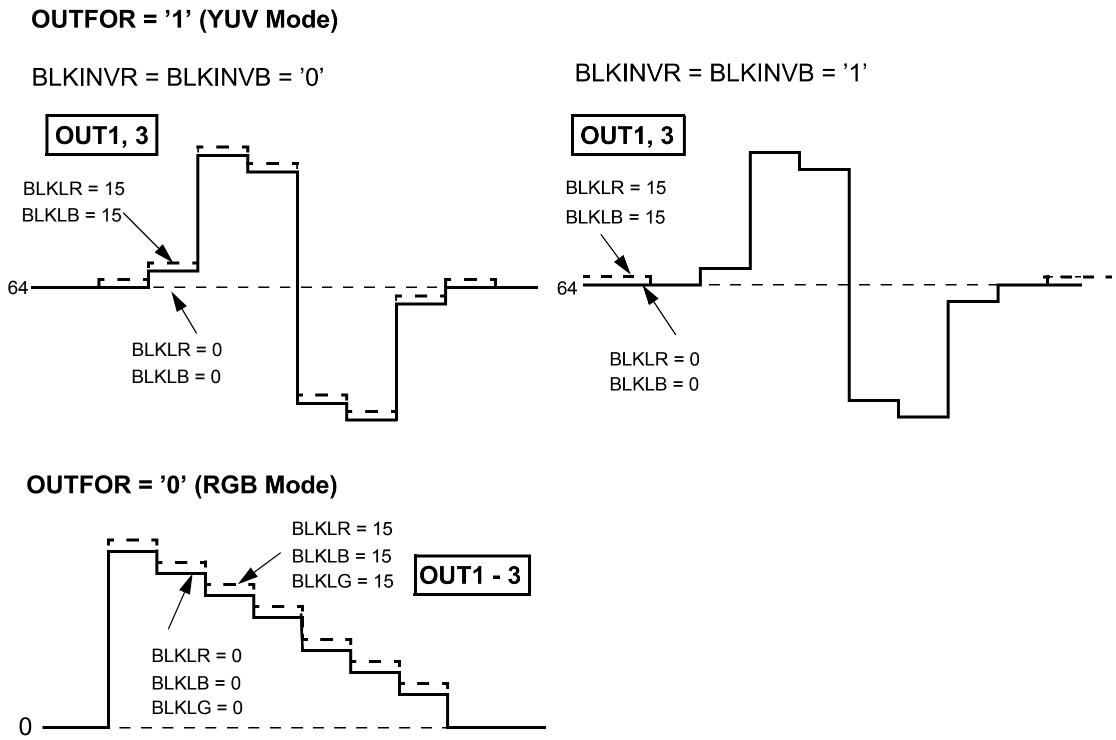

Fig. 2–23: Pedestal Level Adjustment

2.11. Data Slicer

Depending on **SERVICE**, Closed Caption data ("Line 21") or WSS (Wide screen signalling) is sliced by the digital data slicer and can be read out from I²C interface. The line number of the sliced data is selectable with **SELLNR**. Therefore WSS and CC can be processed in different regions (e.g. CC with PAL M). The Closed Caption data is assumed to conform with the ITU standards EIA-608 and EIA-744-A. WSS data is assumed to conform with ETS 300 294 (2nd edition, May 1996).

2.11.1. Closed Caption

The closed caption data stream contains different data services. In field 1 (line 21) the captions CC1 and CC2 and the text pages T1 and T2 are transmitted whereas in field 2 (line 284) caption CC3, CC4, text T3, T4 and the XDS data are transmitted. For more information please refer to the above mentioned standards.

Raw CC as well as pre-filtered data is provided alternatively. With the built-in programmable XDS-Filter (**XDSCLS**), the program-rating information ("V-chip") as well as others can be filtered out. The XDS filter reduce traffic on the I²C bus and save calculation power of the main controller. If no class filter is selected, all incoming data (both fields) is sliced and provided by the I²C interface. When one or more class filters are chosen, only data in field 2 is sliced. Any combination of class filters is allowed. Each "CLASS" is divided into "TYPES" which can be sorted out by the XDS-secondary filter (**XDSTPE**). Any combination of type filter is allowed. Some type filter require an appropriate class filter.

2.11.2. Wide Screen Signalling (WSS)

In WSS mode (**SERVICE**='1') no filtering is possible. All sliced data is passed to the output registers. In this case **XDSTPE** selects the field number of the data to be sliced. In Europe WSS carries for instance information about aspect ratio and movie mode.

2.11.3. Indication Of New Data

The sliced and possibly filtered data is available in **DATAA** and **DATAB**. The corresponding status bits are **DATAV** and **SLFIELD**. When new data were received, **DATAV** becomes '1' and the controller must read **DATAA**, **DATAB** and the status information. After both data bytes were read **DATAV** becomes '0' until new data arrives. It must be ensured that the data polling is activated once per field (16.7 or 20 ms) or every second field (33.3 or 40 ms), depending on the slicer configuration and inset field frequency. The field number of the data in **DATAA** and **DATAB** can be found in **SLFIELD**. If one or more XDS-class filter are activated, **SLFIELD** contains always '1'.

Additionally pin 10 (INT) may flag that new data is received. Default this pin is in tri-state mode to be compatible with the Micronas SDA 9388X/SDA 9389X PIP devices. It can also be configured by **IRQCON** to output a single short pulse when new data is available or behave equal to **DATAV**. In the last case the output remains active until the two data registers **DATAA/ DATAB** are read. Both modes are useful to avoid continuos polling of the I²C bus. The micro-controller initiates I²C transfers only when required.

```
while (1){
  i2c_read pip4_adr, status_reg_adr, status
  if (status & data_valid_mask) {
     i2c_read_inc pip4_adr, dataa_reg_adr, dataa, datab, status
     process_data dataa, datab, status
  }
}
```

Fig. 2–24: Example in Pseudo-code for Reading the Data

2.11.4. Violence Protection

The rating information is sent in the program rating packet of the current (sometimes future) class in the XDS data stream. If only this information is desired the corresponding XDS filter (class 01h, type 05h) should be used to suppress other data. The class/packet bytes (0105h) precede the 2 bytes rating information. Each sequence is closed by the end-of-packet byte (0fh) and a checksum. This checksum complements the byte truncated sum of all bytes to 00h. Except comparison of the received rating with the adjusted user rating threshold the micro-controller should check the parity of each byte and validate the checksum to avoid miss-interpretation of wrong received data.

The SDA 9589x/SDA 9489x offer some alternatives to blocking the PIP channel completely by switching it off (see Fig. 2–25).

The Mosaic mode (**MOSAIC**) hides details of the picture by reduced sharpness and increased aliasing. The picture looks scrambled and is less perceptible.

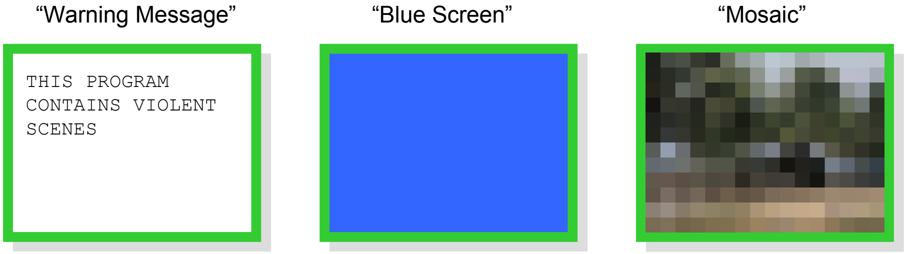

Fig. 2–25: Possibilities of PIP Blocking

2.12. Diagrams

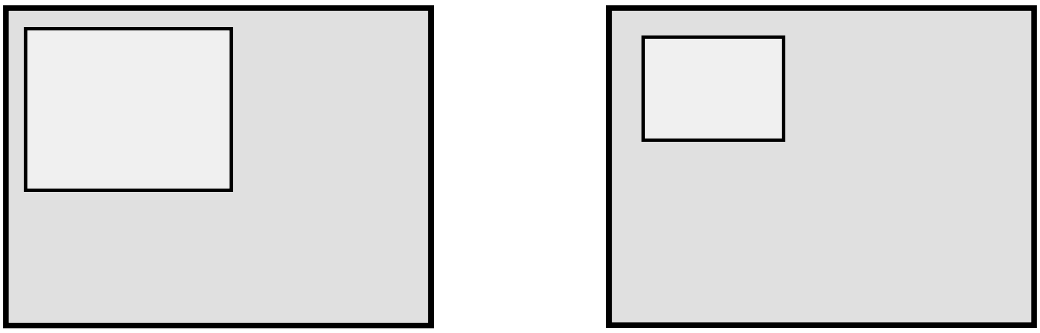

Fig. 2–26: Display Mode 0 with Picture Sizes 1/4 and 1/9

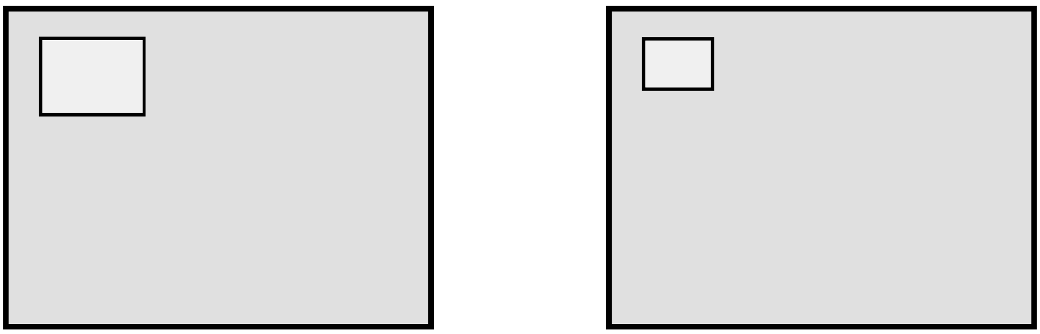

Fig. 2–27: Display Mode 0 with Picture Sizes 1/16 and 1/36

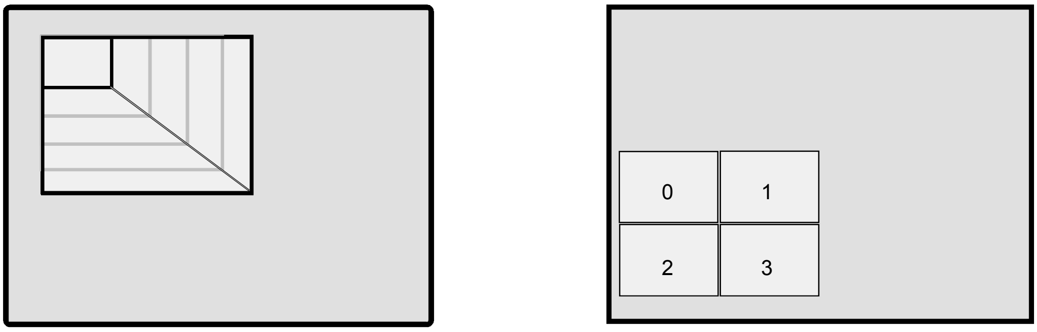

Fig. 2–28: Display Mode 0 (with Scaling) and Display Mode 11

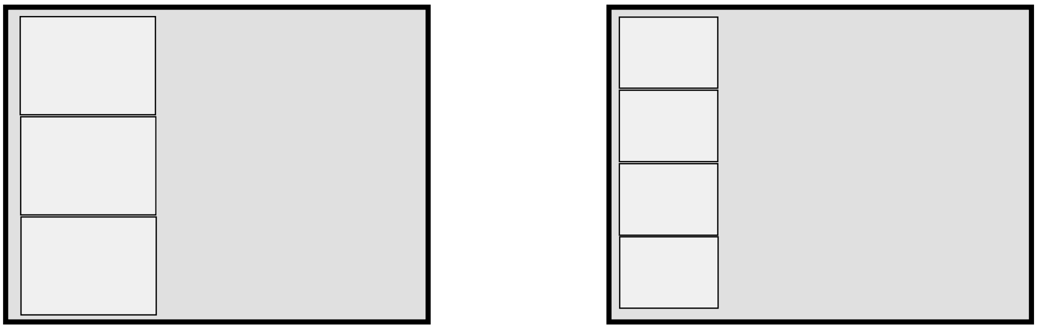

Fig. 2–29: Display Mode 2 and 3 (All Pictures with Same Content)

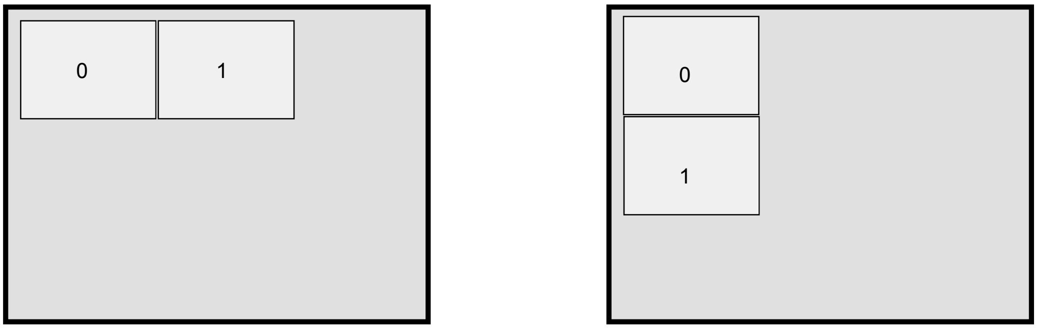

Fig. 2–30: Display Modes 4 and 5

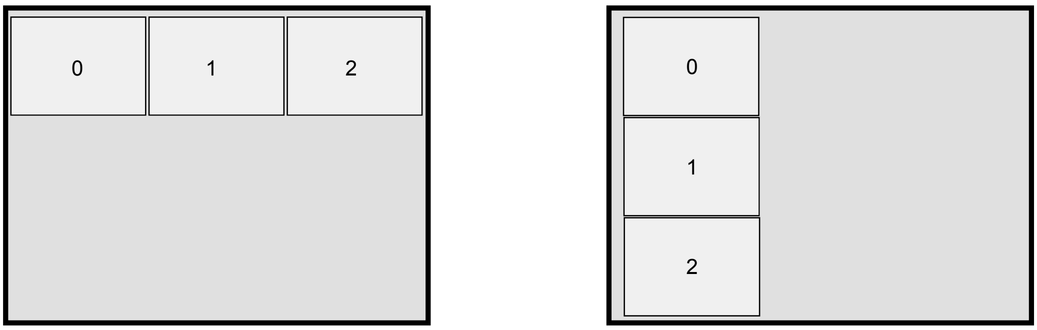

Fig. 2–31: Display Modes 6 and 7

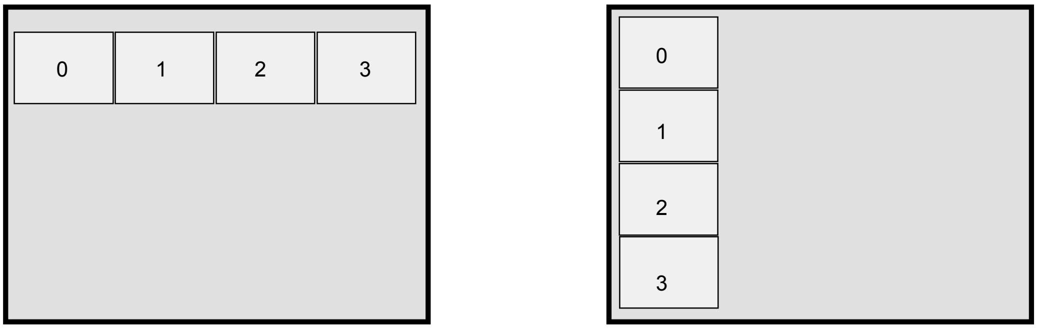

Fig. 2–32: Display Modes 8 and 12

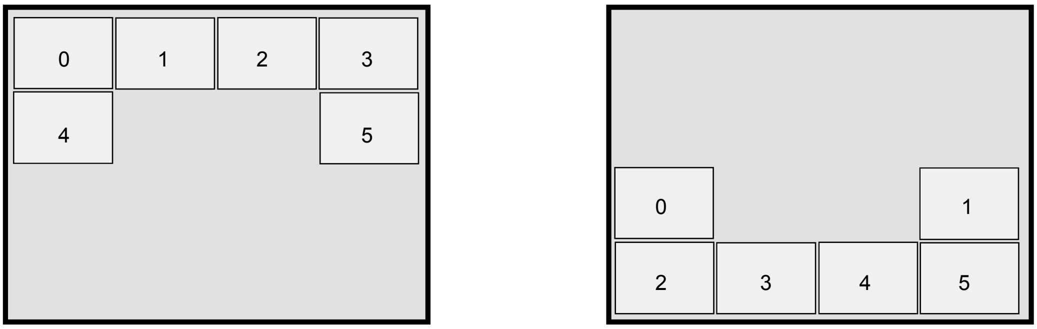

Fig. 2–33: Display Modes 9 and 10

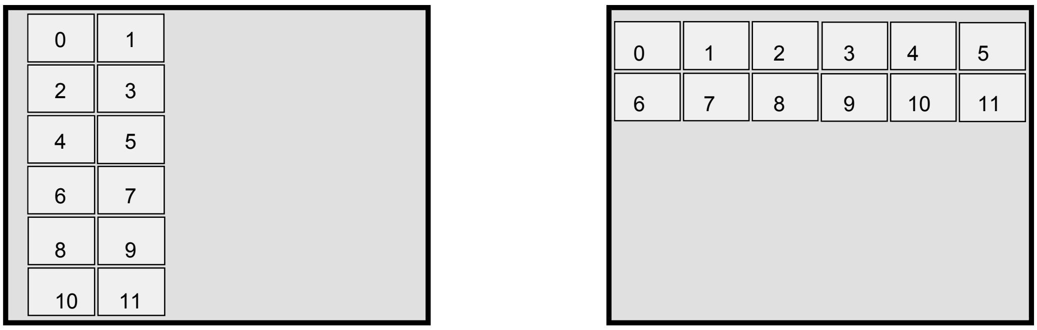

Fig. 2–34: Display Modes 13 and 14

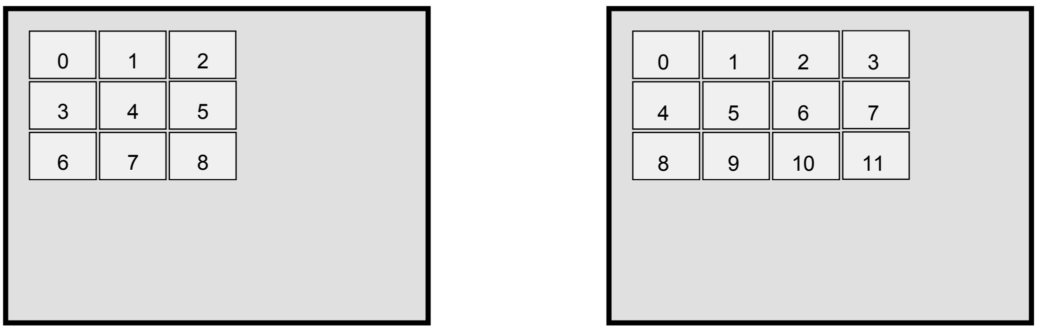

Fig. 2–35: Display Modes 15 and 16

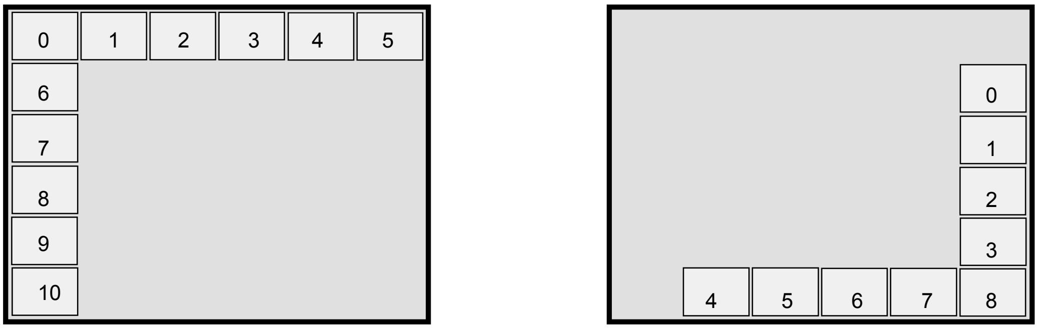

Fig. 2–36: Display Modes 17 and 18

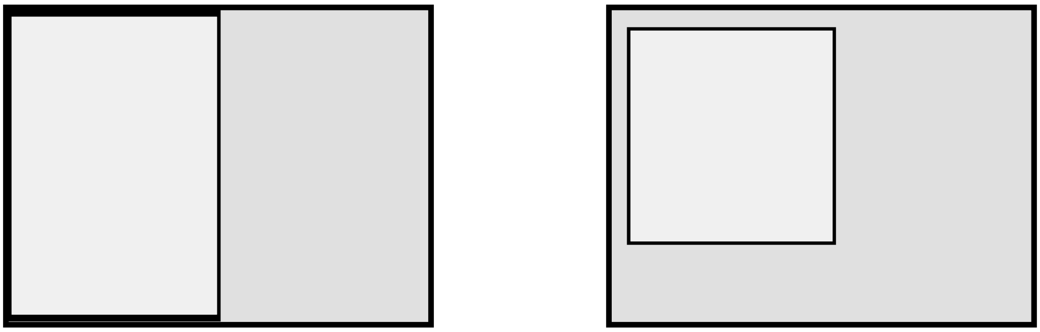

Fig. 2–37: Display Mode 20 (Double Window 1) and 19 (Double Window 1.5)

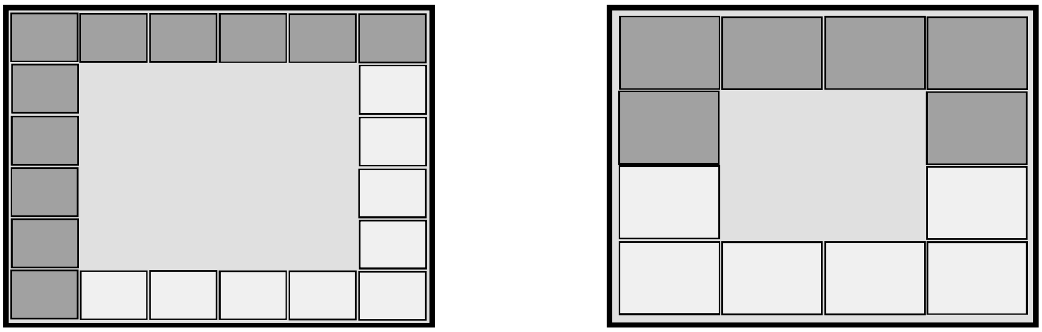

Fig. 2–38: Combination of Display Modes 17/ 18 and 9/ 10 (Dual PIP Application)

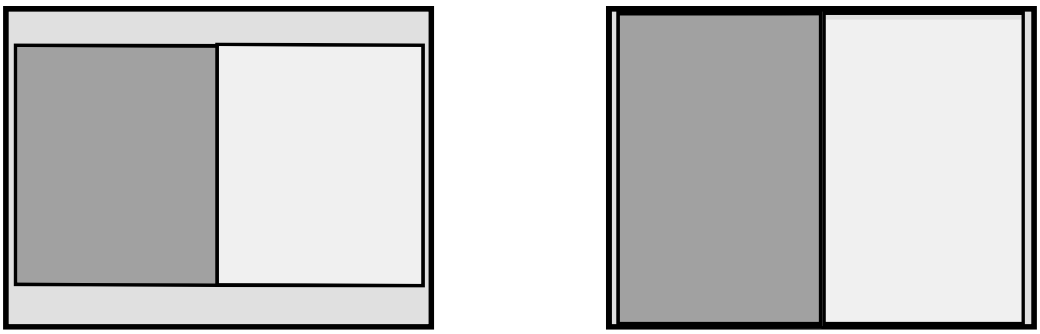

Fig. 2–39: Display Modes 19 and 20 (Dual PIP Application)

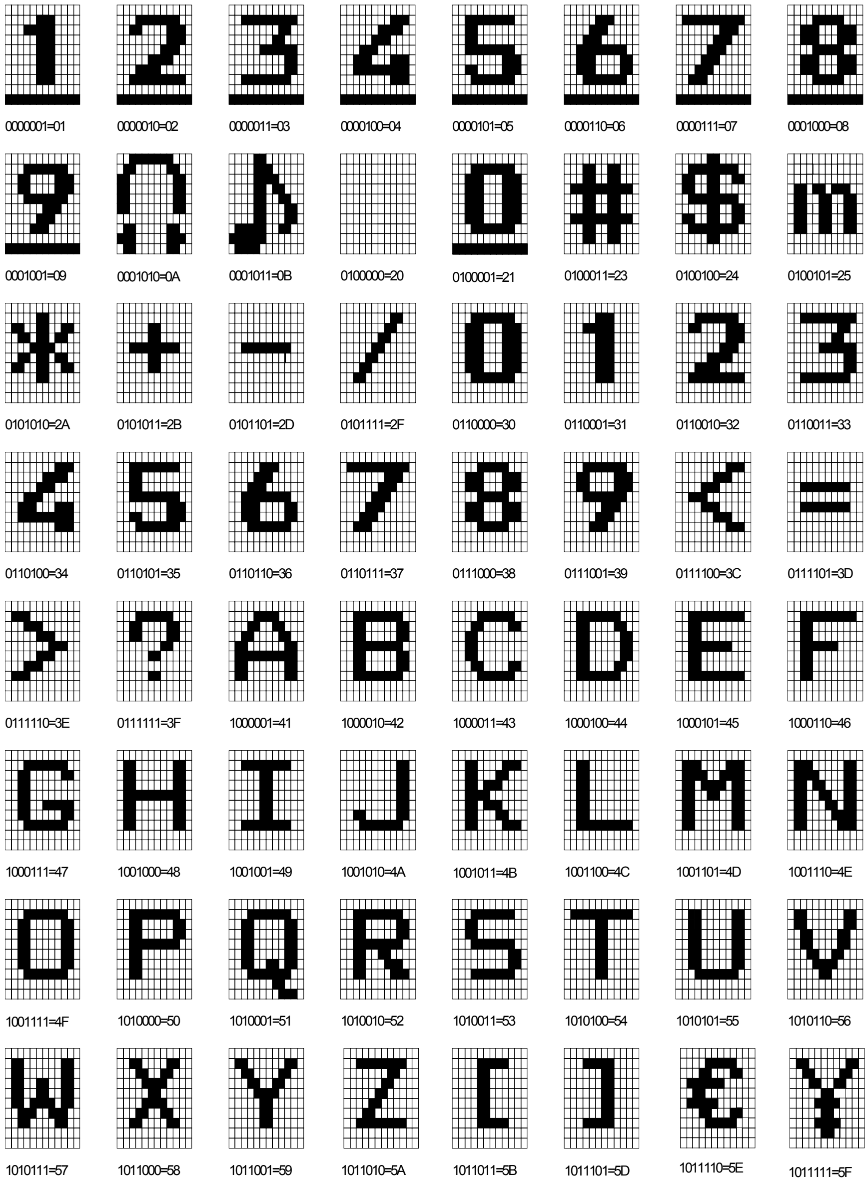

Fig. 2–40: OSD Character Set

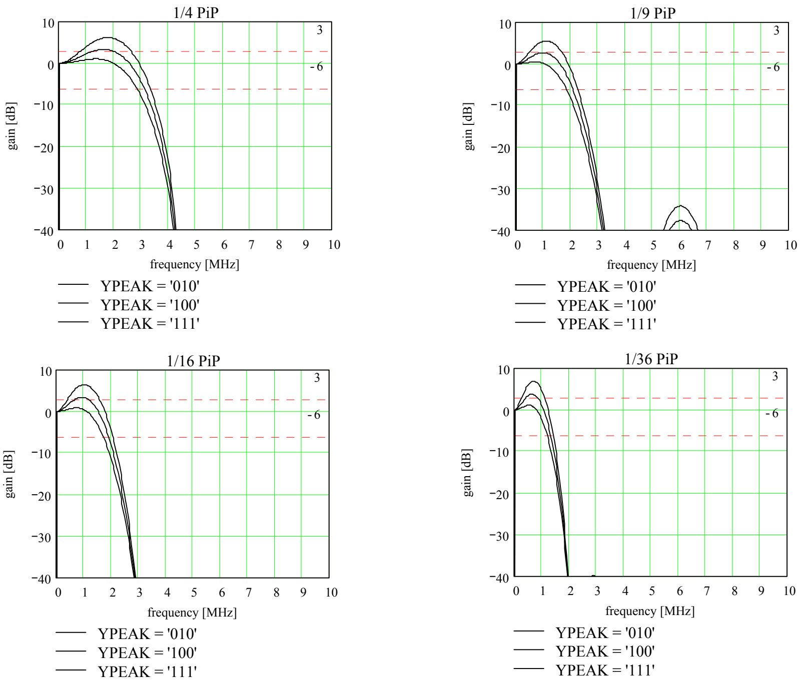

Fig. 2–41: Characteristic (PAL) of Luminance Decimation Filter for Different Peaking Factors

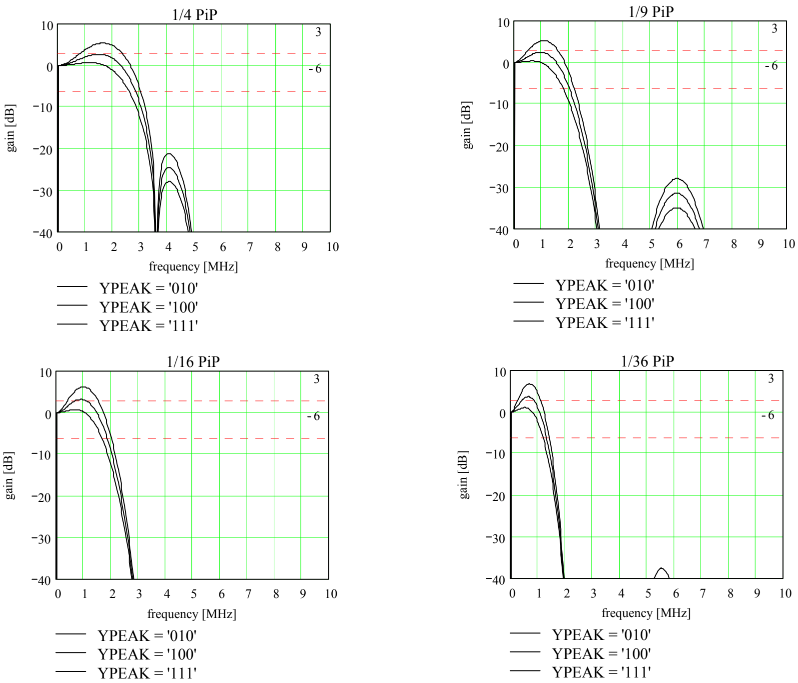

Fig. 2–42: Characteristic (NTSC) of Luminance Decimation Filter for Different Peaking Factors

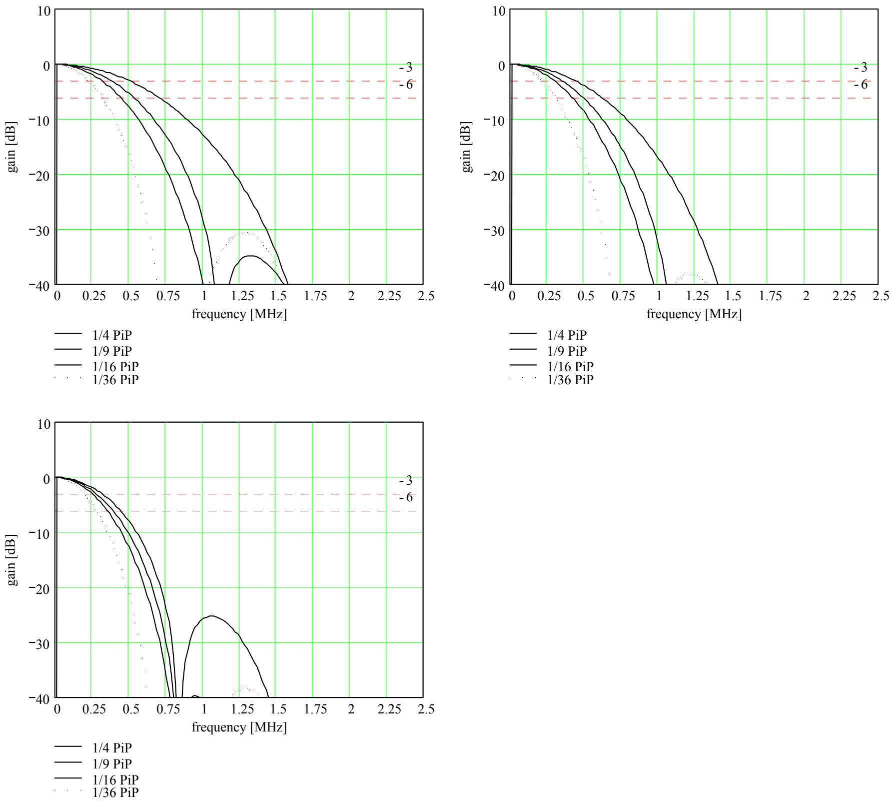

Fig. 2–43: Characteristic of Chrominance Decoder Filter (Small, Medium and Narrow)

3. I²C Bus

3.1. I²C Bus Address

Table 3–1: Primary address (pin 9=’low-level’)

Write Address1	1	1	0	1	0	1	1	0	(D6h)
Read Address1	1	1	0	1	0	1	1	1	(D7h)

Table 3–2: Secondary address (pin 9 = ’high-level’)

Write Address2	1	1	0	1	1	1	1	0	(DEh)
Read Address2	1	1	0	1	1	1	1	1	(DFh)

3.2. I²C Bus Format

Table 3–3: I²C-bus format

WRITE	S	1101x110	A	Subaddress	A	Data Byte		A	****	A	P
READ	S	1101x110	A	Subaddress	A	Sr	1101x111	A	Data Byte n	NA	P
S: Start condition / Sr Repeated start condition / A: Acknowledge / P: Stop condition / NA: No Acknowledge											

Write operation is possible at registers 00h-21h and 2Eh-37h only, read operation is possible at registers 28, 2Ah-2Ch only. An automatic address increment function is implemented.

3.3. I²C Bus Command Table

Table 3–4: I²C bus command table

Subadd (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
00h	PIPON	CPOS1	CPOS0	YUVSEL	READD	PROGEN	FIESEL1	FIESEL0
01h	POSHOR7	POSHOR6	POSHOR5	POSHOR4	POSHOR3	POSHOR2	POSHOR1	POSHOR0
02h	POSVER7	POSVER6	POSVER5	POSVER4	POSVER3	POSVER2	POSVER1	POSVER0
03h	VFP3	VFP2	VFP1	VFP0	HFP3	HFP2	HFP1	HFP0
04h	DISPSTD1	DISPSTD0	FREEZE	MOSAIC	SIZEHOR1	SIZEHOR0	SIZEVER1	SIZEVER0
05h	FPSTD1	FPSTD0	PIPBG1	PIPBG0	FMACTP	HZOOM2	HZOOM1	HZOOM0
06h	HSPINV	VSPINV	VSPNSRQ	VSPDEL4	VSPDEL3	VSPDEL2	VSPDEL1	VSPDEL0
07h	FRSEL	INFRM	VPSRED	FRWIDH2	FRWIDH1	FRWIDH0	FRWIDV1	FRWIDV0
08h	RGBINS1	RGBINS0	VERBLK	SELDOWN	SELDEL3	SELDEL2	SELDEL1	SELDEL0
09h	set to 0	DISPMOD1	DISPMOD0	CLPDEL4	CLPDEL3	CLPDEL2	CLPDEL1	CLPDEL0
0Ah	AGCRES	AGCMD1	AGCMD0	AGCVAL3	AGCVAL2	AGCVAL1	AGCVAL0	NOSIGB
0Bh	CVBSEL1	CVBSEL0	CLMPID1	CLMPID0	BLKVCHYS	BLKCVAL	LMOFST1	LMOFST0
0Ch	PLLITC1	PLLITC0	BLKVCFIL	(reserved)	YCDEL3	YCDEL2	YCDEL1	YCDEL0
0Dh	CSTAND2	CSTAND1	CSTAND0	CSTDEX1	CSTDEX0	(reserved)	CKILL1	CKILL0

Table 3–4: I²C bus command table, continued

Subadd (Hex)	Data Byte							
	D7	D6	D5	D4	D3	D2	D1	D0
0Eh	BGPOS	(reserved)	DEEMP1	DEEMP0	COLON	ACCFIX	CHRBW1	CHRBW0
0Fh	IFCOMP1	IFCOMP0	HUE5	HUE4	HUE3	HUE2	HUE1	HUE0
10h	SATNR	FMACTI	CPLLOF	SCADJ4	SCADJ3	SCADJ2	SCADJ1	SCADJ0
11h	CONADJ3	CONADJ2	CONADJ1	CONADJ0	BLKLR3	BLKLR2	BLKLR1	BLKLR0
12h	BRTADJ3	BRTADJ2	BRTADJ1	BRTADJ0	BLKLG3	BLKLG2	BLKLG1	BLKLG0
13h	TRIOUT	REFINT	BLKINVR	BLKINVB	BLKLB3	BLKLB2	BLKLB1	BLKLB0
14h	PKLR7	PKLR6	PKLR5	PKLR4	PKLR3	PKLR2	PKLR1	PKLR0
15h	PKLG7	PKLG6	PKLG5	PKLG4	PKLG3	PKLG2	PKLG1	PKLG0
16h	PKLB7	PKLB6	PKLB5	PKLB4	PKLB3	PKLB2	PKLB1	PKLB0
17h	MAT1	MAT0	BGY1	BGY0	FRY3	FRY2	FRY1	FRY0
18h	OUTFOR	UVPOLAR	BGU1	BGU0	FRU3	FRU2	FRU1	FRU0
19h	(reserved)	BGFRC	BGV1	BGV0	FRV3	FRV2	FRV1	FRV0
1Ah	SATADJ3†	SATADJ2	SATADJ1	SATADJ0†	YPEAK2	YPEAK1	YPEAK0	YCOR
1Bh	XDSCLS4	XDSCLS3	XDSCLS2	XDSCLS1	XDSCLS0	XDSTPE2	XDSTPE1	XDSTPE0
1Ch	UVSEQ	MPIPBG	SERVICE	SELLNR1	SELLNR0	IRQCON2	IRQCON1	IRQCON0
1Dh	(reserved)	(reserved)	PALIDL2	PALIDL1_1	PALIDL1_0	PIPBLK	(reserved)	PALIDL0
1Eh	POSOFV2	POSOFV1	POSOFV0	POSOFH4	POSOFH3	POSOFH2	POSOFH1	POSOFH0
1Fh	(reserved)	(reserved)	(reserved)	VSHRNK4	VSHRNK3	VSHRNK2	VSHRNK1	VSHRNK0
20h	(reserved)	(reserved)	(reserved)	HSHRNK4	HSHRNK3	HSHRNK2	HSHRNK1	HSHRNK0
21h	(reserved)	(reserved)	(reserved)	(reserved)	DWCOR	PKBOOST	CLPLEN1	CLPLEN0
22h	PIPHLT	ABRTHD3	ABRTHD2	ABRTHD1	ABRTHD0	ABRSPD2	ABRSPD1	ABRSPD0
23h	INFRMOD	DISPMOD6	DISPMOD5	DISPMOD4	DISPMOD3	DISPMOD2	WIPESP1†	WIPESP0
24h	CZMEN	CZMSP1	CZMSP0	(reserved)	WRPOS3	WRPOS2	WRPOS1	WRPOS0
25h	CHRFRC	CHRDHW	CHRY1	CHRY0	CHRBGY1	CHRBGY0	CHRBGON1	CHRBGON0
26h	OSDON	CHRADR6	CHRADR5	CHRADR4	CHRADR3	CHRADR2	CHRADR1	CHRADR0
27h	CHRCLR	CHRCOD6	CHRCOD5	CHRCOD4	CHRCOD3	CHRCOD2	CHRCOD1	CHRCOD0
28h	FRMMD	PIPSTAT	SYNCST1	SYNCST0	CKSTAT	STDET2	STDET1	STDET0
29h	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)
2Ah	DATAA7	DATAA6	DATAA5	DATAA4	DATAA3	DATAA2	DATAA1	DATAA0
2Bh	DATAB7	DATAB6	DATAB5	DATAB4	DATAB3	DATAB2	DATAB1	DATAB0
2Ch	PALDET		DEVICE1	DEVICE0	PRNSTD	PALID	DATAV	SLFIELD
2Dh	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)	(reserved)
2Eh	SCMREL1	SCMREL0	SCMIDL2	SCMIDL1	SCMIDL0	SECDIV		BELLIIR
2Fh	PALINC1	PALINC2	LOCKSP1	LOCKSP0	SECACCL2	SECACCL1	SECACCL0	SECACC
30h	ADLCK	ADLCKSEL	ADLCKCC	CLRANGE1	CLRANGE0	NADJ2	NADJ1	NADJ0

Table 3–4: I²C bus command table, continued

Subadd (Hex)	Data Byte							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
31h	NSRED2	NSRED1	NSRED0	SLLTHD1	SLLTHD0	ISHFT1	ISHFT0	ENLIM
32h	DTECT5060	VTHRL50_6	VTHRL50_5	VTHRL50_4	VTHRL50_3	VTHRL50_2	VTHRL50_1	VTHRL50_0
33h	BCOROFF	VTHRL60_6	VTHRL60_5	VTHRL60_4	VTHRL60_3	VTHRL60_2	VTHRL60_1	VTHRL60_0
34h	VTHRH50_3	VTHRH50_2	VTHRH50_1	VTHRH50_0	VTHRH60_3	VTHRH60_2	VTHRH60_1	VTHRH60_0
35h	CLMSTGY	SLLTHDVP	SLLTHDV2	SLLTHDV1	SLLTHDV0	VFLYWHLM1	VFLYWHLM0	VFLYWHL
36h	FLNSTRD1	FLNSTRD0	CLMPCHRY1	CLMPCHRY0	VDETIFS	VDETITC	VLP1	VLP0
37h	LATENCY1	LATENCY0	FILTBRST	CLMPIST4	CLMPIST3	CLMPIST2	CLMPIST1	CLMPIST0
	= After power on, the grey marked data bits are set to '1', all other to '0'.							

3.4. I²C Bus Command Description

Subaddress 00h

Table 3–5: PIPON

PIPON	**PIP On:** Switches the PIP insertion on
D7	
0	PIP insertion off
1	PIP insertion on

Table 3–6: CPOS

CPOS		**Coarse Position:** Coarse postition of the picture
D6	**D5**	
0	0	Upper left position
0	1	Upper right position
1	0	Lower left position
1	1	Lower right position

Table 3–7: YUVSEL

YUVSEL	**YUV Select:** Selects YUV Mode
D4	
0	CVBS or Y/C source
1	YUV source

Table 3–8: READD

READD	**Read Double Mode:** Double read frequency for compatibility with systems that use 2fH (e.g.100 Hz, progressive)
D3	
0	PIP display with single read frequency and 2x oversampling
1	PIP display with double read frequency

Table 3–9: PROGEN

PROGEN	**Progressive Scan Enable:** For compatibility with progressive scan systems
D2	
0	Each line of PIP is read once (normal operation)
1	Each line of PIP is read twice (line doubling operation)

Table 3–10: FIESEL

FIESEL		**Field Select:** Set field or frame display mode
D1	**D0**	
0	0	Frame mode (if possible)
0	1	Field mode (first field only)
1	0	Field mode (second field only)
1	1	Field mode (one of both)

Subaddress 01h

Table 3–11: POSHOR

POSHOR	**Horizontal Picture Position:** Horizontal position adjustment of the PIP in steps of 4 pixel shift direction depends on the coarse positioning of the picture
D7-D0	

Subaddress 02h

Table 3–12: POSVER

POSVER	**Vertical Picture Position:** Vertical position adjustment of the PIP in steps of 1 lines shift direction depends on the coarse positioning of the picture
D7-D0	

Subaddress 03h

Table 3–13: HFP

HFP				**Horizontal Fine Positioning:** Changes the position of the horizontal acquisition window by steps of 2 pixel	**Note**
D3	**D2**	**D1**	**D0**		
1	0	0	0	-16 pixel (-0.8 μs), most right position of the image	Values refer to the undecimated picture
			..		
0	0	0	0	0 pixel, nominal center position	
			..		
0	1	1	1	+14 pixel (0.7 μs), most left position	

Table 3–14: VFP

VFP				Vertical Fine Positioning: Changes the position of the vertical acquisition window by steps of 1 line	Note
D7	D6	D5	D4		
1	0	0	0	-8 lines, most upper position of the image	values refer to the undecimated picture
			..		
0	0	0	0	0 lines, nominal center position	
			..		
0	1	1	1	+7 lines, most lower position	

Subaddress 04h

Table 3–15: DISPSTD

DISPSTD		Display Standard: Selects the line standard of PIP display
D7	D6	
0	0	PIP depends on detected parent standard (multi-PIP) or inset standard (single-PIP)
0	1	PIP display is always in 625 line mode
1	0	PIP display is always in 525 line mode
1	1	Freeze last detected display standard and size

Table 3–16: FREEZE

FREEZE	Freeze Picture: Interrupts the inset picture writing and displays still picture
D5	
0	Live picture
1	Still picture

Table 3–17: MOSAIC

MOSAIC	**Mosaic Mode:** Hides picture details, intended for use with parental control
D4	
0	Mosaic mode off
1	Mosaic mode on

Table 3–18: SIZEHOR

SIZEHOR		**Horizontal Size:** Horizontal decimation
D3	**D2**	
0	0	Reduction = 2
0	1	Reduction = 3
1	0	Reduction = 4
1	1	Reduction = 6

Table 3–19: SIZEVER

SIZEVER		**Vertical Size:** Vertical decimation
D1	**D0**	
0	0	Reduction = 2
0	1	Reduction = 3
1	0	Reduction = 4
1	1	Reduction = 6

Subaddress 05h

Table 3–20: FPSTD

FPSTD		**Force Parent Standard:** Forces the parent standard to one of the following modes
D7	**D6**	
0	0	Auto-detect parent standard
0	1	50 Hz/625 lines parent standard forced
1	0	60 Hz/525 lines parent standard forced
1	1	Freeze last detected standard

Table 3–21: PIPBG

PIPBG		**PIP Background Display:** Selects the background display
D5	**D4**	
0	0	PIP visible, no background display
0	1	PIP invisible, background display in PIP
1	0	PIP visible, full screen background display
1	1	PIP invisible, background display in PIP and full screen background

Table 3–22: FMACTP

FMACTP	**Frame Mode Activation Parent:** Selects the parent condition for the activation of the frame mode
D3	
0	Frame mode active for standard parent video sources only
1	Frame mode active for some nonstandard sources also

Table 3–23: HZOOM

HZOOM			**Horizontal Zoom:** Selects the parent (display) clock frequency
D2	**D1**	**D0**	
0	0	0	27.34 MHz
0	0	1	20.25 MHz
0	1	0	35.27 MHz
0	1	1	25.43 MHz
1	0	0	26.67 MHz
1	0	1	20.63 MHz
1	1	0	34.17 MHz
1	1	1	28.04 MHz

Subaddress 06h

Table 3–24: HSPINV

HSPINV	**Horizontal Sync Pulse Inversion:** Inverts the polarity of HSP
D7	
0	No inversion, raising edge is sync reference
1	HSP inverted, falling edge is sync reference

Table 3–25: VSPINV

VSPINV	**Vertical Sync Pulse Inversion:** Inverts the polarity of VSP
D6	
0	No inversion, raising edge is sync reference
1	VSP inverted, falling edge is sync reference

Table 3–26: VSPNSRQ

VSPNSRQ D5	**Vertical Sync Pulse Noise Reduction:** Activates automatic V insertion that generates vertical sync pulses in case of missing external VSP
0	On
1	Off

Table 3–27: VSPDEL

VSPDEL					**Vertical Sync Pulse Delay:** Delay of the vertical sync pulse in steps of 128 parent clocks	**Note**
D4	**D3**	**D2**	**D1**	**D0**		
0	0	0	0	0	No delay (0)	Delay depends on HZOOM
				...		
1	1	1	1	1	Maximum delay, 4096 clocks of parent frequency	

Subaddress 07h

Table 3–28: FRSEL

FRSEL D7	**Frame Select:** Selects between the normal frame and the shaded frame
0	Normal frame
1	Shaded frame with 3D impression

Table 3–29: INFRM

INFRM D6	**Inner Frame Activation:** Actives inner frame (4 pixel width, 2 lines height) for multi-PIP display
0	Inner frame off
1	Inner frame on

Table 3–30: VPSRED

VPSRED	Vertical Picture Size Reduction: Reduces vertical picture size to suppress black bars in 16:9 programs
D5	
0	No reduction
1	Reduction on

Table 3–31: FRWIDH

FRWIDH			Frame Width Horizontal: Adjusts the horizontal width of the PIP frame in steps of one pixel
D4	D3	D2	
0	0	0	No horizontal frame
		...	
1	1	1	7 pixel

Table 3–32: FRWIDV

FRWIDV		Frame Width Vertical: Adjusts the vertical width of the PIP frame in steps of one line
D1	D0	
0	0	No vertical frame
	...	
1	1	3 lines

Subaddress 08h

Table 3–33: RGBINS

RGBINS		RGB Insertion: Controls the insertion of external RGB/YUV sources
D7	D6	
0	0	No external insertion possible, FSW input inactive
0	1	External insertion forced (FSW = 1)
1	0	External insertion with FSW possible (priority of FSW input)
1	1	External insertion with FSW possible (priority of PIP)

Table 3–34: VERBLK

VERBLK	**Vertical Blanking:** Switches the vertical blanking mode
D5	
0	Blanking level at DAC outputs only during line-blanking intervals
1	Blanking level at DAC outputs during line-blanking intervals and field-blanking intervals, 16 lines following the parent vertical synchronization pulse are blanked

Table 3–35: SELDOWN

SELDOWN	**Select Down:** Switches the driver type at the output of the SEL pin
D4	
0	Open source output
1	TTL output

Table 3–36: SELDEL

SELDEL				**Select Delay:** Adjusts the delay of select signal
D3	**D2**	**D1**	**D0**	
1	0	0	0	-8 clock periods of display clock
			..	
0	0	0	0	0 clock periods of display clock
			..	
0	1	1	1	+7 clock cycles of display clock

Subaddress 09h

Table 3–37: DISPMOD

DISPMOD		Display Mode: Selects display modes with equal pictures
D6	**D5**	
0	0	Single PIP mode
0	1	3 x1/9 PIP (same content)
1	0	4 x1/16 PIP (same content)
1	1	(Reserved)

Table 3–38: CLPDEL

CLPDEL					Clamping Delay: Delay of the clamping pulse for the external RGB/YUV inputs in steps of 8 parent clock periods
D4	**D3**	**D2**	**D1**	**D0**	
0	0	0	0	0	No delay (0)
				...	
1	1	1	1	1	Maximum delay, 256 clock periods of parent frequency

Subaddress 0Ah

Table 3–39: AGCRES

AGCRES	Automatic Gain Control Reset: Resets AGC
D7	
0	Normal operation
1	Reset of AGC

Table 3–40: AGCMD

AGCMD		AGC Mode: Controls the AGC operation
D6	**D5**	
0	0	Evaluation of sync height and ADC overflow
0	1	Evaluation of sync height only
1	0	Evaluation of ADC overflow only
1	1	AGC fixed (gain depends on AGCVAL)

Table 3–41: AGCVAL

AGCVAL				Automatic Gain Control Value: AGC value for fixed mode (AGCMD=’11’)
D4	**D3**	**D2**	**D1**	
0	0	0	0	Input voltage 0.5 Vpp
			..	
1	0	0	0	Input voltage 1 Vpp
			..	
1	1	1	1	Input voltage 1.5 Vpp

Table 3–42: NOSIGB

NOSIGB	No Signal Behavior: Controls behavior if synchronization is not possible (no source applied)
D0	
0	Noisy picture
1	Colored background

Subaddress 0Bh

Table 3–43: CVBSEL

CVBSEL		CVBS Select: Select CVBS source
D7	**D6**	
0	0	CVBS1
0	1	CVBS2
1	0	Y/C (Y@CVBS2 / C@CVBS3)
1	1	CVBS3

Table 3–44: CLMPID

CLMPID		Clamping Duration: Adjusts duration of clamping pulse for ADC (inset channel)
D5	**D4**	
0	0	0.5 µs
0	1	0.9 µs
1	0	1.2 µs
1	1	1.5 µs

Table 3–45: BLKVCHYS

BLKVCHYS	Blankvalue Hysteresis: Blankvalue generation ... (sync-tip clamping only
D3	
0	Without hysteresis
1	With hysteresis

Table 3–46: BLKVCVAL

BLKVCVAL	Clamping Correction Offset: (Back-porch clamping only)
D2	
0	0
1	-1

Table 3–47: LMOFST

LMOFST		**Luminance Offset:** Modifies black to blank level offset
D1	**D0**	
0	0	No offset
0	1	Offset of 16 LSB
1	0	Offset of -8 LSB
1	1	Offset of -16 LSB

Subaddress 0Ch

Table 3–48: PLLITC

PLLITC		**Inset PLL Time Constant:** Switches the time constant of the inset PLL
D7	**D6**	
0	0	VCR1 (very fast)
0	1	VCR2
1	0	TV1
1	1	TV2 (very slow)

Table 3–49: BLKVCFIL

BLKVCFIL	**Blankvalue Filtering:** (Sync-tip clamping only)
D5	
0	Lowpass filter off
1	Lowpass filter on

Table 3–50: YCDEL

YCDEL				Y/C Delay: Adjusts the delay between luminance and chrominance
D3	D2	D1	D0	
1	0	0	0	-8 pixel (-0.4 µs with respect to undecimated picture)
			..	
0	0	0	0	0 pixel
			..	
0	1	1	1	+7 pixel (0.35 µs)

Subaddress 0Dh

Table 3–51: CSTAND

CSTAND			Color Standard: Forces the desired color standard
D7	D6	D5	
0	0	0	Automatic standard identification
0	0	1	NTSC-M
0	1	0	PAL-N (Argentina)
0	1	1	PAL-M
1	0	0	NTSC44
1	0	1	PAL-B/G/H/I/D
1	1	0	SECAM
1	1	1	PAL60

Table 3–52: CSTDEX

CSTDEX		Color Standard Exclusion: Excludes standards from automatic standard identification
D4	D3	
0	0	Ignore PAL-M / PAL-N
0	1	Ignore SECAM, PAL B/G, PAL60, NTSC4.4
1	0	Ignore PAL-M /PAL-N / NTSC-M
1	1	Ignore PAL-M / PAL-N / NTSC4.4 / PAL60

Table 3–53: CKILL

CKILL		Color Killer Threshold: Damping of color carrier to switch color off	Note
D1	D0		
0	0	-30 dB	Only valid if color killer active (COLON=’0’), Values are approximative
0	1	-18 dB	
1	0	-24 dB	
1	1	Color always off	

Subaddress 0Eh

Table 3–54: BGPOS

BGPOS	Burst Gate Position: Adjusts position of burst gate (SECAM only)
D7	
0	Normal position
1	0.5 µs delayed

Table 3–55: DEEMP

DEEMP		Deemphase Selection: Adjusts SECAM deemphase filter
D5	D4	
0	0	Filter1
0	1	ITU recommendation
1	0	Filter2
1	1	Filter3

Table 3–56: COLON

COLON	Color On: Disable color killer
D3	
0	Color killer active
1	Color forced on

Table 3–57: ACCFIX

ACCFIX	Disable Automatic Chroma Control: Disables the automatic chroma control (ACC)
D2	
0	ACC active
1	ACC fixed (ACC set to nominal value)

Table 3–58: CHRBW

CHRBW		Chroma Bandwidth	
D1	D0	PAL	SECAM
0	0	Wide	Small
0	1	Medium	Medium
1	0	Reserved	
1	1	Small	Wide

Subaddress 0Fh

Table 3–59: IFCOMP

IFCOMP		IF-Compensation Filter: Equalizes the IF-stage characteristic
D7	D6	
0	0	No filtering
0	1	Chroma bandpass active
1	0	IF-compensation bandpass (6 dB/octave)
1	1	Reserved

Table 3–60: HUE

HUE						Hue Control: Phase of color subcarrier for NTSC	Note
D5	**D4**	**D3**	**D2**	**D1**	**D0**		
1	0	0	0	0	0	-44.8 °	Skin color becomes greenish
					..		
0	0	0	0	0	0	0°	
					..		
0	1	1	1	1	1	43.4 °	Skin color becomes redish

Subaddress 10h

Table 3–61: SATNR

SATNR	Satellite Noise Reduction: Stabilizes the horizontal PLL for bad satellite signals („fishes“)
D7	
0	Disabled
1	Enabled

Table 3–62: FMACTI

FMACTI	Frame Mode Activation Inset: Sets the inset condition for the activation of the frame mode
D6	
0	Frame mode only active for standard inset video sources
1	Enhanced frame mode activation range

Table 3–63: CPLLOF

CPLLOF	Chroma PLL Off: Opens loop of chroma PLL (only for test and servicing)
D5	
0	Chroma PLL active
1	Chroma PLL opened (free running oscillator)

Table 3–64: SCADJ

SCADJ					Color Subcarrier Adjustment: Color subcarrier frequency fine adjustment
D4	**D3**	**D2**	**D1**	**D0**	
0	0	0	0	0	Max. negative deviation (-150 ppm)
				...	
0	0	1	1	1	Default (for nominal crystal frequency
				...	
1	1	1	1	1	Max. positive deviation (+310 ppm)

Subaddress 11h

Table 3–65: CONADJ

CONADJ				Contrast Adjustment: Adjusts the contrast of the picture, acts on OUT1-OUT3
D7	**D6**	**D5**	**D4**	
0	0	0	0	Nominal contrast
			..	
1	1	1	1	+30 % contrast increase

Table 3–66: BLKLR

BLKLR				Blanking Level Red: Adjusts the pedestal level of the OUT1 channel in steps of 0.5LSB
D3	**D2**	**D1**	**D0**	
0	0	0	0	No pedestal
			..	
1	1	1	1	+7.5 LSB offset

Subaddress 12h

Table 3–67: BRTADJ

BRTADJ				**Brightness Adjustment:** Adjusts the brightness of the picture, acts on OUT1-OUT3 in RGB mode (YUVFOR = ’0’) and on OUT1 in YUV mode (YUVFOR = ’1’)
D7	**D6**	**D5**	**D4**	
0	0	0	0	Nominal brightness
			..	
1	1	1	1	+20 % brightness increase

Table 3–68: BLKLG

BLKLG				**Blanking Level Green:** Adjusts the pedestal level of the OUT2 channel in steps of 0.5LSB
D3	**D2**	**D1**	**D0**	
0	0	0	0	No pedestal
			..	
1	1	1	1	+7.5 LSB offset

Subaddress 13h

Table 3–69: TRIOUT

TRIOUT	**Tristate Output:** Sets OUT1-OUT3 to tristate mode (high resistance)
D7	
0	Normal operation, outputs are active
1	Pins OUT1-3 are in tri-state mode

Table 3–70: REFINT

REFINT	**Refresh Intervall:** Changes the refresh rate of eDRAM	**Note**
D6		
0	Normal refresh	Keep it at ’0’
1	Fast refresh	

Table 3–71: BLKINVR

BLKINVR	**Blanking Inversion Red:** Inverts the sign of the OUT1 channel offset (BLKLR)
D5	
0	Offset added during the active picture
1	Offset added during blanking

Table 3–72: BLKINVB

BLKINVB	**Blanking Inversion Blue:** Inverts the sign of the OUT3 channel offset (BLKLB)
D4	
0	Offset added during the active picture
1	Offset added during blanking

Table 3–73: BLKLB

BLKLB				**Blanking Level Blue:** Adjusts the pedestal level of the OUT3 channel in steps of 0.5LSB
D3	**D2**	**D1**	**D0**	
0	0	0	0	No pedestal
			..	
1	1	1	1	+7.5 LSB offset

Subaddress 14h

Table 3–74: PKLR

PKLR								**Peak Level Red:** Peak to peak output voltage of the OUT1 channel	**Note**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0	0	0	0	0	0.3 V_{pp}	Values refer to contrast (CONADJ) and brightness (BRTADJ) at minimum
							...		
1	1	0	0	0	0	0	0	1 V_{pp}	
							...		
1	1	1	1	1	1	1	1	1.2 V_{pp}	

Subaddress 15h

Table 3–75: PKLG

PKLG								**Peak Level Green:** Peak to peak output voltage of the OUT2 channel	**Note**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0	0	0	0	0	0.3 V_{pp}	Values refer to contrast (CONADJ) and brightness (BRTADJ) at minimum
							...		
1	1	0	0	0	0	0	0	1 V_{pp}	
							...		
1	1	1	1	1	1	1	1	1.2 V_{pp}	

Subaddress 16h

Table 3–76: PKLB

PKLB								**Peak Level Blue:** Peak to peak output voltage of the OUT2 channel	**Note**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0	0	0	0	0	0.3 V_{pp}	Values refer to contrast (CON-ADJ) and bright-ness (BRTADJ) at minimum
							...		
1	1	0	0	0	0	0	0	1 V_{pp}	
							...		
1	1	1	1	1	1	1	1	1.2 V_{pp}	

Subaddress 17h

Table 3–77: MAT

MAT		**RGB Matrix Select:** Selects the RGB matrix coefficients for YUV to RGB conversion
D7	**D6**	
0	0	EBU- Matrix
0	1	NTSC-Japan Matrix
1	0	NTSC-USA Matrix
1	1	(Reserved)

Table 3–78: BGY

BGY	**Background Color Y:** Adjusts the Y background color component the values gives the two MSBs of the Y background signal
D5-D4	

Table 3–79: FRY

FRY	**Frame Color Y:** Adjusts the Y frame color component the value gives the 4 MSBs of the Y frame signal
D3-D0	

Subaddress 18h

Table 3–80: OUTFOR

OUTFOR	**Output Format:** Switches between RGB output and YUV output
D7	
0	RGB output signals, matrix active
1	YUV output signals

Table 3–81: UVPOLAR

UVPOLAR	**UV Polarity:** Switches between UV or inverted UV output, has no influence in RGB mode
D6	
0	+U / +V output
1	-U / -V output

Table 3–82: BGU

BGU	**Background Color U:** Adjusts the U background color component the values gives the two MSBs of the U background signal
D5-D4	

Table 3–83: FRU

FRU	**Frame Color U:** Adjusts the U frame color component the value gives the 4 MSBs of the U frame signal
D3-D0	

Subaddress 19h

Table 3–84: BGFRC

BGFRC	**Background Frame Color:** Selects background color table or frame color table for background color
D6	
0	Background color according to BGY, BGU, BGV
1	Background color according to FRY, FRU, FRV

Table 3–85: BGV

BGV	**Background Color V:** Adjusts the V background color component the values gives the two MSBs of the V background signal
D5-D4	

Table 3–86: FRV

FRV	**Frame Color V:** Adjusts the V frame color component the value gives the 4 MSBs of the V frame signal
D3-D0	

Subaddress 1Ah

Table 3–87: SATADJ

SATADJ				**Color Saturation Adjustment:** Adjusts the color saturation in steps of x/8
D7	**D6**	**D5**	**D4**	
0	0	0	0	No color
			..	
1	0	0	0	Nominal saturation
			..	
1	1	1	1	1.875 times saturation

Table 3–88: YPEAK

YPEAK			**Y Peaking Adjustment:** Adjusts luminance peaking
D3	**D2**	**D1**	
0	0	0	No peaking
0	1	1	Recommended value
1	1	1	Strongest peaking

Table 3–89: YCOR

YCOR D0	**Y Coring Enable:** Suppresses noise introduced by peaking
0	Coring off
1	1 LSB coring

Subaddress 1Bh

Table 3–90: XDSCLS

XDSCLS					**XDS Class Select:** Closed Caption XDS-Primary Filter (Class)
D7	**D6**	**D5**	**D4**	**D3**	
0	0	0	0	0	Transparent, no filtering
1	X	X	X	X	“Current” class selected
X	1	X	X	X	“Future” class selected
X	X	1	X	X	“Channel” class selected
X	X	X	1	X	“Miscellaneous” class selected
X	X	X	X	1	“Public Services” class selected

Table 3–91: XDSTPE

XDSTPE			XDS Type Select/WSS Field Select			
D2	**D1**	**D0**	**XDS-Secondary Filter Type**	**Meaning**	**WSS field**	**Note**
0	0	0	All	No filtering	0	Behavior of these bits depends on selected data-service
0	0	1	05h	Program rating	1	
0	1	0	01h, 04h	Time information only	0/1	
0	1	1	40h	Out of band only	0/1	
1	0	0	01h, 02h, 03h, 04h, 0Dh, 40h	VCR information	0/1	
1	0	1	01h, 04h, 05h	Time information and program rating	0/1	
1	1	0	05h, 40h	Out of band and program rating	0/1	
1	1	1	01h, 02h, 03h, 04h, 05h, 0Dh, 40h	VCR information and program rating	0/1	

Subaddress 1Ch

Table 3–92: UVSEQ

UVSEQ	UV Sequence: Changes the UV multiplex sequence	Note
D7		
0	U and V are correct	Valid only if **YUVSEL**='1'
1	U and V are exchanged	

Table 3–93: MPIPBG

MPIPBG	Multi-PIP Background: Selects the background color for multi-PIP mode
D6	
0	Black
1	Same as background color

Table 3–94: SERVICE

SERVICE	Data Service Select: Selects data service for slicing
D5	
0	Closed Caption
1	Widescreen Signalling (WSS)

Table 3–95: SELLNR

SELLNR		Select Line Number: Line number of data service field 0 (field1)	Note
D4	D3		
0	0	[NTSC] 20 (283), [PAL M] 17 (280)	WSS
0	1	[NTSC] 21 (284), [PAL M] 18 (281)	Closed Caption
1	0	[PAL B/G] 22 (329)	Closed Caption
1	1	[PAL B/G] 23 (330)	WSS

Table 3–96: IRQCON

IRQCON			Interrupt Request Pin Configuration: Output of INT pin	Note
D2	D1	D0		
0	0	0	Tri-state (high-Z)	
0	0	1	Interrupt, when new data received (neg. polarity)	Pulse length is approximately 2 µs
0	1	0	Interrupt, when new data received (pos. polarity)	
0	1	1	Equivalent to DATAV for both registers (neg. polarity)	
1	0	0	Equivalent to DATAV for both registers (pos. polarity)	
1	0	1	Inset V-pulse (neg. polarity)	Pulse length is 50 ns
1	1	0	Inset field	High = first field, low = second field,
1	1	1	Inset clamping pulse (neg. polarity)	Only for test purpuse

Subaddress 1D

Table 3–97: PALIDL2

PALIDL2	PAL/NTSC Identifikation level 2 : Sensitivity of identification of PAL/NTSC signals
D5	
0	1/2 or 1/4
1	1/8 or 1/16

Table 3–98: PALIDL1

PALIDL1		PAL/NTSC Identifikation level 1: Sensitivity of identification of PAL/NTSC signals
D4	D3	
0	0	+ 0
0	1	+ 32
1	0	+ 64
1	1	+ 128

Table 3–99: PIPBLK

PIPBLK	**PIP Blank:** Blanks the current picture by setting it to background color
D2	
0	No blank
1	Blanks the current selected (**WRPOS**) PIP

Table 3–100: PALIDL

PALIDL	**PAL ID Level:** Sensitivity of identification of PAL/NTSC signals
D0	
0	High rejection of PAL/NTSC
1	Low rejection of PAL/NTSC

Subaddress 1Eh

Table 3–101: POSOFV

POSOFV			**Position Offset Vertical:** Vertical position offset in steps of 4 lines
D7	**D6**	**D5**	
1	0	0	-16 lines
		...	
0	0	0	0 lines
		...	
0	1	1	+12 lines

Table 3–102: POSQFH

POSOFH					Position Offset Horizontal: Horizontal position offset in steps of 16 pixel
D4	D3	D2	D1	D0	
1	0	0	0	0	-256 pixel
				...	
0	0	0	0	0	0 pixel
				...	
0	1	1	1	1	+240 pixel

Subaddress 1Fh

Table 3–103: VSHRNK

VSHRNK					Vertical Shrink: Changes the vertical size in steps of 2 lines	Note
D4	D3	D2	D1	D0		
0	0	0	0	0	No shrink, picture size according to SIZEVER	Max. usable value depends on SIZEVER
				...		
1	1	1	1	1	Max. possible shrink	

Subaddress 20h

Table 3–104: HSHRNK

HSHRNK					Horizontal Shrink: Changes the horzontal size in steps of 4 pixel	Note
D4	D3	D2	D1	D0		
0	0	0	0	0	No shrink, picture size according to SIZEHOR	Max. usable value depends on SIZEVER
				...		
1	1	1	1	1	Max. possible shrink	

Subaddress 21h

Table 3–105: DWCOR

DWCOR D3	Test Only
0	(Reserved)
1	Normal operation

Table 3–106: PKBOOST

PKBOOST D2	**Peaking Boost:** Influences peaking of *YPEAK* (A2h)
0	Use normal peaking values
1	Double peaking values

Table 3–107: CLPLEN

CLPLEN		Clamping Pulse Length		
D1	**D0**	**Clamping Pulse Length**	**Blanking Duration**	**Note**
0	0	5 μs	10.5 μs	The clamping pulse length and the blanking is also influenced by the setting of READD and HZOOM
0	1	3.75 μs	7.9 μs	
1	0	2.5 μs	5.2 μs	
1	1	1.25 μs	2.6 μs	

Subaddress 22h

Table 3–108: PIPHLT

PIPHLT D7	**PIP Highlighting:** Highlights the current selected (WRPOS) PIPr
0	No highlighting
1	Highlighting the PIP

Table 3–109: ABRTHD

ABRTHD				**Automatic Brightness Reduction Threshold:** Threshold adjustment for reduction of luminance magnitude
D6	**D5**	**D4**	**D3**	
0	0	0	0	ABR off
0	0	0	1	ABR threshold at luminance value of 240
			..	
1	1	1	1	ABR threshold at luminance value of 180

Table 3–110: ABRSPD

ABRSPD			**Automatic Brightness Reduction Speed:** Speed adjustment for reduction of luminance magnitude
D2	**D1**	**D0**	
0	0	0	2 fields
		...	
1	1	1	16 fields

Subaddress 23h

Table 3–111: INFRMOD

INFRMOD	**Inner Frame Modification:** Modifies the look of the frame for dual-PIP applications
D7	
0	Inner frame suited for usage of single SDA 9589x/SDA 9489x applications
1	Inner frame suited for usage of dual SDA 9589x/SDA 9489x applications

Table 3–112: DISPMOD

DISPMOD					**Display Mode:** Selects the single PIP modes, Multi-PIP modes or Double-Window mode	**Note**
D6	**D5**	**D4**	**D3**	**D2**		
0	0	0	0	0	Single PIP mode	See Table 2–9 on page 15 for description of modes
				...		
1		0	1	0	OSD only mode	

Table 3–113: WIPESP

WIPESP		**Wipe Speed:** Selects the period for opening/closing the PIP window
D1	**D0**	
0	0	Wipe off
0	1	1/3 second
1	0	2/3 second
1	1	1 second

Subaddress 24h

Table 3–114: CZMEN

CZMEN	**Continuos Zoom Enable:** Controls the update of the picture size
D7	
0	Delayed execution of **HDEC/VDEC/HSHRNK/VSHRNK** update
1	Picture size will be updated

Table 3–115: CZMSP

CZMSP		**Continuos Zoom Speed:** Speed setting for continous zooming	**Note**
D6	**D5**		
0	0	No zoom	1 step means 20 pixel and 8 lines (PAL) or 6 lines (NTSC) decrement or increment
0	1	1 step per 1 fields	
1	0	1 step per 2 fields	
1	1	1 step per 4 fields	

Table 3–116: WRPOS

WRPOS				Write Position: Position of the current written picture	Note
D3	**D2**	**D1**	**D0**		
0	0	0	0	First writing position = first picture	Number of last valid writing position depends on display mode (**DISPMOD**)
0	0	0	1	Second writing position	
			..		
1	0	0	1	Maximum writing position	

Subaddress 25h

Table 3–117: CHRFRC

CHRFRC	**Character Frame Color:** Modifies the character color
D7	
0	Character luminance table used
1	Frame color table used

Table 3–118: CHRDHW

CHRDHW	**Character Double Height and Width:** Doubles the characters' height and width
D6	
0	Normal height and width
1	Double height and width

Table 3–119: CHRY

CHRY		**Character Luminance:** Character luminance level (IRE)	Note
D5	**D4**		
0	0	60	Valid only if CHRFRC = '0', character chrominance is 0 IRE
0	1	70	
1	0	80	
1	1	90	

Table 3–120: CHRBGY

CHRBGY		Character Background Luminance: Character background luminance level (IRE)
D3	D2	
0	0	10
0	1	20
1	0	30
1	1	40

Table 3–121: CHRBGON

CHRBGON		Character Background On: Defines the characters' background	Note
D1	D0		
0	0	No character background (transparent mode)	
0	1	Character background (dependent on CHRBGY)	
1	0	Semi-transparent mode (black&white)	Not possible in case of active background in PIP
1	1	Semi-transparent mode (colored)	

Subaddress 26h

Table 3–122: OSDON

OSDON	OSD On: Switches OSD on
D7	
0	OSD off
1	OSD on

Table 3–123: CHRADR

CHRADR							Character Address		
D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**No. Picture**	**No. Character**	**Note**
0	0	0	0	0	0	0	0	0	Will be auto-incremented with every write access to CHR-COD
0	0	0	0	0	0	1	0	1	
						...	...	...	
0	0	0	0	1	0	0	0	4	
0	0	0	1	0	0	1	1	1	
						...	...	...	
1	0	1	1	1	0	0	11	4	

Subaddress 27h

Table 3–124: CHRCLR

CHRCLR	Character Clear: Resets all characters to 'blank' character
D7	
0	No blank
1	Character reset

Table 3–125: CHRCOD

CHRCOD	Character Code: Character code, see Appendix
D6-D0	

Subaddress 28h

Table 3–126: FRMMD

FRMMD	**Frame Mode Indication:** PIP displays field or frame mode
D7	
0	Field mode, one field is repeated twice
1	Frame mode, both fields are displayed

Table 3–127: PIPSTAT

PIPSTAT	**PIP Status:** Indication of visibility of PIP, corresponds to PIPON
D6	
0	PIP off
1	PIP on

Table 3–128: SYSNCST

SYNCST		**Inset Synchronization Status:** Inset synchronization PLL is
D5	**D4**	
0	0	Not locked to CVBS signal
0	1	
1	0	Locked to CVBS signal (60 Hz)
1	1	Locked to CVBS signal (50 Hz)

Table 3–129: CKSTAT

CKSTAT	**Color Killer Status:** Chroma
D3	
0	Chroma: Off
1	Chroma: On

Table 3–130: STDET

STDET			**Standard Detection:** Detected color standard
D2	**D1**	**D0**	
0	0	0	Non-standard or standard not detected
0	0	1	NTSC-M
0	1	0	PAL-M
0	1	1	NTSC44
1	0	0	PAL60
1	0	1	PAL-N
1	1	0	SECAM
1	1	1	PAL-B/G

Subaddress 2Ah

Table 3–131: DATAA

DATAA	**First Data Byte:** First word of sliced data, D7 = MSB, D0 = LSB
D7-D0	

Subaddress 2Bh

Table 3–132: DATAB

DATAB	**Second Data Byte:** Second word of sliced data, D7 = MSB, D0 = LSB
D7-D0	

Subaddress 2Ch

Table 3–133: PALDET

PALDET	**PAL identification:** PAL identifikation (algorithm B)
D7	
0	Not PAL
1	PAL

Table 3–134: DEVICE

DEVICE		**Device Identification:** Micronas PIP IC
D5	**D4**	
0	0	SDA 9488X (PIP IV Basic)
0	1	SDA 9489X (PIP IV Advanced)
1	0	SDA 9588X (OCTOPUS)
1	1	SDA 9589X (SOPHISTICUS)

Table 3–135: PRNSTD

PRNSTD	**Parent Standard Detection:** Status of parent (display) standard detection
D3	
0	60 Hz field frequency detected
1	50 Hz field frequency detected

Table 3–136: PALID

PALID	**PAL Identification:** Identification of PAL signal (algorithm A)	**Note**
D2		
0	NTSC signal	Not valid if STDET= '000'
1	PAL signal	

Table 3–137: DATAV

DATAV	**Data Valid:** New data indication, used for data flow control (polling mode)
D1	
0	Data read via I²C or no data available
1	New data received and available in DATAA and DATAB

Table 3–138: SLFIELD

SLFIELD	**Sliced Data Field Number:** DATAA and DATAB
D0	
0	DATAA and DATAB are from: First field
1	DATAA and DATAB are from: Second field

Subaddress 2Eh

Table 3–139: SCMREL

SCMREL		**Secam Rejection Level**
D7	**D6**	
0	0	320
0	1	384
1	0	352
1	1	1024

Table 3–140: SCMIDL

SCMIDL			SECAM Identification Level
D5	D4	D3	
0	0	0	128
0	0	1	64
0	1	0	96
0	1	1	80
1	0	0	70
1	0	1	76
1	1	0	84
1	1	1	90

Table 3–141: SCCDIV

SCCDIV	Secam Divider
D2	
0	Divide by 4
1	Divide by 2

Table 3–142: BELLIIR

BELLIIR	Bellfilter Adjustment
D0	
0	17/64
1	12/64

Subaddress 2Fh

Table 3–143: PALINC1

PALINC1	**PAL Increment 1:** PAL/NTSC identification
D7	
0	+3
1	+2

Table 3–144: PALINC2

PALINC2	**PAL Increment 2:** PAL/NTSC identification
D6	
0	-1
1	-2

Table 3–145: LOCKSP

LOCKSP		**Locking Speed:** Duration Of Chroma PLL Search
D5	**D4**	
0	0	25 fields
0	1	20 fields
1	0	17 fields
1	1	15 fields

Table 3–146: SECACCL

SECACCL			Secam Acceptance Level
D3	D2	D1	
0	0	0	100
0	0	1	84
0	1	0	64
0	1	1	32
1	0	0	70
1	0	1	76
1	1	0	90
1	1	1	(Reserved)

Table 3–147: SECACC

SECACC	Secam Acceptance
D0	
0	Disabled
1	Enabled

Subaddress 30h

Table 3–148: ADLCK

ADLCK	Additional Lock-detection
D7	
0	Do not use lock signal
1	Use lock-signal

Table 3–149: ADLCKSEL

ADLCKSEL	Additional Lock-detection Selection
D6	
0	PALID
1	PALDET

Table 3–150: ADLCKCCI

ADLCKCC	Additional Lock-detection Color-killer
D5	
0	Do not use lock signal
1	Use lock-signal

Table 3–151: CLRANGE

CLRANGE		Chroma Lock-range
D4	D3	
0	0	± 425 Hz
0	1	± 463 Hz
1	0	± 505 Hz
1	1	± 550 Hz

Table 3–152: NADJ

NADJ			**Notch Adjustment:** Color-carrier notch adjustment
D2	D1	D0	
0	0	0	Broadest notch
...			
1	1	1	Steepest notch

Subaddress 31h

Table 3–153: NSRED

NSRED			Noise Reduction for Horizontal PLL
D7	D6	D5	
0	0	0	1/16
0	0	1	1/8
0	1	0	1/4
0	1	1	1/2
1	0	0	1
1	0	1	2
1	1	0	4
1	1	1	8

Table 3–154: SLLTHD

SLLTHD		Slicing Level Threshold H
D4	D3	
0	0	No offset
0	1	Adaptive negative (limited to ± 4)
1	0	Adaptive positive (limited to ± 4)
1	1	Adaptive positive (limited to ± 8)

Table 3–155: ISHFT

ISHFT		I-Adjustment for Horizontal PLL
D2	D1	
0	0	*1
0	1	*2
1	0	*4
1	1	*8

Table 3–156: ENLIM

ENLIM D0	Enable Limiter
0	Disabled
1	Enabled

Subaddress 32h

Table 3–157: DETECT5060

DETECT5060 D7	Detection of 50 and 60 Hz Signals
0	Immediately
1	Delayed

Table 3–158: VTHRL50

VTHRL50 D6-D0	Vertical Window Noise Suppression Opening 50 Hz	Note
0000000	Opening in first line	Opening=4* ***VTHRL50***
...		
1111111	Opening in line 508	

Subaddress 33h

Table 3–159: BCOROFF

BCOROFF D7	**Blanklevel Coring Off:** Blanklevel generation coring (for sync-tip clamping only)
0	Coring on
1	Coring off

Table 3–160: VTHRL60

VTHRL60 D6-D0	Vertical Window Noise Suppression Opening 60 Hz	Note
0000000	Opening in first line	Opening=4****VTHRL60***
...		
1111111	Opening in line 508	

Subaddress 34h

Table 3–161: VTHRH60

VTHRH60 D3-D0	Vertical Window Noise Suppression Closing 60 Hz	Note
0000	Closing in line 262	Closing=262+4****VTHRH60***
...		
1111	Closing in line 262+60	

Table 3–162: VTHRH50

VTHRH50 D7-D4	Vertical Window Noise Suppression Closing 50 Hz	Note
0000	Closing in line 312	Closing=312+4****VTHRH50***
...		
1111	Closing in line 312+60	

Subaddress 35h

Table 3–163: CLMPSTGY

CLMPSTGY	Clamping Strategy
D7	
0	Back-porch clamping
1	Sync-tip-clamping

Table 3–164: SLLTHDVP

SLLTHDVP	Slicing Level Threshold V Polarity
D6	
0	Positive
1	Negative

Table 3–165: SLLTHDV

SLLTHDV			Slicing Level Threshold V
D5	D4	D3	
0	0	0	No offset
0	0	1	4
0	1	0	8
0	1	1	12
1	0	0	(Reserved)
1	0	1	Adaptive (limited to ±4)
1	1	0	Adaptive (limited to ±8)
1	1	1	Adaptive (limited to ±12)

Table 3–166: VFLYWHLMD

VFLYWHLMD		Vertical Flywheel Mode
D2	D1	
0	0	Check for correct standard
0	1	3 lines deviation allowed
1	0	4 lines deviation allowed, no check for interlace
1	1	5 lines deviation allowed, no check for interlace

Table 3–167: VFLYWHL

VFLYWHL	Vertical Flywheel
D0	
0	Disabled
1	Enabled

Subaddress 36h

Table 3–168: FLNSTRD

FLNSTRD		Force Line Standard at CVBS/RGB Front-end
D7	D6	
0	0	Automatic
0	1	Force 50 Hz
1	0	Force 60 Hz
1	1	(Reserved)

Table 3–169: CLMPCHARY

CLMPCHARY		Clamping Characteristic Y/CVBS: Characteristic of clamping error vs. clamping current
D5	D4	
0	0	High gain
0	1	Medium gain 1
1	0	Medium gain 2
1	1	Low gain

Table 3–170: VDETIFS

VDETIFS	Vertical Detection Slope
D3	
0	Normal
1	Slow

Table 3–171: VDETITC

VDETITC	Vertical Detection Integration Time Constant
D2	
0	Long
1	Short

Table 3–172: VLP

VLP		Lowpass for Vertical Sync-Separation
D1	D0	
0	0	None
0	1	Weak
1	0	Medium
1	1	Strong

Subaddress 37h

Table 3–173: LATENCY

LATENCY		Clamping Latency: ... additional idle-states
D7	**D6**	
0	0	0
0	1	2
1	0	4
1	1	6

Table 3–174: FILTBRST

FILTBRST	Burst Filter for Y/CVBS ADC
D5	
0	Disabled
1	Enabled

Table 3–175: CLMPIST

CLMPIST	Start of Clamping Pulse	Note
D4-D0		
00000	0.5 μs	START=0.5 μs+***CLMPIST****0.25 μs
...		
11111	8.25 μs	

4. Specifications

4.1. Outline Dimensions

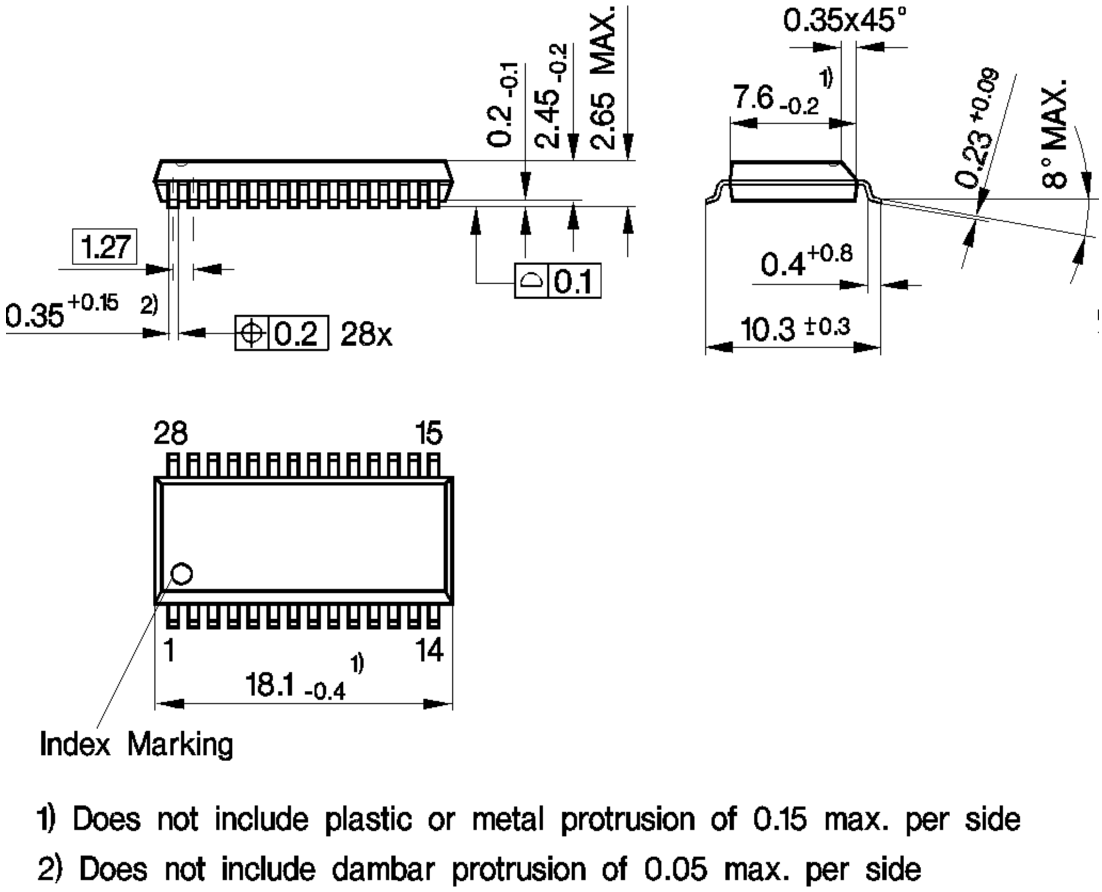

Fig. 4–1:
SOIC28-1: Plastic **S**mall **O**utline Package, **28** leads, (300mil)
Ordering code: XI
Weight approximately 0.77 g

4.2. Pin Connections and Short Descriptions

Pin No. SOIC28-1	Pin Name	Type	Connection (If not used)	Short Description
1	XIN	I		Crystal oscillator (input) or external clock input
2	XQ	O		Crystal oscillator (output)
3	HSP	I/TTL		Horizontal sync for parent channel
4	VSP	I/TTL		Vertical sync for parent channel
5	SDA	I/O		I^2C-bus data
6	SCL	I		I^2C-bus clcok
7	VDD	S		Digital supply voltage
8	VSS	S		Digital ground
9	I^2C	I		I^2C address
10	INT	O/TTL		Interupt
11	IN1	I/ANA	Let open or connect with 10 nf to ground	V/R input for external YUV/RGB source
12	IN2	I/ANA		Y/G input for external YUV/RGB source
13	IN3	I/ANA		U/B input for external YUV/RGB source
14	FSW	I		Fast switch input for YUV/RGB switch
15	SEL	O		Fast blanking output for PIP
16	OUT3	O/ANA		Analog output: Chrominance signal +(B-Y) or (B-y) or B
17	OUT2	O/ANA		Analog output: Luminance signal Y or G
18	OUT1	O/ANA		Analog output: Chrominance signal +(R-Y) or (R-Y) or R
19	VDDA2	S		Analog supply voltage for DAC
20	VSSA2	S		Analog ground for DAC
21	VREFH	I/ANA		Upper reference voltage for ADC and DAC
22	VDDA1	S		Analog supply voltage for ADC
23	VSSA1	S		Analog grouund for ADC
24	CVBS3	I/ANA		CVBS3 or V (SDA 9589x) or Y (from Y/C) input
25	VREFL	I/O		Lower reference voltage for ADC
26	CVBS2	I/ANA		CVBS2 or U (SDA 9589x) or Y (from Y/C) input
27	VREFM	I/O		Mid-level reference voltage for ADC
28	CVBS1	I/ANA		CVBS1 or Y (from YUV, SDA 9589x) input

4.3. Pin Descriptions

Pin 1, **XIN** - Crystal oscillator (input). Can be used for external clocking.

Pin 2, **XQ** - Crystal oscillator (output). Can be used for external clocking.

Pin 3, **HSP** - Horizontal sync for parent channel. Schmitt-trigger input with high hysteresis, for best jitter performance use pulses with steep slopes.

Pin 4, **VSP** - Vertical sync for parent channel. Schmitt-trigger input with high hysteresis, for best jitter performance use pulses with steep slopes.

Pin 5, **SDA** - I^2C-bus data. Low-side driver not used for SCL, slope of aknowledge is limited.

Pin 6, **SCL** - I^2C-bus clock. Low-side driver not used for SCL, slope of aknowledge is limited.

Pin 7, **VDD** - Digital supply voltage.

Pin 8, **VSS** - Digital ground

Pin 9, **I^2C** - I^2C address selection, only static switch supported.

Pin 10, **INT** - Interrupt.

Pin 11, **IN1** - V/R input for external YUV/RGB source.

Pin 12, **IN2** - Y/G input for external YUV/RGB source.

Pin 13, **IN3** - U/B input for external YUV/RGB source.

Pin 14, **FSW** - Fast switch input for YUV/RGB switch.

Pin 15, **SEL** - Fast blanking output for PIP. Low-side driver can be disabled (open source mode).

Pin 16, **OUT3** - Analog output: Chrominance signal +(B-Y) or (B-y) or B.

Pin 17, **OUT2** - Analog output: Luminance signal Y or G.

Pin 18, **OUT1** - Analog output: Chrominance signal +(R-Y) or (R-Y) or R.

Pin 19, **VDDA2** - Analog supply voltage for DAC.

Pin 20, **VSSA2** - Analog ground for DAC.

Pin 21, **VREFH** - Upper reference voltage for ADC and DAC.

Pin 22, **VDDA1** - Analog supply voltage for ADC

Pin 23, **VSSA1** - Analog grouund for ADC

Pin 24, **CVBS3** - Clamped video input. CVBS3 or V (SDA 9589x) or Y (from Y/C) input.

Pin 25, **VREFL** - Lower reference voltageefor ADC.

Pin 26, **CVBS2** - Clamped video input. CVBS2 or U (SDA 9589x) or Y (from Y/C) input.

Pin 27, **VREFM** - Mid-level reference voltage for ADC.

Pin 28, **CVBS1** - Clamped video input. CVBS1 or Y (from YUV, SDA 9589x) input.

4.4. Pin Configurations

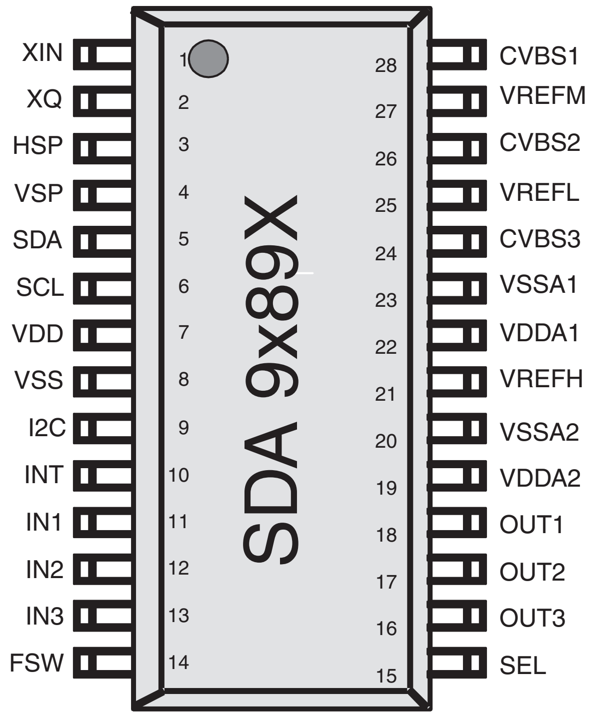

Fig. 4–2: SOIC28-1 Package

4.5. Pin Circuits

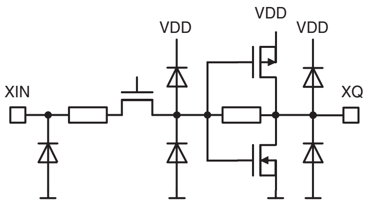

Fig. 4–3: Input/Output Pins: **XIN, XQ**

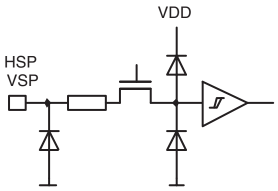

Fig. 4–4: Input Pins: **HSP, VSP**

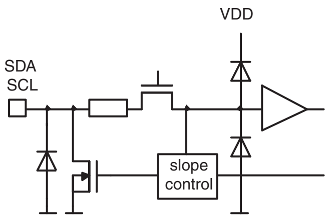

Fig. 4–5: Input/Output Pins: **SDA, SCL**

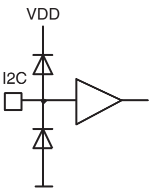

Fig. 4–6: I²C Bus Pins

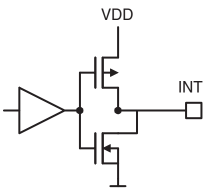

Fig. 4–7: Interrup Pin: **INT**

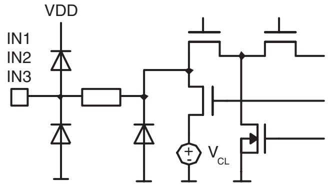

Fig. 4–8: Video Input Pins: **IN1, IN2, IN3**

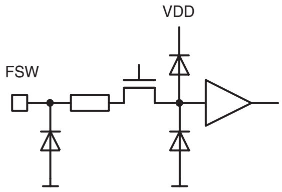

Fig. 4–9: Switch Input Pin: **FSW**

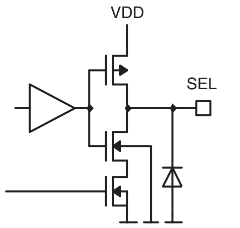

Fig. 4–10: Output Pin: **SEL**

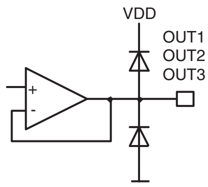

Fig. 4–11: Output Pins: **OUT3, OUT2, OUT1**

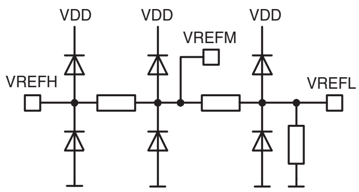

Fig. 4–12: Reference Voltage Pins: **VREFH, VREFL, VREFM**

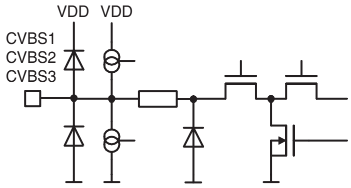

Fig. 4–13: Video Input Pins: **CVBS3, CVBS2, CVBS1**

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined
vacant = not applicable
positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

All voltages listed are referenced to ground (VSS) except where noted.All GND pins must be connected to a low-resistive ground plane close to the IC.

Table 4–1: Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Limit Values		Unit
			Min.	Max.	
T_A [1]	Ambient Operating Temperature SOIC28-1		0	70[2]	°C
T_C	Case Operating Temperature SOIC28-1		0	115	°C
T_S	Storage Temperature		–55	125	°C
P_{MAX}	Maximum Power Dissipation SOIC28-1			0.86	W
V_{SUP1}	Supply Voltage 1	VDD, VDDAx	-0.3	3.6	V
ΔV_{SUP}	Voltage differences within supply domains		-0.25	0.25	V
V_I	Input Voltage	SDA, SCL, HSP, VSP only	-0.3	5.5	V
V_I	Input Voltage	Except SDA, SCL, HSP, VSP	-0.3	V_{DD}+0.3	V
I_I	Input current		-100	+100	mA
V_O	Output Voltage	SDA only	-0.3	5.5	V
V_O	Output Voltage	Except SDA	-0.3	V_{DD}+0.3	V
I_O	Output Current		-100	+100	mA

[1] Measured on Micronas typical 2-layer (1s1p) board based on JESD - 51.2 Standard with maximum power consumption allowed for this package

[2] A power-optimized board layout is recommended. The Case Operating Temperature mentioned in the “Absolute Maximum Ratings” must not be exceeded at worst case conditions of the application.

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions/Characteristics” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All voltages listed are referenced to ground (VSS) except where noted.

All GND pins must be connected to a low-resistive ground plane close to the IC.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

4.6.2.1. General Recommended Operating Conditions

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
T_A	Ambient Operating Temperature SOIC28-1		0	25	70[1]	°C
T_C	Case Operating Temperature SOIC28-1		0	80	115	°C
P_{MAX}	Maximum Power Dissipation SOIC28-1				0.86 [2]	W
V_{SUP1}	Supply Voltage		3.15	3.3	3.45	V
ΔV_{SUP}	Voltage differences within supply domains			0.3		V
VIL	Input Voltage Low			0		V
VIH	Input Voltage High			V_{DD}		V

[1] A power-optimized board layout is recommended. The Case Operating Temperatures mentioned in the “Recommended Operating Conditions” must not be exceeded at worst case conditions of the application.

[2] P_{MAX} variation: user-determined by application circuit for I/Os

4.6.2.2. Recommended Operating Range

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
Main Horizontal/Vertical Sync Inputs						
F_{PH}	HSP Signal Frequency (1f_H mode)	VSP, HSP	15.000	15.625	16.250	kHz
F_{P2H}	HSP Signal Frequency (2f_H mode)		30.000	31.250	32.500	kHz
F_{P2H}	HSP Signal Frequency (VGA mode)		11.7	25.2	48	kHz
t_r	HSP Signal Rise Time (Noisefree transition)				100	ns
t_{HH}	HSP Signal High Time		200			ns
t_{LH}	HSP Signal Low Time		900			ns
f_{PV}	VSP Signal Frequency			50/60		Hz
f_{PV}	VSP Signal Frequency (Scan rate conversion)			100/ 120		Hz
t_{HV}	VSP Signal High Time		200			ns
t_{LV}	VSP Signal Low Time		200			ns
Inset Input						
f_H	Horizontal Frequency (60 Hz input)	CVBS3, CVBS2, CVBS1		15.734		kHz
f_H	Horizontal Frequency (50 Hz input)			15.625		kHz
V_{Sync}	Amplitude of Synchronization Pulse			300		mV
t_{DH}	Length of Horizontal Synchronisa-tion pulse			4.7		µs
t_{DV}	Length of Vertical Synchronization pulse			22		µs
A_{CHR}	Chroma Amplitude			300		mV
C_{CLI}	Input Coupling Capacitors (Necessary for proper clamping)		2.2	10	100	nF
R_{SRCI}	CVBS Source Resistance			100	500	Ω
V_i	Input Voltage Ranger at inputs CVBS1-3 (dep. on AGC setting)		0.5	1	1.5	V
Reference Voltages						
V_{REFL}	Reference Voltage Low	VREFL, VREFM, VREFH	1.10	1.20	1.30	V
V_{REFM}	Reference Voltage Medium		1.90	2.05	2.20	V
V_{REFH}	Reference Voltage Low		3.15	3.3	V_{DDA1}	V
RGB/YUV Switch						

Symbol	Parameter	Pin Name	Limit Values			Unit
			Min.	Typ.	Max.	
C_{CLS}	Input Coupling Capacitors (Necessary for proper clamping)	IN1, IN2, IN3, FSW	2.2	10	100	nF
R_{SRCS}	Source Resistance			100	500	Ω
V_{IS}	Input Voltage Range at inputs IN1-3		0.3	1	1.6	V
V_{IF}	Input Voltage Range at input FSW		0.3	1	1.6	V
I²C Addresse [1]						
V_{SA1}	Input Voltage Range for Address	I²C	0		0.8	V
V_{SA2}	Input Voltage Range for Address		2.8		V_{DDD}	V
f_{SCL}	SCL clock Frequency		0		400	kHz
t_{BUF}	Inactive Time before Start of Transmission		1.3			µs
$T_{SU;STA}$	Set-up Time Start Condition		0.6			µs
t_{LOW}	SCL Low Time		1.3			µs
t_{HIGH}	SCL High Time		0.6			µs
$T_{SU;DAT}$	Set-up Time DATA		100			ns
$T_{HD;DAT}$	Hold Time DATA		0		0.9	µs
t_R, t_F	SDA/SCL Rise/Fall Times		20+$		300	$=0.1 C_b/pF
$T_{SU;STO}$	Set-up Time Stop Condition		0.6			µs
C_b	Capacitive Load/Bus Line				400	pF
I²C Bus Inputs/Outputs						
V_{IH}	High Level Input Voltage (also for SDA/SCL input stages)	SDA, SCL	3		5.5	V
V_{IL}	Low Level Input Voltage (also for SDA/SCL input stages)		-0.25		1.5	V
	Spike Duration at Inputs		0	0	50	ns
I_{OL}	Low Lewel Output Current				6	mA
Digital to Analog Converters (7-bit)						
R_L	Load Resistance	OUT1, OUT2, OUT3	10			kΩ
C_L	Loas Capacitance				30	pF

1) Fast I²C Bus (All values arereferred to min(VIH) and max(VIL).
This specification of the bus lines need not be identical with the I/O stages specification because of optional series resistors between bus lines and I/O pins.

4.6.3. Characteristics

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
I_{DDtot}	Average Total Supply Current		180	210	240	mA	
All Digital Inputs							
C_I	Input Capacitance	TTL,I²C		7		pF	
	Input Leakage Current		-10		10	µA	Incl. leakage current of SDA output stage
SEL							
V_{OH}	High Level Output Voltage	SEL	2.4		V_{DD}	V	I_{OH}= -200 µA
V_{OH}	High Level Output Voltage		1.5		V_{DD}	V	I_{OH}= -4.5 µA
V_{OL}	Low Level Output Voltage				0.4		I_{OL}= 1.6 µA Only valid if bit SELDOWN= 1
FSW							
V_{IL}	Low Level Input Voltage	FSW	-0.25		0.4	V	
V_{IH}	High Level Input Voltage		0.9		V_{DD} +0.5	V	
	Delay FSW in → SEL out			10		V	
I²C Inputs							
V_{hys}	Schmitt-Trigger Hysteresis	SDA, SCL	0.1	0.2	0.5	V	Not tested
I²C Input/Output (Referenced to SCL; Open Drain Output)							
V_{OL}	Low Level Output Voltage	SDA			0.4	V	I_{OL}= 3 mA
V_{OL}	Low Level Output Voltage				0.6	V	I_{OL}= max
t_{OF}	Output Fall Time from min(V_{IH}) to max(V_{IL})		20 + 0.1* C_b/pF		250	ns	10 pF ≤ Cb ≤ 400 pF
Analog Inputs							
I_L		CVBS1, CVBS2, CVBS3	-100		100	nA	Clamping inactive
C_I				7		pF	
ΔCLE			-1		1	LSB	Settled stage
$\lvert\bar{I}_{CLP}\rvert$			43		326	µA	Dependent on clamping error
$\lvert\bar{I}_{CLPx}\rvert$ / $\lvert\bar{I}_{CLP}\rvert$			-40		40	%	
V_{REFH} - V_{REFL}			0.5		1.5	V	VDDA1= 3.3 V
DNL			-1		1	LSB	V_{REFH} - V_{REFL} = max
CT				-50		dB	

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Digital to Analog Converters (7-bit)							
DNLE	D.C Differential Nonlinearity	OUT1, OUT2, OUT3	-0.5		0.5	LSB	
V_{OL}	Full Range Output Voltage		0.3			V	CON, UAMP, VAMP, YAMP = 0
V_{OH}	Full Range Output Voltage				1.6	V	CON, UAMP, VAMP, YAMP = max
V_O	Output Voltage		0.9	1	1.1		CON, UAMP, VAMP, YAMP = default, VREF = constant
M_{CH}	Deviation of OUT1-3 (matching)		-3		3	%	
ΔCON	Contrast Increase			30		%	
ΔAMP	Output Amplitude Ratio $(U_{OH} - U_{OL}) / U_{OL}$			400		%	
ΔBRT	Brightness Increase				15	LSB	
ΔPED	Pedestal Level Variation				± 7.5	LSB	
RGB/YUV Switch							
ΔV_I	Input Voltage Range	IN1, IN2, IN3			1.2	V_{pp}	
BW	Bandwidth (-3 dB)			25		MHz	R_L>10kΩ; C_L = 20pF
G	Gain		0.9		1.1		
ΔG	Gain Difference RGB				3	%	f< 4 MHz
CT_I	Crosstalk between Inputs				-40	dB	f= 5 MHz, (R-G-B, U-V)
CT_I	Crosstalk between Inputs				-45	dB	f= 5 MHz, (Y-UV)
D	Isolation (off state)		45			dB	f= 5 MHz
ΔCLPE	Clamping Level Difference at Output				15	mV	Between external and internal source
Color Decoder/Synchronization and Luminance Processing							
$\Delta f_H/f_H$	Horizontal PLL pull-in Range		13.3		17.4	kHz	VCR1 and VCR2
$\Delta f_H/f_H$	Horizontal PLL pull-in Range		13.3		17.4	kHz	TV1 and TV2
V_{sync}	Amplitude of Synchronization pulse		60		600	mV	AGC set to 1.2 V input signals
t_{HD}	Length of Horizontal synchronization pulse		1.8			µs	
t_{DV}	Length of vertical synchronization pulse		22			µs	
CR_{ACC}	ACC Range		-24		+6	dB	
CR_{AGC}	AGC Range		-7.5		+2	dB	
Δf_{SC}	Chroma PLL pull-in Range			± 500		Hz	Nominal crystal frequency

Symbol	Parameter	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Data Slicer							
V_D	Data Level		266	350	434	mV	CC
ΔV_D	Data Height		280	350	420	mV	CC
EH	Eye Height		26.6			%	
CD25	Co Channel Distorsion				174	mV	25 kHz
CD50	Co Channel distortion				155	mV	50 kHz
N	Max. Permissible Noise				20	dB	

4.6.4. Recommended Crystal Characteristics

Symbol	Parameter	Limit Values			Unit
		Min.	Typ.	Max.	
f_{xtal}	Frequency (Deviation outside this range will cause color decoding failures)	XIN, XQ	20.248	20.25	20.252
$\Delta f_{max}/f_{xtal}$	Maximum Permissible Frequency Deviation (Deviation outside this range will cause color decoding failures)		-100		100
$\Delta f/f_{xtal}$	Recommended Permissible Fre-quency Deviation		-40	0	40
C_L	Load Capacitance		12	27	39
R_S	Series Resonance Resistance			25	
C_1	Motional Capacitance			27	
C_0	Paralle Capacitance			7	
In the operating range the function given in the circuit description are fulfilled.					

5. Application

5.1. Application Circuit

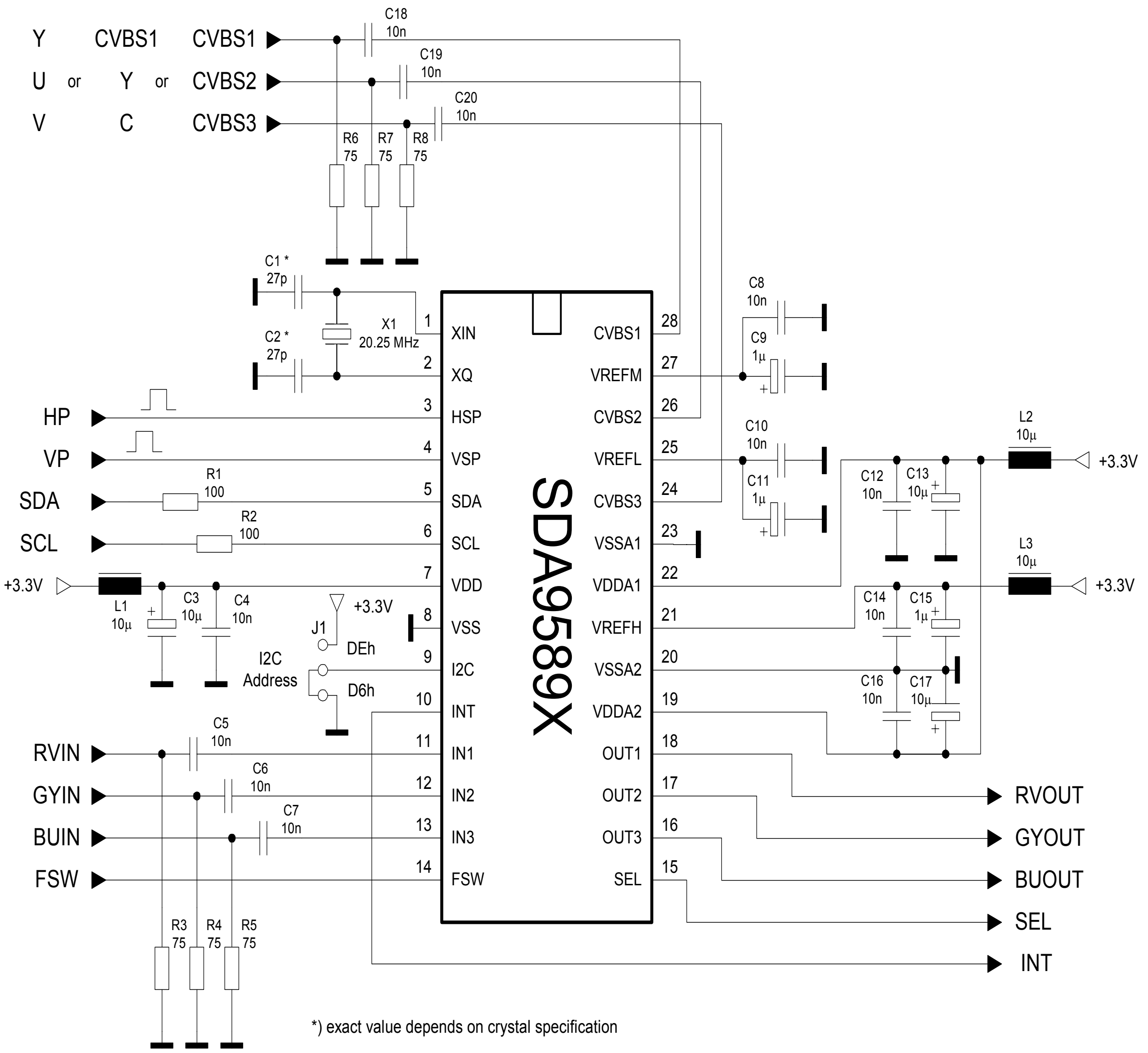

Fig. 5–1: Application Circuit

5.2. Application Examples

The following two figures show 100/120 Hz applications with the Micronas Feature Box SDA 9400/01. As the chip supports two I²C addresses and owns a RGB switch dual-PIP applications are easy to implement. The arrangement for best possible performance is shown in the Fig. 5–2.

The output of two SOPHISTICUS are connected to the YUV (or RGB) input of the video processor of the main channel. Due to the 4:2:2 processing within the SDA 9400 the inset picture remains brilliant.

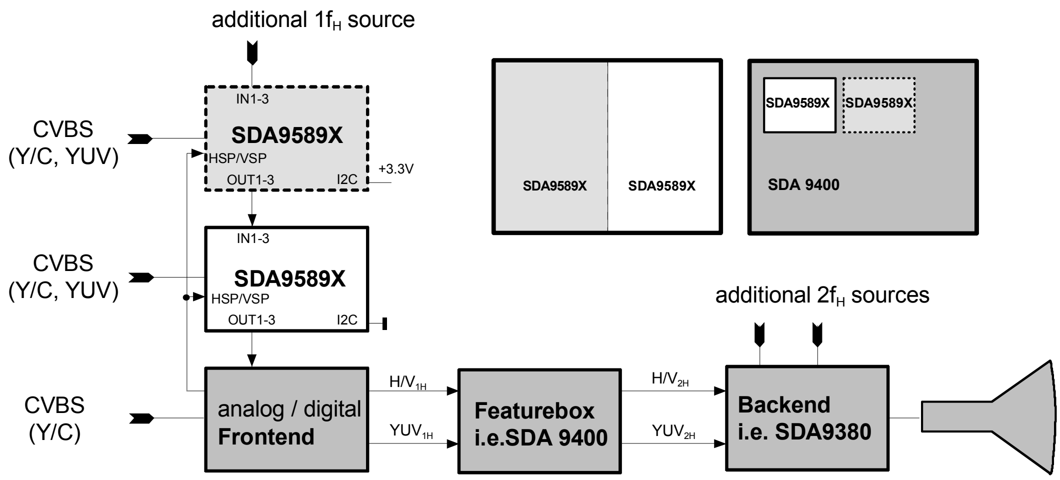

Fig. 5–2: SDA 9589X Application with Insertion in Front of the Feature Box

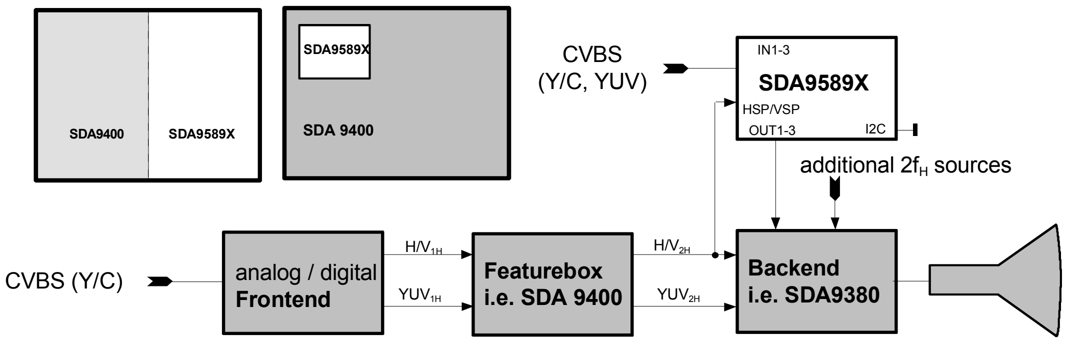

Fig. 5–3: SDA 9589X Application with Insertion behind the Feature Box

Connecting the SDA 9589x/SDA 9489x directly to the RGB input of the RGB processor is possible as well. One picture is generated from SDA 9589x/SDA 9489x device, the other one from the Feature Box. This cheap implementation preserves the chroma of inset channel at its full bandwidth, although frame mode is only possible for PIP pictures smaller than 1/9. The output of an OSD/Text processor may be fed to the RGB switch of the SDA 9589x/SDA 9489x.

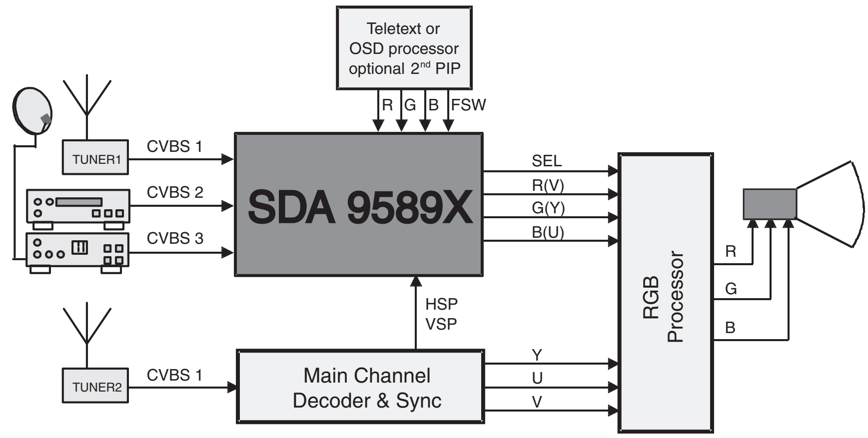

Fig. 5–4: General Application with 3 CVBS Sources and Teletext-Processor

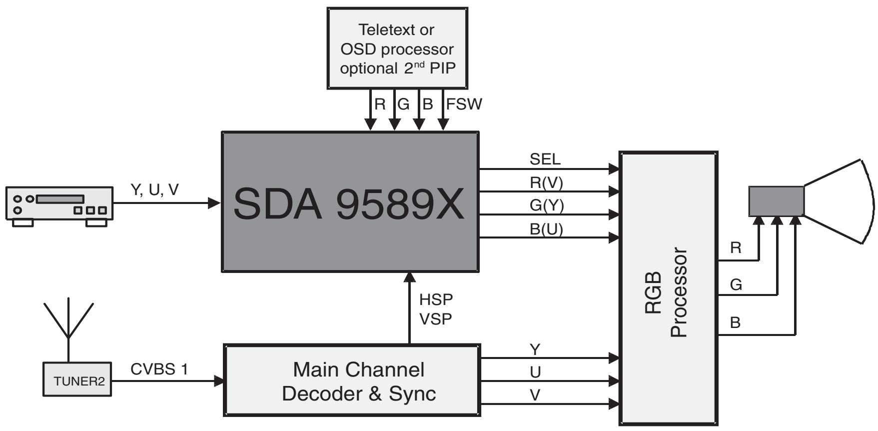

Fig. 5–5: General Application with YUV Source from DVD

6. Data Sheet History

1. Preliminary Data Sheet: "SDA 9489x PIP IV Advanced, SDA 9589x SOPHISTICUS High-end Picture-In-Picture ICs", Dec. 14, 2001, 6251-562-2PD. Second release of the preliminary data sheet.

2. Data Sheet: "SDA 9489X, SDA 9589X High-end Picture-In-Picture ICs", March 15, 2004, 6251-562-1DS. First release of the data sheet.
   Major changes:

– Subaddress 03h
  HFP: Bit names updated (new:D3-D0)
  VFP: Bit namess updated (new:D7-D4)

– Subaddress 34h:
  VTHRH60: Bit names updated (new:D3-D0)
  VTHRH50: Bit names updated (new:D7-D4)

Micronas GmbH
Hans-Bunte-Strasse 19
D-79108 Freiburg (Germany)
P.O. Box 840
D-79008 Freiburg (Germany)
Tel. +49-761-517-0
Fax +49-761-517-2174
E-mail: docservice@micronas.com
Internet: www.micronas.com

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