Signetics

SAB3037
FLL Tuning and Control Circuit

Product Specification

Linear Products

DESCRIPTION

The SAB3037 provides closed-loop digital tuning of TV receivers, with or without AFC, as required. It also controls up to 4 analog functions, 4 general purpose I/O ports and 4 high-current outputs for tuner band selection.

The IC is used in conjunction with a microcomputer from the MAB8400 family and is controlled via a two-wire, bi-directional I^2C bus.

FEATURES

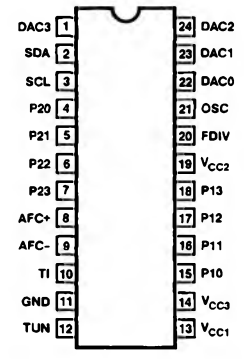
- **Combined analog and digital circuitry minimizes the number of additional interfacing components required**
- **Frequency measurement with resolution of 50kHz**
- **Selectable prescaler divisor of 64 or 256**
- **32V tuning voltage amplifier**
- **4 high-current outputs for direct band selection**
- **4 static digital to analog convertors (DACs) for control of analog functions**
- **Four general purpose input/output (I/O) ports**
- **Tuning with control of speed and direction**
- **Tuning with or without AFC**
- **Single-pin, 4MHz on-chip oscillator**
- **I^2C bus slave transceiver**

APPLICATIONS

- **TV receivers**
- **Satellite receivers**
- **CATV converters**

PIN CONFIGURATION

N Package



TOP VIEW

CD11970S

PIN NO.	SYMBOL	DESCRIPTION
1	DAC3	Output of static DAC
2	SDA	Serial data line } I^2C bus
3	SCL	Serial clock line } I^2C bus
4	P20	General purpose input/output ports
5	P21	
6	P22	
7	P23	
8	AFC+	AFC inputs
9	AFC−	
10	TI	Tuning voltage amplifier inverting input
11	GND	Ground
12	TUN	Tuning voltage amplifier output
13	V_{CC1}	+12V supply voltage
14	V_{CC3}	+32V supply for tuning voltage amplifier
15	P10	High-current band-selection output ports
16	P11	
17	P12	
18	P13	
19	V_{CC2}	Positive supply for high-current band-selection output circuits
20	FDIV	Input from prescaler
21	OSC	Crystal oscillator input
22	DAC0	Outputs of static DACs
23	DAC1	
24	DAC2	

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−20°C to +70°C	SAB3037N

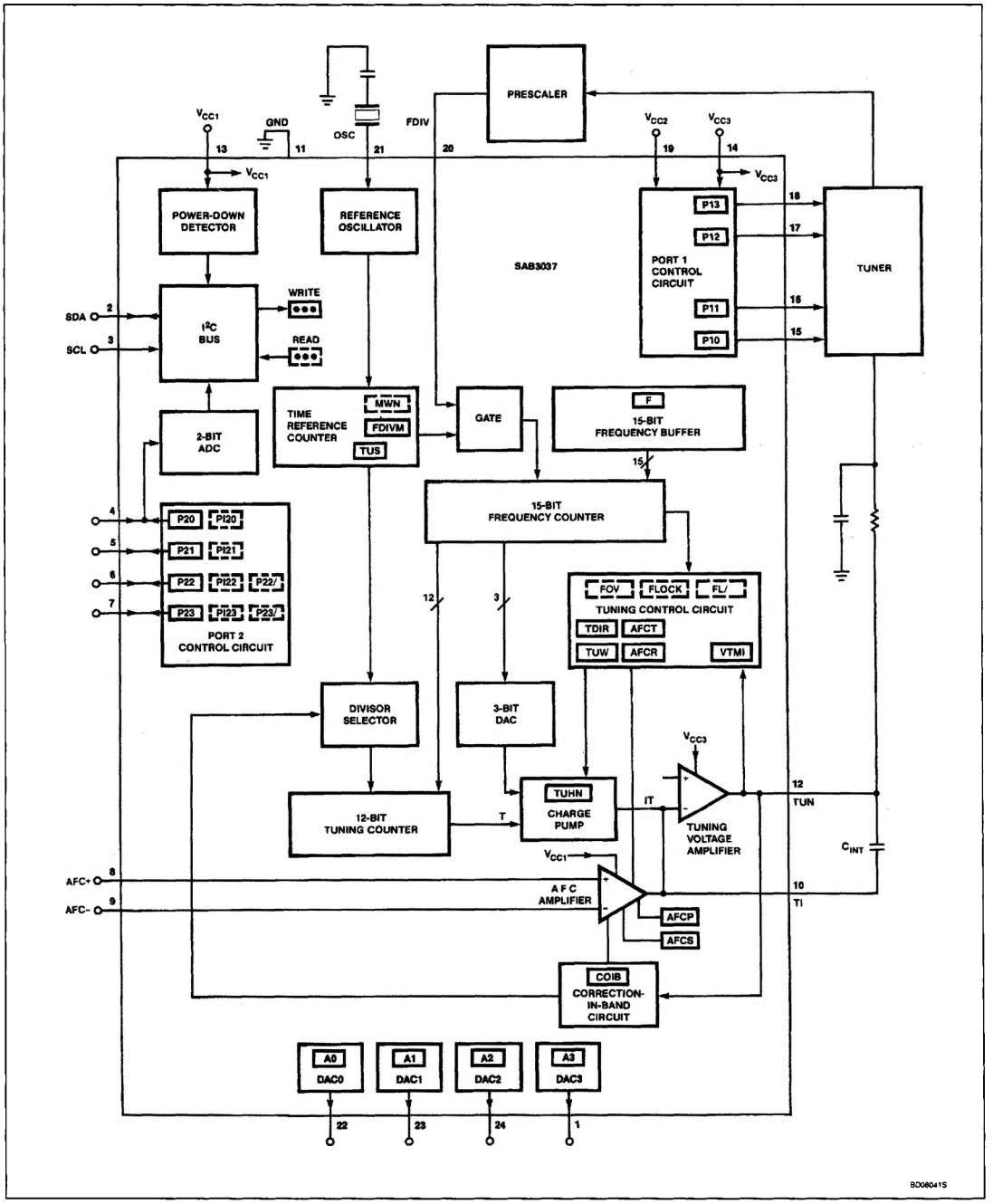
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Supply voltage ranges:		
V_{CC1}	(Pin 13)	−0.3 to +18	V
V_{CC2}	(Pin 19)	−0.3 to +18	V
V_{CC3}	(Pin 14)	−0.3 to +36	V
	Input/output voltage ranges:		
V_{SDA}	(Pin 2)	−0.3 to +18	V
V_{SCL}	(Pin 3)	−0.3 to +18	V
V_{P2X}	(Pins 4 to 7)	−0.3 to +18	V
$V_{AFC+,\ AFC-}$	(Pins 8 and 9)	−0.3 to V_{CC1} [1]	V
V_{TI}	(Pin 10)	−0.3 to V_{CC1} [1]	V
V_{TUN}	(Pin 12)	−0.3 to V_{CC3} [3]	V
V_{P1X}	(Pins 15 to 18)	−0.3 to V_{CC2} [3]	V
V_{FDIV}	(Pin 20)	−0.3 to V_{CC1} [1]	V
V_{OSC}	(Pin 21)	−0.3 to +5	V
V_{DACX}	(Pins 1 and 22 to 24)	−0.3 to V_{CC} [1]	V
P_{TOT}	Total power dissipation	1000	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−20 to +70	°C

NOTES:

1. Pin voltage may exceed supply voltage if current is limited to 10mA.
2. Pin voltage must not exceed 18V but may exceed V_{CC2} if current is limited to 200mA.

BLOCK DIAGRAM



DC AND AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC1}	Supply voltages	10.5	12	13.5	V
V_{CC2}		4.7	13	16	V
V_{CC3}		30	32	35	V
I_{CC1}	Supply currents (no outputs loaded)	18	30	45	mA
I_{CC2}		0		0.1	mA
I_{CC3}		0.2	0.6	2	mA
I_{CC2A}	Additional supply currents (A)[1]	−2		I_{OHP1X}	mA
I_{CC3A}		0.2		2	mA
P_{TOT}	Total power dissipation		380		mW
T_A	Operating ambient temperature	−20		+70	°C
I²C bus inputs/outputs SDA input (Pin 2); SCL input (Pin 3)					
V_{IH}	Input voltage HIGH[2]	3		$V_{CC}-1$	V
V_{IL}	Input voltage LOW	−0.3		1.5	V
I_{IH}	Input current HIGH[2]			10	μA
I_{IL}	Input current LOW[2]			10	μA
	SDA output (Pin 2, open-collector)				
V_{OL}	Output voltage LOW at $I_{OL} = 3mA$			0.4	V
I_{OL}	Maximum output sink current		5		mA
Open-collector I/O ports P20, P21, P22, P23 (Pins 4 to 7, open-collector)					
V_{IH}	Input voltage HIGH	2		16	V
V_{IL}	Input voltage LOW	−0.3		0.8	V
I_{IH}	Input current HIGH			25	μA
$-I_{IL}$	Input current LOW			25	μA
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
I_{OL}	Maximum output sink current		4		mA
AFC amplifier Inputs AFC+, AFC− (Pins 8, 9)					
	Transconductance for input voltages up to 1V differential: AFCS1 AFCS2				
g00	0 0	100	250	800	nA/V
g01	0 1	15	25	35	μA/V
g10	1 0	30	50	70	μA/V
g11	1 1	60	100	140	μA/V
ΔM_g	Tolerance of transconductance multiplying factor (2, 4 or 8) when correction-in-band is used	−20		+20	%
V_{IOFF}	Input offset voltage	−75		+75	mV
V_{COM}	Common-mode input voltage	3		$V_{CC1}-2.5$	V
CMRR	Common-mode rejection ratio		50		dB
PSRR	Power supply (V_{CC1}) rejection ratio		50		dB
I_I	Input current			500	nA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Tuning voltage amplifier Input TI, output TUN (Pins 10, 12)					
V_{TUN}	Maximum output voltage at $I_{LOAD} = \pm 2.5mA$	$V_{CC3} - 1.6$		$V_{CC3} - 0.4$	V
	Minimum output voltage at $I_{LOAD} = \pm 2.5mA$: VTMI1 VTMI0				
V_{TM00}	0 0	300		500	mV
V_{TM10}	1 0	450		650	mV
V_{TM11}	1 1	650		900	mV
$-I_{TUNH}$	Maximum output source current	2.5		8	mA
I_{TUNL}	Maximum output sink current		40		mA
I_{TI}	Input bias current	−5		+5	nA
PSRR	Power supply V_{CC3} rejection ratio		60		dB
	Minimum charge IT to tuning voltage amplifier TUHN1 TUHN0				
CH_{00}	0 0	0.4	1	1.7	µA/µs
CH_{01}	0 1	4	8	14	µA/µs
CH_{10}	1 0	15	30	48	µA/µs
CH_{11}	1 1	130	250	370	µA/µs
ΔCH	Tolerance of charge (or ΔV_{TUN}) multiplying factor when COIB and/or TUS are used	−20		+20	%
	Maximum current I into tuning amplifier TUHN1 TUHN0				
I_{T00}	0 0	1.7	3.5	5.1	µA
I_{T01}	0 1	15	29	41	µA
I_{T10}	1 0	65	110	160	µA
I_{T11}	1 1	530	875	1220	µA
Correction-in-band					
ΔV_{CIB}	Tolerance of correction-in-band levels 12V, 18V, and 24V	−15		+15	%
Band-select output ports P10, P11, P12, P13 (Pins 15 to 18)					
V_{OH}	Output voltage HIGH at $-I_{OH} = 50mA$[3]	$V_{CC2} - 0.6$			V
V_{OL}	Output voltage LOW at $I_{OL} = 2mA$			0.4	V
$-I_{OH}$	Maximum output source current[3]		130	200	mA
I_{OL}	Maximum output sink current		5		mA
FDIV Input (Pin 20)					
$V_{FDIV\ (P-P)}$	Input voltage (peak-to-peak value) (t_{RISE} and $t_{FALL} \leq 40ns$)	0.1		2	V
	Duty cycle	40		60	%
f_{MAX}	Maximum input frequency	14.5			MHz
Z_I	Input impedance		8		kΩ
C_I	Input capacitance		5		pF
OSC Input (Pin 21)					
R_X	Crystal resistance at resonance (4MHz)			150	Ω

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$; V_{CC1}, V_{CC2}, V_{CC3} at typical voltages, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
DAC outputs 0 to 3 (Pins 22 to 24 and Pin 1)					
V_{DH}	Maximum output voltage (no load) at $V_{CC1} = 12V$[4]	10		11.5	V
V_{DL}	Minimum output voltage (no load) at $V_{CC1} = 12V$[4]	0.1		1	V
ΔV_D	Positive value of smallest step (1 least significant bit)	0		350	mV
	Deviation from linearity			0.5	V
Z_O	Output impedance at $I_{LOAD} = \pm 2mA$			70	Ω
$-I_{DH}$	Maximum output source current			6	mA
I_{DL}	Maximum output sink current		8		mA
Power-down reset					
V_{PD}	Maximum supply voltage V_{CC1} at which power-down reset is active	7.5		9.5	V
t_R	V_{CC1} rise time during power-up (up to V_{PD})	5			μs
Voltage level for valid module address					
	Voltage level at P20 (Pin 4) for valid module address as a function of MA1, MA0				
	MA1 MA0				
V_{VA00}	0 0	−0.3		16	V
V_{VA01}	0 1	−0.3		0.8	V
V_{VA10}	1 0	2.5		$V_{CC1} - 2$	V
V_{VA11}	1 1	$V_{CC1} - 0.3$		V_{CC1}	V

NOTES:

1. For each band-select output which is programmed at logic 1, sourcing a current I_{OHP1X}, the additional supply currents (A) shown must be added to I_{CC2} and I_{CC3}, respectively.
2. If $V_{CC1} < 1V$, the input current is limited to 10μA at input voltages up to 16V.
3. At continuous operation the output current should not exceed 50mA. When the output is short-circuited to ground for several seconds the device may be damaged.
4. Values are proportional to V_{CC1}.

FUNCTIONAL DESCRIPTION

The SAB3037 is a monolithic computer interface which provides tuning and control functions and operates in conjunction with a microcomputer via an I^2C bus.

Tuning

This is performed using frequency-locked loop digital control. Data corresponding to the required tuner frequency is stored in a 15-bit frequency buffer. The actual tuner frequency, divided by a factor of 256 (or by 64) by a prescaler, is applied via a gate to a 15-bit frequency counter. This input (FDIV) is measured over a period controlled by a time reference counter and is compared with the contents of the frequency buffer. The result of the comparison is used to control the tuning voltage so that the tuner frequency equals the contents of the frequency buffer multiplied by 50kHz within a programmable tuning window (TUW).

The system cycles over a period of 6.4ms (or 2.56ms), controlled by the time reference counter which is clocked by an on-chip 4MHz reference oscillator. Regulation of the tuning voltage is performed by a charge pump frequency-locked loop system. The charge IT flowing into the tuning voltage amplifier is controlled by the tuning counter, 3-bit DAC and the charge pump circuit. The charge IT is linear with the frequency deviation Δf in steps of 50kHz. For loop gain control, the relationship $\Delta IT/\Delta f$ is programmable. In the normal mode (when control bits TUHN0 and TUHN1 are both at logic 1 (see OPERATION) the minimum charge IT at $\Delta f = 50kHz$ equals $250\mu A/\mu s$ (typical).

By programming the tuning sensitivity bits (TUS), the charge IT can be doubled up to 6 times. If correction-in-band (COIB) is programmed, the charge can be further doubled up to three times in relation to the tuning voltage level. From this, the maximum charge IT at $\Delta f = 50kHz$ equals $2^6 \times 2^3 \times 250\mu A/\mu s$ (typical).

The maximum tuning current I is $875\mu A$ (typical). In the tuning-hold (TUHN) mode (TUHN is Active-LOW), the tuning current I is reduced and as a consequence the charge into the tuning amplifier is also reduced.

An in-lock situation can be detected by reading FLOCK. When the tuner oscillator frequency is within the programmable tuning window (TUW), FLOCK is set to logic 1. If the frequency is also within the programmable AFC hold range (AFCR), which always occurs if AFCR is wider than TUW, control bit AFCT can be set to logic 1. When set, digital tuning will be switched off, AFC will be switched on and FLOCK will stay at logic 1 as long as the oscillator frequency is within AFCR. If the frequency of the tuning oscillator does not remain within AFCR, AFCT is cleared automatically and the system reverts to digital tuning. To be able to detect this situation, the occurrence of positive and negative transitions in the FLOCK signal can be read (FL/1N and FL/0N). AFCT can also be cleared by programming the AFCT bit to logic 0.

The AFC has programmable polarity and transconductance; the latter can be doubled up to 3 times, depending on the tuning voltage level if correction-in-band is used.

The direction of tuning is programmable by using control bits TDIRD (tuning direction down) and TDIRU (tuning direction up). If a tuner enters a region in which oscillation stops, then, providing the prescaler remains stable, no FDIV signal is supplied to CITAC. In this situation the system will tune up, moving away from frequency lock-in. This situation is avoided by setting TDIRD which causes the system to tune down. In normal operation TDIRD must be cleared.

If a tuner stops oscillating and the prescaler becomes unstable by going into self-oscillation at a very high frequency, the system will react by tuning down, moving away from frequency lock-in. To overcome this, the system can be forced to tune up at the lowest sensitivity (TUS) value, by setting TDIRU.

Setting both TDIRD and TDIRU causes the digital tuning to be interrupted and AFC to be switched on.

The minimum tuning voltage which can be generated during digital tuning is programmable by VTMI to prevent the tuner from being driven into an unspecified low tuning voltage region.

Control

For tuner band selection there are four outputs — P10 to P13 — which are capable of sourcing up to 50mA at a voltage drop of less than 600mV with respect to the separate power supply input V_{CC2}.

For additional digital control, four open-collector I/O ports — P20 to P23 — are provided. Ports P22 and P23 are capable of detecting positive and negative transitions in their input signals. With the aid of port P20, up to three independent module addresses can be programmed.

Four 6-bit digital-to-analog converters — DAC0 to DAC3 — are provided for analog control.

Reset

CITAC goes into the power-down reset mode when V_{CC1} is below 8.5V (typical). In this mode all registers are set to a defined state. Reset can also be programmed.

OPERATION

Write

CITAC is controlled via a bidirectional two-wire I^2C bus. For programming, a module address, R/$\overline{W}$ bit (logic 0), an instruction byte and a data/control byte are written into CITAC in the format shown in Figure 1.

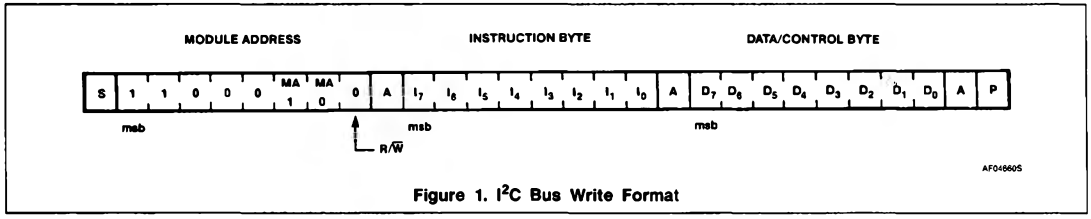


Figure 1. I^2C Bus Write Format

The module address bits MA1, MA0 are used to give a 2-bit module address as a function of the voltage at port P20 as shown in Table 1.

Acknowledge (A) is generated by CITAC only when a valid address is received and the device is not in the power-down reset mode (V_{CC1} > 8.5V (typical)).

Table 1. Valid Module Addresses

MA1	MA0	P20
0	0	Don't care
0	1	GND
1	0	½ V_{CC1}
1	1	V_{CC1}

Tuning

Tuning is controlled by the instruction and data/control bytes as shown in Figure 2.

Frequency

Frequency is set when Bit I_7 of the instruction byte is set to logic 1; the remainder of this byte together with the data/control byte are loaded into the frequency buffer. The frequency to which the tuner oscillator is regulated equals the decimal representation of the 15-bit word multiplied by 50kHz. All frequency bits are set to logic 1 at reset.

Tuning Hold

The TUHN bits are used to decrease the maximum tuning current and, as a consequence, the minimum charge IT (at Δf = 50kHz) into the tuning amplifier.

Table 2. Tuning Current Control

TUHN1	TUHN0	TYP. I_{MAX} (μA)	TYP. IT_{MIN} (μA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (μV)
0	0	3.5[1]	1[1]	1[1]
0	1	29	8	8
1	0	110	30	30
1	1	875	250	250

NOTE:
1. Values after reset.

During tuning but before lock-in, the highest current value should be selected. After lock-in the current may be reduced to decrease the tuning voltage ripple.

The lowest current value should not be used for tuning due to the input bias current of the tuning voltage amplifier (maximum 5nA). However, it is good practice to program the lowest current value during tuner band switching.

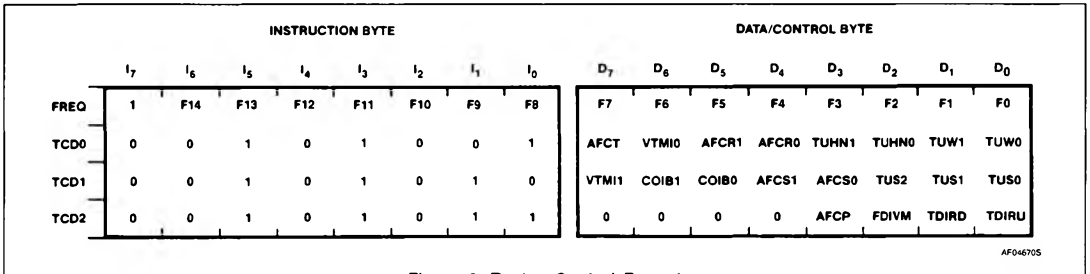


Figure 2. Tuning Control Format

Table 3. Minimum Charge IT as a Function of TUS Δf = 50kHz; TUHN0 = Logic 1; TUHN1 = Logic 1

TUS2	TUS1	TUS0	TYP. IT_{MIN} (mA/μs)	TYP. ΔV_{TUNmin} at C_{INT} = 1μF (mV)
0	0	0	0.25[1]	0.25[1]
0	0	1	0.5	0.5
0	1	0	1	1
0	1	1	2	2
1	0	0	4	4
1	0	1	8	8
1	1	0	16	16

NOTE:
1. Values after reset.

Table 4. Programming Correction-In-Band

COIB1	COIB0	CHARGE MULTIPLYING FACTORS AT TYPICAL VALUES OF V_{TUN} AT:			
		< 12V	12 to 18V	18 to 24V	> 24V
0	0	1[1]	1[1]	1[1]	1[1]
0	1	1	1	1	2
1	0	1	1	2	4
1	1	1	2	4	8

NOTE:
1. Values after reset.

Table 5. Tuning Window Programming

TUW1	TUW0	|Δf| (kHz)	TUNING WINDOW (kHz)
0	0	0[1]	0[1]
0	1	50	100
1	0	150	300

NOTE:
1. Values after reset.

Table 6. AFC Hold Range Programming

AFCR1	AFCR0	|Δf| (kHz)	AFC HOLD RANGE (kHz)
0	0	0[1]	0[1]
0	1	350	700
1	0	750	1500

NOTE:
1. Values after reset.

Table 7. Transconductance Programming

AFCS1	AFCS0	TYP. TRANSCONDUCTANCE (μA/V)
0	0	0.25[1]
0	1	25
1	0	50
1	1	100

NOTE:
1. Values after reset.

Tuning Sensitivity
To be able to program an optimum loop gain, the charge IT can be programmed by changing T using tuning sensitivity (TUS). Table 3 shows the minimum charge IT obtained by programming the TUS bits at Δf = 50kHz; TUHN0 and TUHN1 = logic 1.

Correction-In-Band
This control is used to correct the loop gain of the tuning system to reduce in-band variations due to a non-linear voltage/frequency characteristic of the tuner. Correction-in-band (COIB) controls the time T of the charge equation IT and takes into account the tuning voltage V_{TUN} to give charge multiplying factors as shown in Table 4.

The transconductance multiplying factor of the AFC amplifier is similar when COIB is used, except for the lowest transconductance which is not affected.

Tuning Window
Digital tuning is interrupted and FLOCK is set to logic 1 (in-lock) when the absolute deviation |Δf| between the tuner oscillator frequency and the programmed frequency is smaller than the programmed TUW value (see Table 5). If |Δf| is up to 50kHz above the values listed in Table 5, it is possible for the system to be locked depending on the phase relationship between FDIV and the reference counter.

AFC
When AFCT is set to logic 1 it will not be cleared and the AFC will remain on as long as |Δf| is less than the value programmed for the AFC hold range AFCR (see Table 6). It is possible for the AFC to remain on for values of up to 50kHz more than the programmed value depending on the phase relationship between FDIV and the reference counter.

Transconductance
The transconductance (g) of the AFC amplifier is programmed via the AFC sensitivity bits AFCS as shown in Table 7.

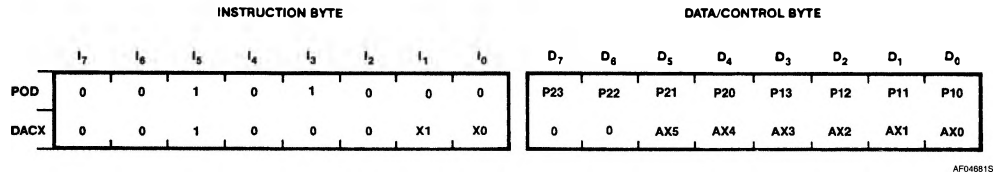


Figure 3. Control Programming

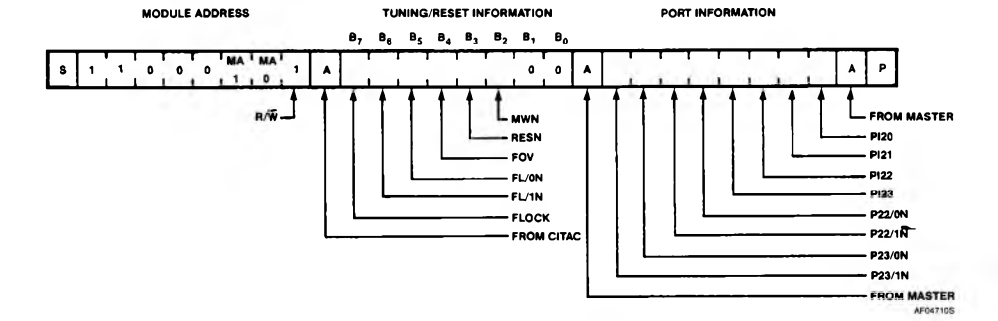


Figure 4. Information Byte Format

AFC Polarity

If a positive differential input voltage is applied to the (switched-on) AFC amplifier, the tuning voltage V_{TUN} falls when the AFC polarity bit AFCP is at logic 0 (value after reset). At AFCP = logic 1, V_{TUN} rises.

Minimum Tuning Voltage

Both minimum tuning voltage control bits, VTMI1 and VTMI0, are at logic 0 after reset. Further details are given in the DC Electrical Characteristics table.

Frequency Measuring Window

The frequency measuring window which is programmed must correspond with the division factor of the prescaler in use (see Table 8).

Tuning Direction

Both tuning direction bits, TDIRU (up) and TDIRD (down), are at logic 0 after reset.

Control

The instruction bytes POD (port output data) and DACX (digital-to-analog converter control) are shown in Figure 5, together with the corresponding data/control bytes. Control is implemented as follows:

P13, P12, P11, P10 — Band select outputs. If a logic 1 is programmed on any of the POD bits D_3 to D_0, the relevant output goes High. All outputs are Low after reset.

P23, P22, P21, P20 — Open-collector I/O ports. If a logic 0 is programmed on any of the POD bits D_7 to D_4, the relevant output is forced LOW. All outputs are at logic 1 after reset (high impedance state).

DACX — Digital-to-analog converters. The digital-to-analog converter selected corresponds to the decimal equivalent of the DACX bits X1, X0. The output voltage of the selected DAC is set by programming the bits AX5 to AX0; the lowest output voltage is programmed with all data AX5 to AX0 at logic 0, or after reset has been activated.

Table 8. Frequency Measuring Window Programming

FDIVM	PRESCALER DIVISION FACTOR	CYCLE PERIOD (ms)	MEASURING WINDOW (ms)
0	256	6.4[1]	5.12[1]
1	64	2.56	1.28

NOTE:
1. Values after reset.

Read

Information is read from CITAC when the R/$\overline{W}$ bit is set to logic 1. An acknowledge must be generated by the master after each data byte to allow transmission to continue. If no acknowledge is generated by the master, the slave (CITAC) stops transmitting. The format of the information bytes is shown in Figure 4.

Tuning/Reset Information Bits

FLOCK — Set to logic 1 when the tuning oscillator frequency is within the programmed tuning window.

FL/1N — Set to logic 0 (Active-LOW) when FLOCK changes from 0 to 1 and is reset to logic 1 automatically after tuning information has been read.

FL/0N — As for FL/1N but is set to logic 0 when FLOCK changes from 1 to 0.

FOV — Indicates frequency overflow. When the tuner oscillator frequency is too high with respect to the programmed frequency, FOV is at logic 1, and when too low, FOV is at logic 0. FOV is not valid when TDIRU and/or TDIRD are set to logic 1.

RESN — Set to logic 0 (Active-LOW) by a programmed reset or a power-down-reset. It is reset to logic 1 automatically after tuning/reset information has been read.

MWN — MWN (frequency measuring window, Active-LOW) is at logic 1 for a period of 1.28ms, during which time the results of frequency measurement are processed. This time is independent of the cycle period. During the remaining time, MWN is at logic 0 and the received frequency is measured.

When slightly different frequencies are programmed repeatedly and AFC is switched on, the received frequency can be measured using FOV and FLOCK. To prevent the frequency counter and frequency buffer being loaded at the same time, frequency should be programmed only during the period of MWN = logic 0.

Port Information Bits

P23/1N, P22/1N — Set to logic 0 (Active-LOW) at a LOW-to-HIGH transition in the input voltage on P23 and P22, respectively. Both are reset to logic 1 after the port information has been read.

P23/0N, P22/0N — As for P23/1N and P22/1N but are set to logic 0 at a HIGH-to-LOW transition.

PI23, PI22, PI21, PI20 — Indicate input voltage levels at P23, P22, P21 and P20, respectively. A logic 1 indicates a HIGH input level.

Reset

The programming to reset all registers is shown in Figure 5. Reset is activated only at data byte HEX 06. Acknowledge is generated at every byte, provided that CITAC is not in the power-down reset mode. After the general call address byte, transmission of more than one data byte is not allowed.

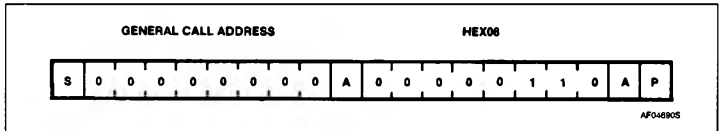


Figure 5. Reset Programming

I²C BUS TIMING (Figure 6)

I²C bus load conditions are as follows:

4kΩ pull-up resistor to +5V; 200pF capacitor to GND.

All values are referred to V_{IH} = 3V and V_{IL} = 1.5V.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
t_{BUF}	Bus free before start	4			μs
t_{SU}, t_{STA}	Start condition setup time	4			μs
t_{HD}, t_{STA}	Start condition hold time	4			μs
t_{LOW}	SCL, SDA LOW period	4			μs
t_{HIGH}	SCL HIGH period	4			μs
t_R	SCL, SDA rise time			1	μs
t_F	SCL, SDA fall time			0.3	μs
t_{SU}, t_{DAT}	Data setup time (write)	1			μs
t_{HD}, t_{DAT}	Data hold time (write)	1			μs
t_{SU}, t_{CAC}	Acknowledge (from CITAC) setup time			2	μs
t_{HD}, t_{CAC}	Acknowledge (from CITAC) hold time	0			μs
t_{SU}, t_{STO}	Stop condition setup time	4			μs
t_{SU}, t_{RDA}	Data setup time (read)			2	μs
t_{HD}, t_{RDA}	Data hold time (read)	0			μs
t_{SU}, t_{MAC}	Acknowledge (from master) setup time	1			μs
t_{HD}, t_{MAC}	Acknowledge (from master) hold time	2			μs

NOTE:

1. Timings t_{SU}, t_{DAT} and t_{HD}, t_{DAT} deviate from the I²C bus specification. After reset has been activated, transmission may only be started after a 50μs delay.

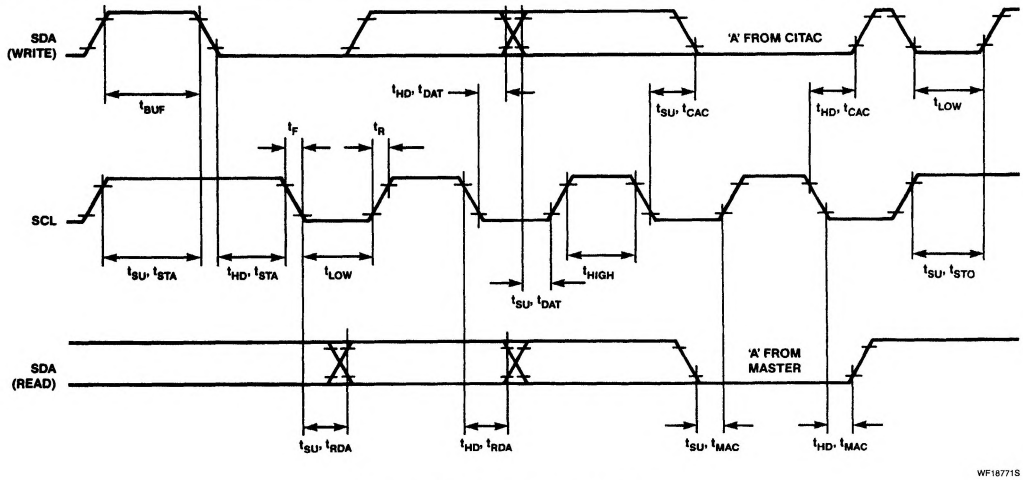


Figure 6. I^2C Bus Timing SAB3037