

DESCRIPTION

These monolithic, positive-edge-triggered flip-flops utilize TTL circuits to implement the D-type flip-flop logic. Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect.

These circuits are fully compatible for use with most TTL or DTL circuits. A full fan-out to 10 low logic-level loads and 20 high-logic-level loads is available from each of the outputs. This simplifies system design by allowing unused inputs to be tied to driven inputs. Maximum clock frequency is typically 25 megahertz, with a typical power dissipation of 38 milliwatts per flip-flop.

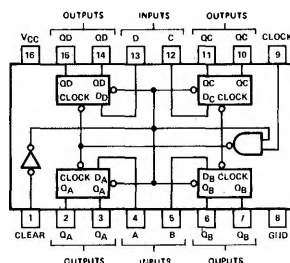
TRUTH TABLE

INPUT	OUTPUT
t_n	$t_n + 1$
D	Q
H	H
L	L

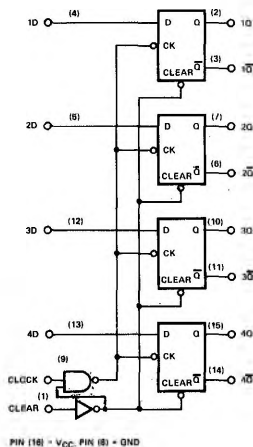
t_n = Bit time before clock pulse transition.
 $t_n + 1$ = Bit time after clock pulse transition.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	54175			74175			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High Logic Level			20			20
	Low Logic Level			10			
Input clock frequency, f _{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t _w (See Figure 1)	20			20			ns
Data setup time, t _{setup} (See Figure 1)	20			20			ns
Hold time t _{hold} (See Figure 1)	0			0			ns
Operating free-air temperature, T _A	-55	25	125	0	25	70	°C
Clear release setup, t _{release} (See Figure 1)	25			25			ns

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†	54175			74175			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	$V_{CC} = \text{MAX}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} \approx -800 \mu\text{A}$	2.4			2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.4			0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS}	Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$							
		Note 1		30	45		30	45	mA

§ Not more than one output should be started at a time.

NOTE 1: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$	Maximum input clock frequency	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output Q from clear	$C_L = 15\text{ pF}$ $R_L = 400$	23	35	ns
t_{PLH}	Propagation delay time low-to-high-level output Q from clear (54175, 74175)		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		20	30	ns

SWITCHING TIMES

