Signetics

PNA7509
7-Bit Analog-to-Digital Converter

Preliminary Specification

Linear Products

DESCRIPTION

The PNA7509 is a monolithic NMOS 7-bit analog-to-digital converter designed for video applications. The device converts the analog input signal into 7-bit binary coded digital words at a sampling rate of 22MHz.

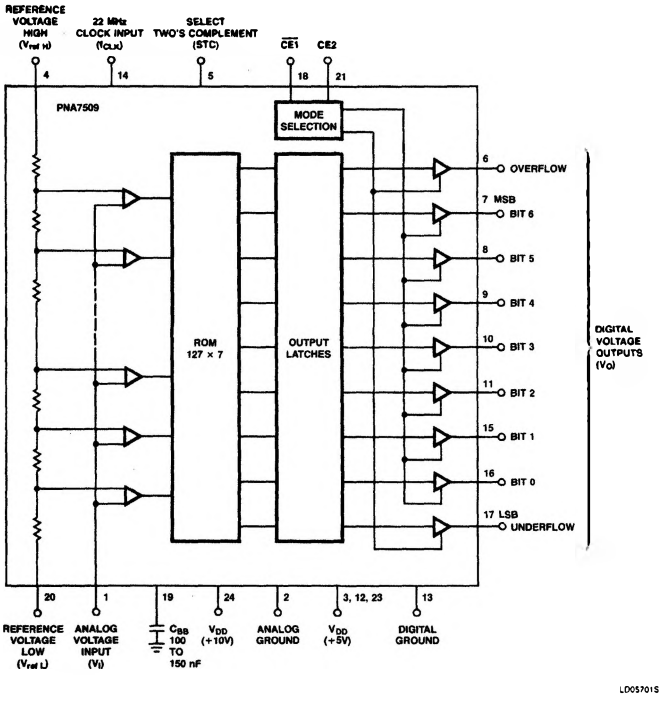
The circuit comprises 129 comparators, a reference resistor chain, combining logic, transcoder stages, and TTL output buffers which are positive edge-triggered and can be switched into 3-State mode. The digital output is selectable in two's complement or binary coding.

The use of separate outputs for overflow and underflow detection facilitates full-scale driving.

FEATURES

- **7-bit resolution**
- **22MHz clock frequency**
- **No external sample and hold required**
- **High input impedance**
- **Binary or two's complement 3-State TTL outputs**
- **Overflow and underflow 3-State TTL outputs**
- **Low reference current (250μA typ.)**
- **Positive supply voltages (+5V, +10V)**
- **Low power consumption (400mW typ.)**
- **Available in SO package**

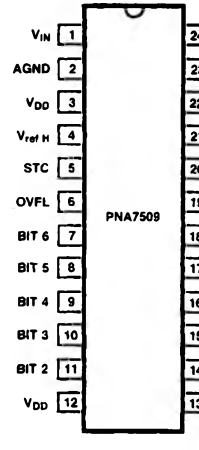
BLOCK DIAGRAM



NOTE:
Pins 3, 12, and 23 must be connected to positive supply voltage +5V.

PIN CONFIGURATION

D, N Packages



PIN NO.	SYMBOL	DESCRIPTION
1	V_{IN}	Analog voltage input
2	AGND	Analog ground
3	V_{DD}	Positive supply voltage (+5V)
4	V_{REFH}	Reference voltage High
5	STC	Select two's complement
6	OVFL	Overflow
7	Bit 6	Most significant bit (MSB)
8	Bit 5	
9	Bit 4	
10	Bit 3	
11	Bit 2	
12	V_{DD}	Positive supply voltage (+5V)
13	DGND	Digital ground
14	f_{CLK}	22MHz clock input
15	Bit 1	
16	Bit 0	Least significant bit (LSB)
17	UNFL	Underflow
18	$\overline{CE1}$	Chip enable input 1
19	V_{BB}	Back bias output
20	V_{REFL}	Reference voltage Low
21	CE2	Chip enable input 2
22	NC	Not connected
23	V_{DD}	Positive supply voltage (+5V)
24	V_{DD}	Positive supply voltage (+10V)

APPLICATIONS

- **High-speed A/D conversion**
- **Video signal digitizing**
- **Radar pulse analysis**
- **High energy physics research**
- **Transient signal analysis**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	0 to +70°C	PNA7509N
24-Pin Plastic SO (SOT-101)	0 to +70°C	PNA7509D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range (Pins 3, 12, 23)	7	V
V_{DD}	Supply voltage range (Pin 24)	12	V
V_{IN}	Input voltage range	7	V
I_{OUT}	Output current	5	mA
P_D	Power dissipation	1	W
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS $V_{DD} = V_{3, 12, 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $C_{BB} = 100nF$; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply					
V_{DD}	Supply voltage (Pins 3, 12, 23)	4.5		5.5	V
V_{DD}	Supply voltage (Pin 24)	9.5		10.5	V
I_{DD}	Supply current (Pins 3, 12, 23)		51	85	mA
I_{DD}	Supply current (Pin 24)		11	18	mA
Reference voltages					
V_{REFL}	Reference voltage Low (Pin 20)	2.4	2.5	2.6	V
V_{REFH}	Reference voltage High (Pin 4)	5.0	5.1	5.2	V
I_{REF}	Reference current	150		450	µA
Inputs					
	Clock input (Pin 14)				
V_{IL}	Input voltage Low	−0.3		0.8	V
V_{IH}	Input voltage High	3.0		5.5	V
	Digital input levels (Pins 5, 18, 21)*				
V_{IL}	Input voltage Low	0		0.8	V
V_{IH}	Input voltage High	2.0		5.5	V
	Input current				
$-I_5$	at $V_5 = 0V$; $V_{13} = GND$	15		70	µA
I_{18}	at $V_{18} = 5V$; $V_{13} = GND$	15		70	µA
	Input leakage current				
$-I_{21}$	at $V_{21} = 0V$; $V_{13} = GND$	25		120	µA
I_{LI}	Input leakage current (except Pins 5, 18, 21)			10	µA
	Analog Input levels (Pin 1)				
	at $V_{REFL} = 2.5V$; $V_{REFH} = 5.1V$				
$V_{IN\ P-P}$	Input voltage amplitude (peak-to-peak value)		2.6		V
V_{IN}	Input voltage (underflow)		2.5		V
V_{IN}	Input voltage (overflow)		5.1		V
$V_I - V_{REFL}$	Offset input voltage (underflow)		10		mV
$V_I - V_{REFH}$	Offset input voltage (overflow)		−10		mV
$C_{1, 2}$	Input capacitance			60	pF
Outputs					
	Digital voltage outputs (Pins 6 to 11 and 15 to 17)				
	Output voltage Low				
V_{OL}	at $I_O = 2mA$	0		−0.4	V
	Output voltage High				
V_{OH}	at $-I_O = 0.5mA$	2.4		5.5	V

*When Pin 5 is Low, binary coding is selected.
When Pin 5 is High, two's complement is selected.
If Pins 5, 18 and 21 are open-circuit, Pins 5, 21 are High and Pin 18 is Low.
For output coding, see Table 1; for mode selection, see Table 2.

AC ELECTRICAL CHARACTERISTICS

$V_{DD} = V_{3,\ 12,\ 23-13} = 4.5$ to 5.5V; $V_{DD} = V_{24-2} = 9.5$ to 10.5V; $V_{REFL} = 2.5$V; $V_{REFH} = 5.1$V; $f_{CLK} = 22$MHz; $C_{BB} = 100$nF; $T_A = 0$ to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Timing (see also Figure 1)					
	Clock input (Pin 14)				
f_{CLK}	clock frequency	1	25	22	MHz
t_{LOW}	clock cycle time Low	20			ns
t_{HIGH}	clock cycle time High	20			ns
	Input rise and fall times[1]				
t_R	rise time			3	ns
t_F	fall time			3	ns
	Analog input[1]				
BW	Bandwidth (−3 dB)	11	20		MHz
dG	Differential gain				
	at $f_I = \leqslant 4.5$MHz[2]		±3	±5	%
dp	Differential phase				
	at $f_I = \leqslant 4.5$MHz[2]		±1	±2.5	deg
P_E	Phase error				
	at $f_I = \leqslant 4.5$MHz[3]		10	±12	deg
S/N	Signal-to-noise ratio (non-harmonic noise)		−40	−36	dB
	Peak error			3	LSB
	Harmonics (full-scale)				
f_0	Fundamental			0	dB
$f_{2,\ 3}$	2nd and 3rd harmonics		−31	−28	dB
f_{4-7}	4th +5th +6th +7th harmonics		−39	−35	dB
	Digital outputs[2, 4]				
t_{HOLD}	Output hold time	6			ns
t_D	Output delay time $C_L = 15$pF			38	ns
	Output delay time $C_L = 50$pF			48	ns
t_{CY}	Internal delay		3		clocks
t_{DT}	3-State delay time (see Figure 2)			25	ns
C_{OL}	Capacitive output load	0		15	pF
	Transfer function				
	Non-linearity at $f_I = 1.1$kHz				
INL	integral		±1/4	±1/2	LSB
DNL	differential		±1/3	±1/2	LSB

NOTES:

1. Clock input rise and fall times are at the maximum clock frequency (10% and 90% levels).
2. Low frequency sine wave (peak-to-peak value of the analog input voltage at $V_{IN} = 1.8$V) amplitude modulated with a sine wave voltage ($V_{IN} = 0.7$V) at $f_I = 5$MHz.
3. Sine wave voltage with increasing amplitude at $f_I = 5$MHz (minimum amplitude $V_{IN} = 0.25$V; maximum amplitude $V_{IN} = 2.5$V).
4. The timing values of the digital output Pins 6 to 11 and 15 to 17 are measured with the clock input reference level at 1.5V.

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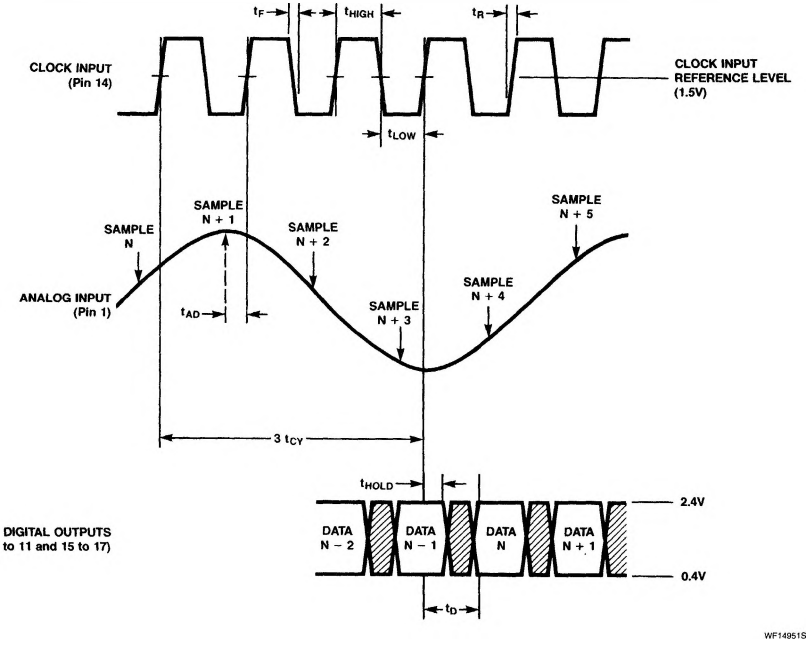
Table 1. Output Coding (V_{REFL} = 2.5V; V_{REFH} = 5.1V)

STEP	$V_{1,2}$ (Typ)	UNFL	OVFL	BINARY Bit 6 – Bit 0	TWO's COMPLEMENT Bit 6 – Bit 0
Underflow	< 2.51	1	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
0	2.51	0	0	0 0 0 0 0 0 0	1 0 0 0 0 0 0
1	2.53	0	0	0 0 0 0 0 0 1	1 0 0 0 0 0 1
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
•	•	•	•	• • • • • • •	• • • • • • •
126	5.03	0	0	1 1 1 1 1 1 0	0 1 1 1 1 1 0
127	5.05	0	0	1 1 1 1 1 1 1	0 1 1 1 1 1 1
Overflow	⩾ 5.07	0	1	1 1 1 1 1 1 1	0 1 1 1 1 1 1

Table 2. Mode Selection

CE1	CE2	BIT 0 to BIT 6	UNFL, OVFL
X	0	High-impedance	High-impedance
0	1	Active	Active
1	1	High-impedance	Active



NOTE:
There is a delay of 3 clock cycles between sampling of an analog input signal and the corresponding digital output.

Figure 1. Timing Diagram

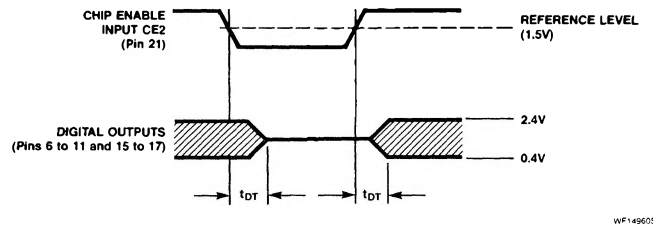


Figure 2. Timing Diagram for 3-State Delay

APPLICATION INFORMATION

The minimum and maximum values provided in the data sheet are guaranteed over the whole voltage and temperature range. This note gives additional information to the data sheet where the typical values indicate the behavior under nominal conditions; V_{DD5} = 5V, V_{DD10} = 10V, T_A = 22°C.

SYMBOL	PARAMETER	TYP	UNIT
I_{DD5}	Supply current (Pins 3, 12, 23)	51	mA
I_{DD10}	Supply current (Pin 24)	11	mA
f_{CLK}	Maximum clock frequency	25	MHz
B	Bandwidth (–3dB)	20	MHz
P_D	Total power dissipation	365	mW
	Peak error (non-harmonic noise)	1.5	LSB
	Suppression of harmonics sum of:		
$f_{2,3}$	$f_{2nd} + f_{3rd}$	31	dB
f_{4-7}	$f_{4th} + f_{5th} + f_{6th} + f_{7th}$	39	dB
	Non-linearity		
INL	integral	± ¼	LSB
DNL	differential	± ⅓	LSB
D_G	Differential gain	± 3	%
D_P	Differential phase	± 1	%
P_e	Large-signal phase error	10	deg
S/N	Signal-to-noise ratio (non-harmonic noise)	–40	dB

NOTE:
1. Typical values are measured on sample base.

Application Recommendation

- Spikes at the 10V supply input have to be avoided (e.g., overshoots during switching). Even a spike duration of less than 1µs can destroy the device.

Test Philosophy

Figure 3 is a block diagram showing analog-to-digital testing with a phase-locked signal source. The signal generator provides a 5MHz sine wave for the device under test (except for the linearity test). The 22MHz clock input is provided by the clock generator.

The phase relationship between signal and clock generator is shifted by 100ps each signal period to provide an effective clock rate of 10GHz for analysis.

Most calculations are carried out in the spectral domain using Fast Fourier Transformation (FFT) and the inverse FFT to return to time domain.

The successive processing completes the specific measurement (Figures 4, 5, 6, and 7).

The non-linearities of the converter, integral (INL) and differential (DNL), are measured using a low frequency ramp signal. Within a general uncertain range of conversion between two steps, the output signal of the converter randomly switches.

After low-pass filtering, the different step width is used for calculating the line of least squares to obtain integral non-linearity.

To calculate differential non-linearity, a counter is used to count the frequency of each step. A histogram is calculated from the counter result to provide the basis for further computation (Figure 6).

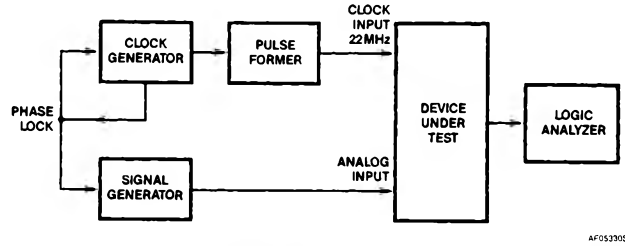
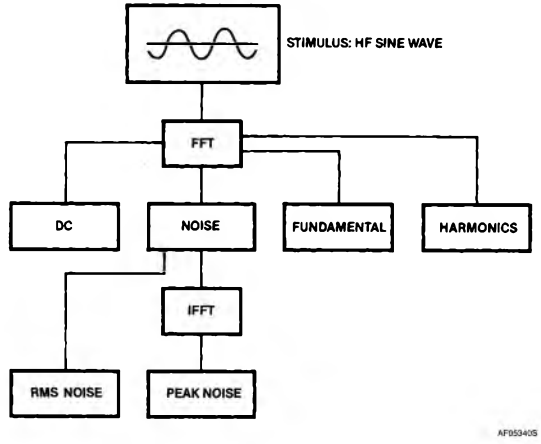


Figure 3. Analog-to-Digital Converter Testing with Phase-Locked Signal Source



Where: FFT = Fast Fourier Transformation.
IFFT = Inverse Fast Fourier Transformation.

Figure 4. Sine Wave Test; Non-Harmonic Noise and Peak Error

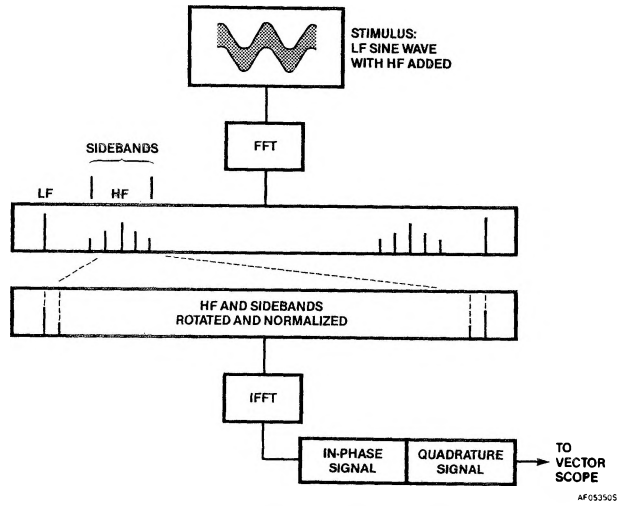
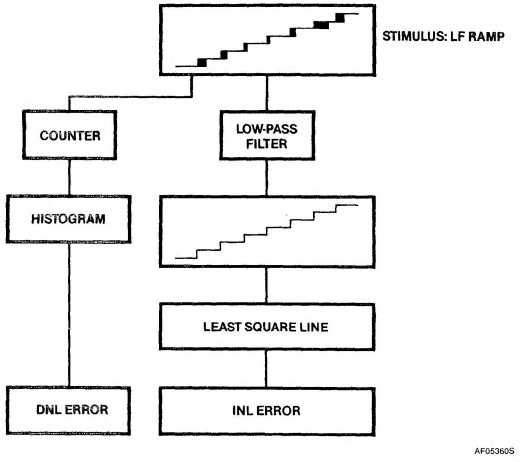


Figure 5. Differential Gain and Phase



Where: INL = Integral Non-Linearity.
DNL= Differential Non-Linearity.

Figure 6. Low Frequency Ramp Test; Linearity

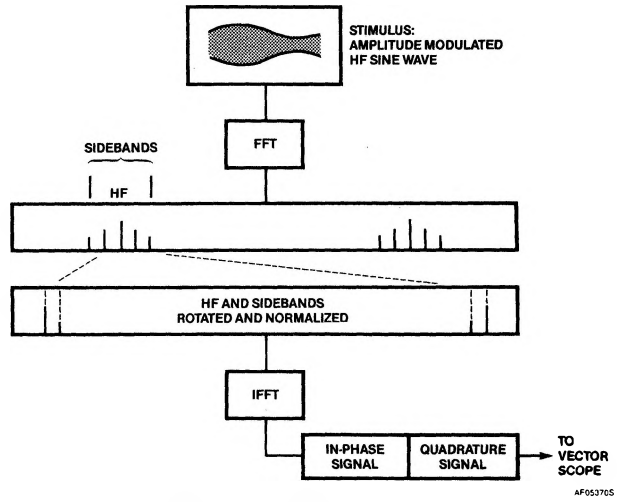


Figure 7. Large-Signal Phase Error

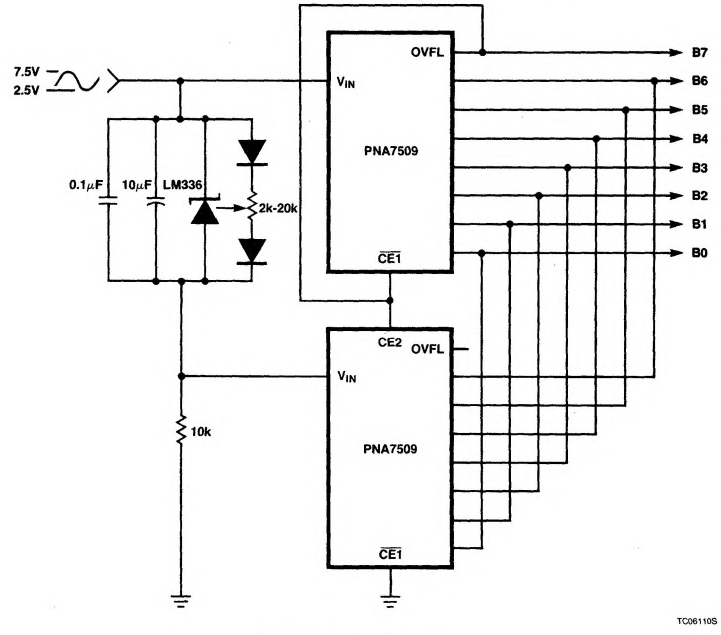


Figure 8. 8-Bit Resolution