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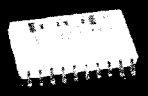

PCM1714U

ADVANCED INFORMATION
SUBJECT TO CHANGE

Dual Voltage Output, CMOS Delta-Sigma DIGITAL-TO-ANALOG CONVERTER

FEATURES

- NEW MULTI-LEVEL NOISE-SHAPING ARCHITECTURE
- HIGH PERFORMANCE:
  THD+N: 0.0015% typ
  S/N RATIO: 104dB typ
  DYNAMIC RANGE: 102dB typ
- DUAL CO-PHASE ANALOG VOLTAGE OUTPUT: 2.8Vp-p
- SELECTABLE 18-BIT/20-BIT INTERFACE
- VERSATILE SYSTEM CLOCK
- TTL LEVEL INPUT INTERFACE
- 5V SINGLE POWER SUPPLY
- LOW POWER DISSIPATION
- SMALL 20-PIN SOIC PACKAGE

DESCRIPTION

The PCM1714U is dual voltage output CMOS Delta-Sigma high performance DAC which is combined with a new Multi-Level Noise-shaping architecture and voltage output amplifier.

This new architecture and internal output amplifier in the PCM1714U provides a clean analog output signal with lower jitter and lower RFI sensitivity than the typical 1-bit DAC.

The PCM1714U accepts 18-bit or 20-bit, MSB first, serial data (Lch/Rch parallel). The PCM1714U does not use forced mute by zero detection which is used by typical 1-bit DAC. The PCM1714U offers very low noise and linear D/A conversion in demanding situations such as fade out signal on electronic piano or music instruments.

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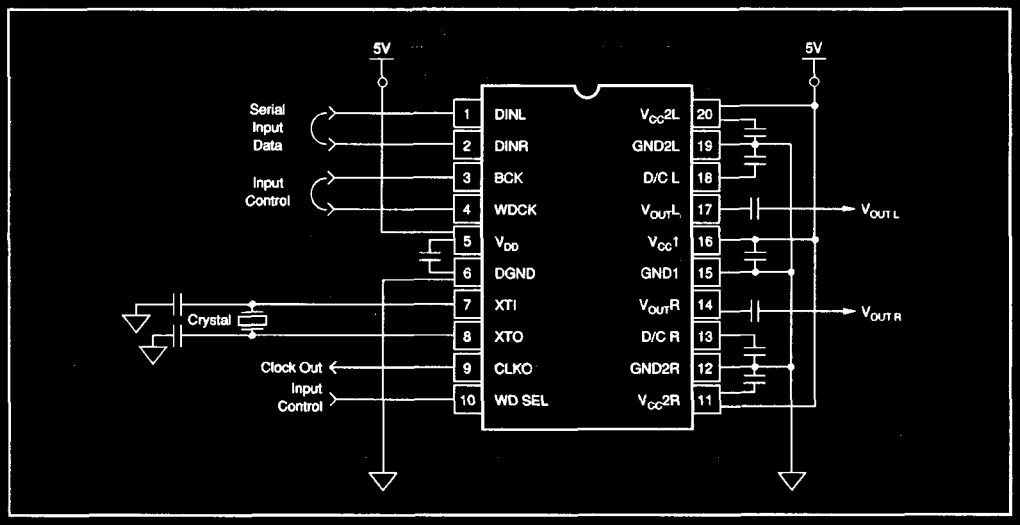
SPECIFICATIONS

ELECTRICAL

At +25°C, $+V_{CC} = +V_{DD} = +5V$, fs = 44.1kHz, 20-bit data, SYSCLK = 256fs, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1714U MIN	PCM1714U TYP	PCM1714U MAX	UNITS
RESOLUTION		18		20	Bits
DIGITAL INPUT/OUTPUT					
Input Logic Level (except XTI)					
V_{IH}		2.0			VDC
V_{IL}				+0.8	VDC
Input Logic Current (except XTI)					
I_I				–200	µA
Input Logic Level (XTI)					
V_{IH}		3.2			VDC
V_{IL}				1.4	VDC
Input Logic Current (XTI)					
I_I				±50	µA
Output Logic Level (CLKO)					
V_{OH}		4.5			VDC
V_{OL}				0.2	VDC
Output Logic Current: I_O		±10			mA
Data Bit		18-Bit/20-Bit Selectable			
Sampling Frequency		1	44.1		kHz
System Clock Frequency		100k	11.2896M	20M	Hz
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mis-match Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	$V_O = 1/2V_{CC}$ at Bipolar Zero		±20		mV
Gain Drift			±50		ppm of FSR/°C
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE					
Effective Bandwidth			SYSCLK/564		Hz
THD+N at F/S (0dB)	f_{IN} = 991Hz		–96		dB
Dynamic Range	EIAJ A-weighted		102		dB
S/N Ratio	EIAJ A-weighted		104		dB
Channel Separation	f_{IN} = 991Hz		94		dB
ANALOG OUTPUT					
Voltage Range	F/S (0dB) OUT		2.8		Vp-p
Load Impedance		5k			Ω
Center Voltage			$\pm 1/2V_{CC}$		V
POWER SUPPLY REQUIREMENTS					
Voltage Range: $+V_{CC}$		+4.5	+5.0	+5.5	VDC
$-V_{DD}$		+4.5	+5.0	+5.5	VDC
Supply Current: $+I_{CC}+I_{DD}$	$+V_{CC} = +V_{DD} = +5.0V$		25		mA
Power Dissipation	$+V_{CC} = +V_{DD} = +5.0V$		125		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

CONNECTION DIAGRAM



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	DINL	Data Input, Lch
2	DINR	Data Input, Rch
3	BCK	Bit Clock Input
4	WDCK	Word Clock Input
5	V_{DD}	Digital Power Supply (+5V)
6	DGND	Digital Ground
7	XTI	Oscillator Input (External Clock Input)
8	XTO	Oscillator Output
9	CLKO	Buffered Output of Oscillator
10	WD SEL	Word Select Input (18-Bit/20-Bit)
11	$V_{CC}2R$	Analog (DAC) Power Supply (+5V), Rch
12	GND2R	Analog (DAC) Ground, Rch
13	D/C R	DeCoupling, Rch
14	$V_{OUT}R$	Rch Analog Output
15	GND1	Analog Ground
16	$V_{CC}1$	Analog Power Supply (+5V)
17	$V_{OUT}L$	Lch Analog Output
18	D/C L	De Coupling, Lch
19	GND2L	Analog (DAC) Ground, Lch
20	$V_{CC}2L$	Analog (DAC) Power Supply (+5V), Lch

NOTES: (1) XTO (Pin 8) must be open when the external clock enter to XTI (Pin 7). (2) All input pins are with pull up resistor.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
PCM1714U	20-Pin SOIC	248

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

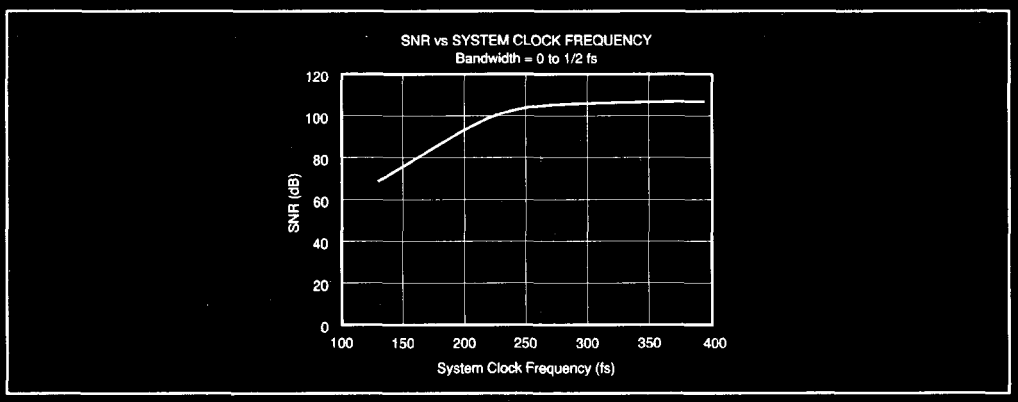
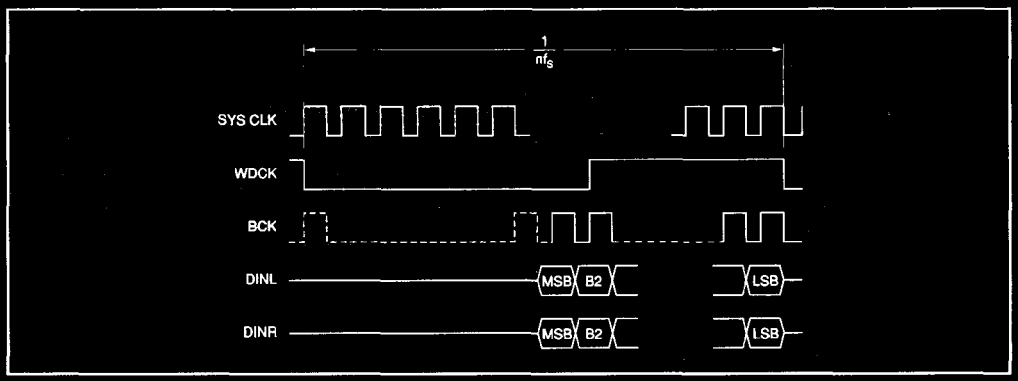


FIGURE 1. System Clock Frequency.

TIMING DIAGRAM



INPUT TIMING CONDITIONS

fs: 32kHz – 48kHz

n: Integer 1 – 8 (capable from 1fs to 8fs input)

SYSCLK: 8 *m* • *nfs* (*fmax* 20MHz)

m: Integer

BCK: More than number of input data bit (fmax 10MHz)

DINL (R): 16-Bit or 20-Bit MSB first, right justified

Example 1: fs = 44.1kHz input

SYSCLK = 8m • fs

if m = 48, *then* SYSCLK is calculated as SYCSLK = 8 x 48 x fs = 384fs
= 16.934MHz

if m = 32, then SYSCLK is calculated as SYCSLK = 8 x 32 x fs = 256fs
= 11.2896MHz

In above conditions, PCM1714 can be operated with both 384fs or 256fs, or any other system clock which will keep above timing conditions.

Example 2: 8 time over sampling (8fs) input

SYSCLK = 8m • 8fs

if m = 6, then SYSCLK is calculated as SYCSLK = 8 x 6 x 8fs = 384fs
= 16.9344MHz

if m = 8, then SYSCLK is calculated as SYCSLK = 8 x 8 x 8fs = 512fs
= 22.579MHz

In above conditions, PCM1714 can be operated with both 384fs but not 512fs since the system clock frequency at 512fs will exceed the max conditions of PCM1714 system clock (20MHz).

NOTE: SYSCLK > 256fs is recommended to obtain optimized SNR performance. See Figure 1 for the relation of SYSCLK vs SNR.