DATA SHEET

PCK857

66–150MHz Phase Locked Loop
Differential 1:10 SDRAM Clock Driver

Preliminary specification

1998 Dec 10

Philips
Semiconductors

PHILIPS

66–150MHz Phase Locked Loop Differential 1:10 SDRAM Clock Driver

PCK857

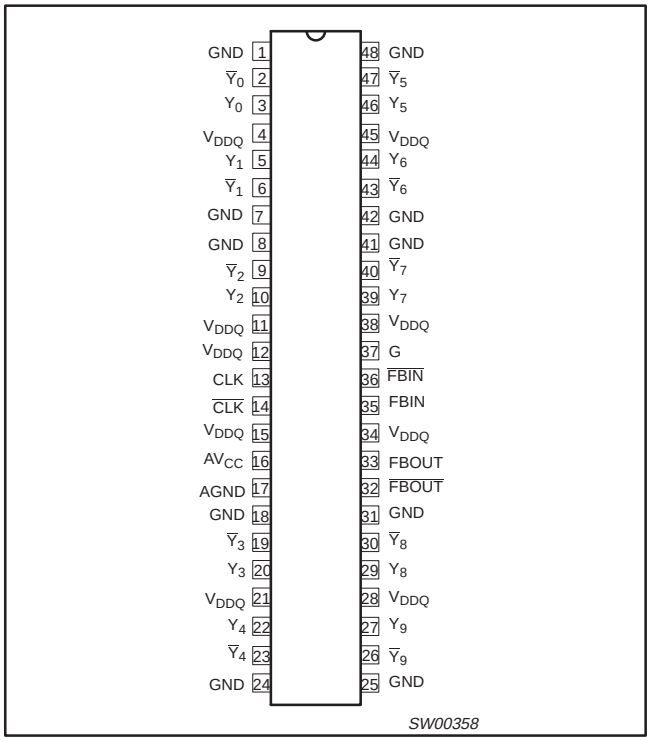
FEATURES

- Optimized for clock distribution in DDR (Double Data Rate) SDRAM applications
- 1-to-10 differential clock distribution
- Very low skew (< 100ps) and jitter (< 100ps)
- 3V AV_{CC} and 2.5V V_{ddq}
- SSTL_2 interface clock inputs and outputs
- CMOS control signal input
- Test mode enables buffers while disabling PLL
- Low current power-down mode
- Tolerant of Spread Spectrum input clock
- Full DDR solution provided when used with SSTL16857 and CBT3857

DESCRIPTION

Zero delay buffer to distribute an SSTL differential clock input pair to 10 SSTL_2 differential output pairs. Outputs are slope controlled. External feedback pin for synchronization of the outputs to the input. A CMOS style Enable/Disable pin is provided for low power disable.

PIN CONFIGURATION



ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
48-Pin Plastic TSSOP	0°C to +70°C	PCK857 DGG	PCK857 DGG	SOT362-1

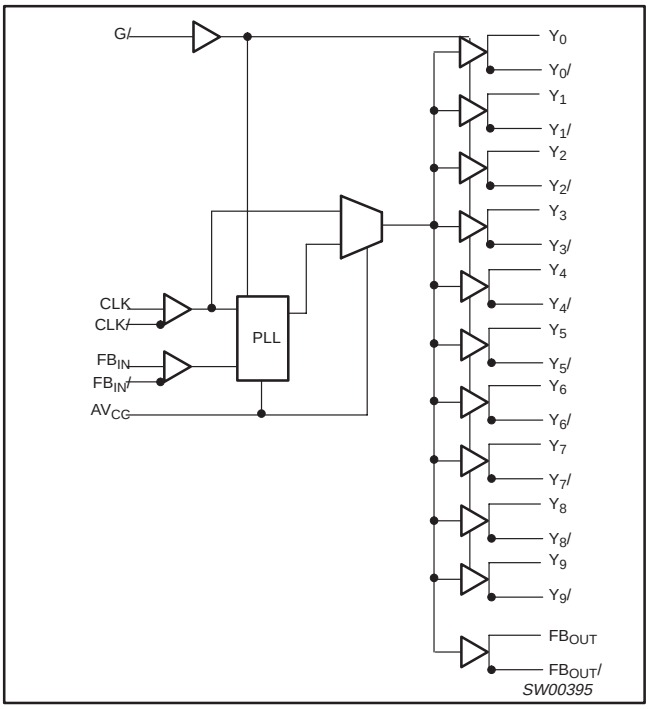
PINS	SYMBOL	DESCRIPTION
1, 7, 8, 18, 24, 25, 31, 41, 42, 48	GND	SSTL_2 ground pins
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 32, 33, 39, 40, 43, 44, 46, 47	Y_n, Y_{nb}, FB_{OUT}, FB_{OUTb}	SSTL_2 differential outputs
4, 11, 12, 15, 21, 28, 34	V_{DDQ}	SSTL_2 power pins
13, 14, 35, 36	CLK_{IN}, CLK_{INb}, FB_{IN}, FB_{INb}	SSTL_2 differential inputs
16	AV_{CC}	Analog power
17	AGND	Analog ground
37	G	Power-down control input

FUNCTION TABLE

INPUTS			OUTPUTS				PLL ON/OFF
G	CLK	$\overline{CLK}$	Y	$\overline{Y}$	FBOUT	FBOUT	
L	L	H	Z	Z	Z[1]	Z[1]	OFF
L	H	L	Z	Z	Z[1]	Z[1]	OFF
H	L	H	L	H	L	H	ON
H	H	L	H	L	H	L	ON
X[2]	< 20MHz	< 20MHz	Z	Z	Z[1]	Z[1]	OFF

NOTES:
H = HIGH voltage level
L = LOW voltage level
Z = high impedance OFF-state
X = don't care
1. Subject to change. May cause conflict with FBIN pins.
2. Additional feature that senses when the clock input is less than 20MHz and places the part in sleep mode.

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
AV_{CC}	Analog supply voltage		3	3.3	3.6	V
V_{DDQ}	I/O supply voltage		2.3	2.5	2.7	V
V_{IL}	Input low voltage		–0.3		V_{ref} –0.35	V
V_{IH}	Input high voltage		V_{ref} + 0.35		V_{ddq} + 0.3	V
V_{OL}	Output low voltage[1]		0		0.5	V
V_{OH}	Output high voltage[1]		2		V_{ddq}	V

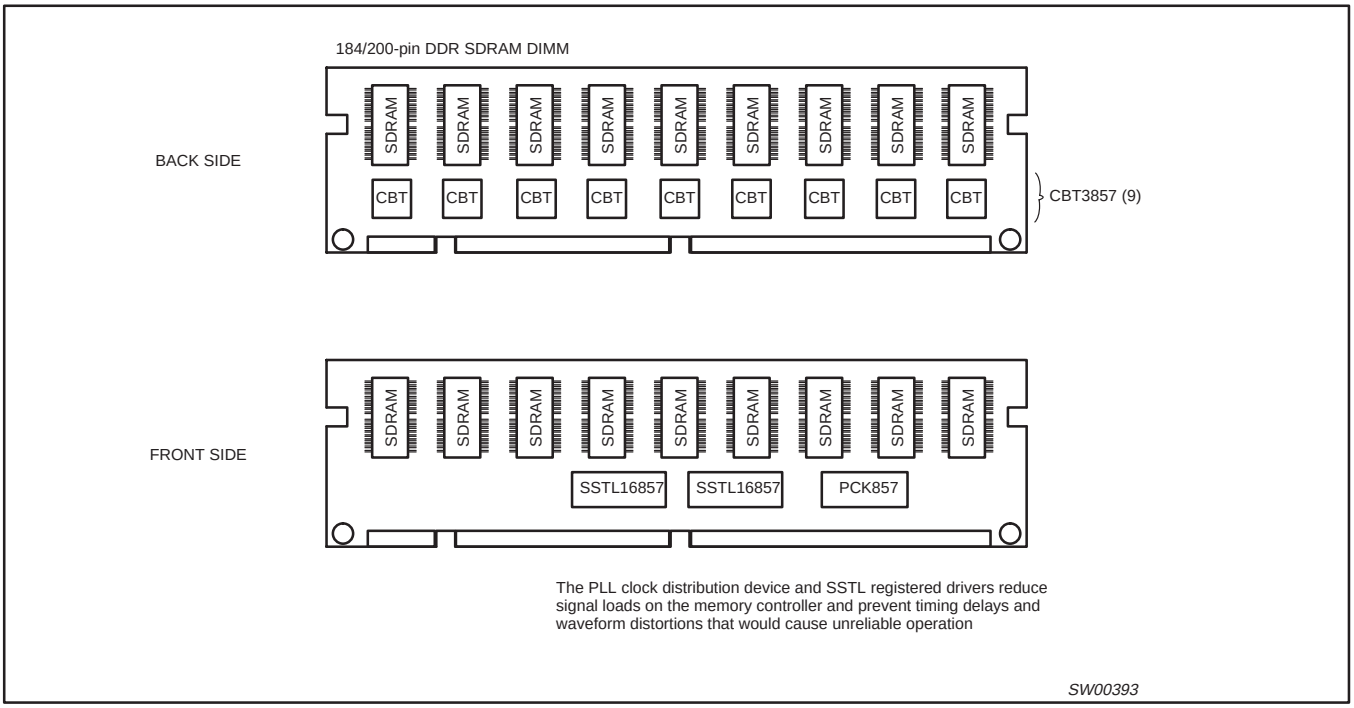
NOTE:
1. This is intended to operate in the SSTL_2 type IV unterminated mode without series resistors on the outputs.

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1K\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS			UNIT
				MIN	TYP	MAX	
f_{CK}	Clock frequency			50	133	150	MHz
$f_{PHASERROR}$	Phase error			–150	0	150	ps
f_{SK}	Output clock skew					200	ps
$fdif_{SK}$	Differential clock skew					100	ps
f_{SL}	Output clock skew			1	1.5		V/ns
$Jitter_{pp}$	Peak-to-Peak jitter (long term)			–100		100	ps
$Jitter_{cc}$	Cycle-to-cycle jitter (short term)			> –100		< 100	ps
O/P impedance	Inherent series resistance				25		Ω
f_{DC}	Duty cycle			45		55	%
C_{in}	Input capacitance			2.5		4	pF
Sync time						100	µs

NOTE:
1. Rise and fall



AC WAVEFORMS

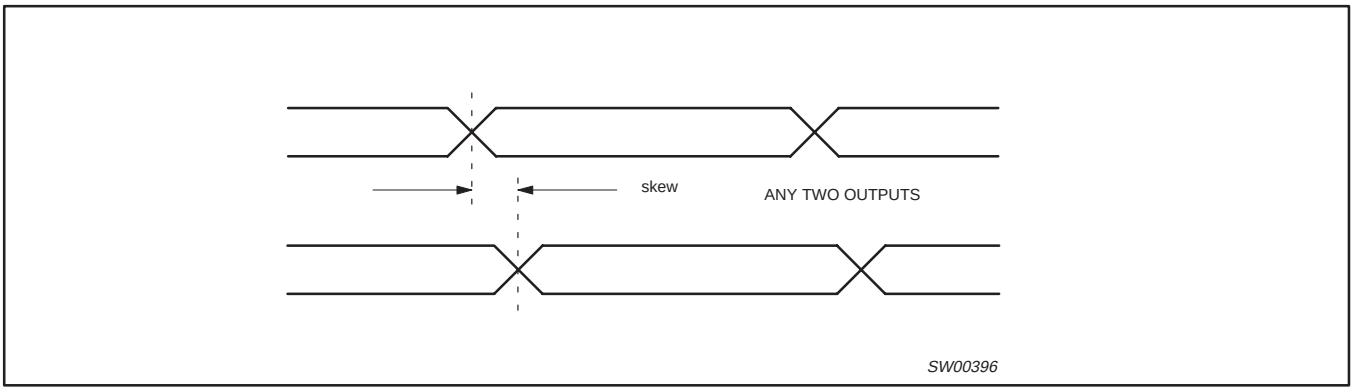


Figure 1. Skew between any two outputs.

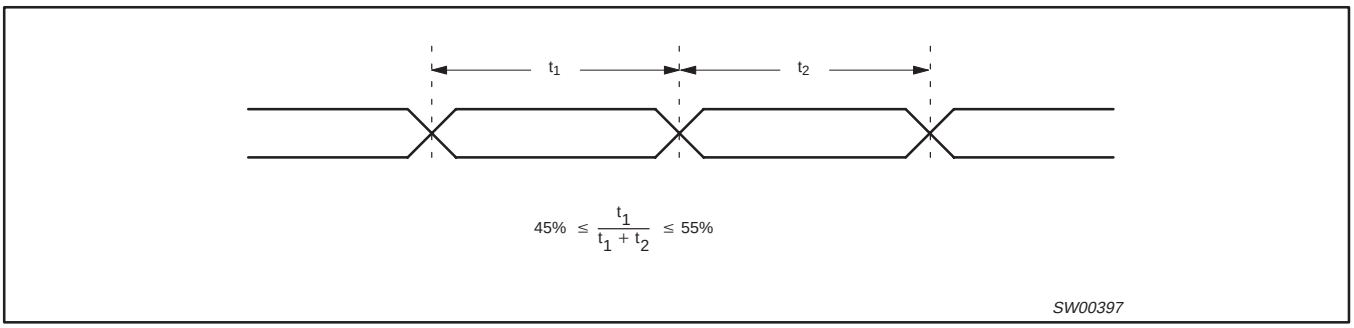


Figure 2. Duty cycle limits and measurement

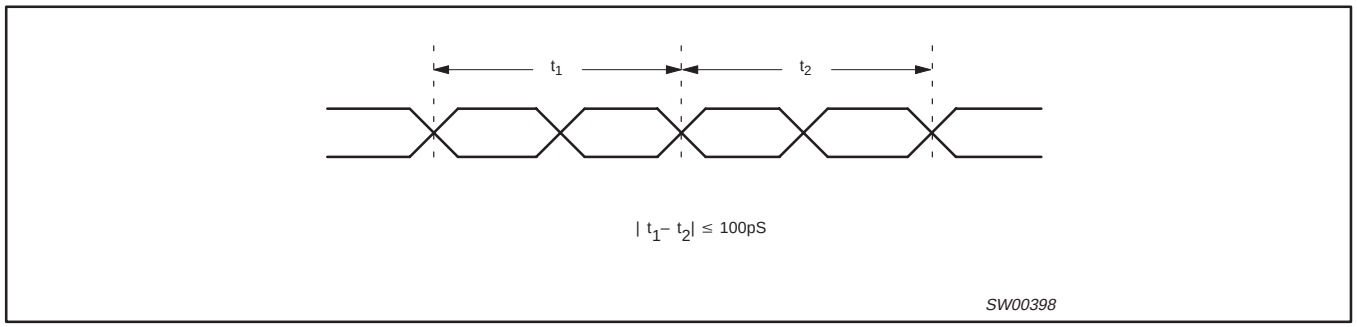
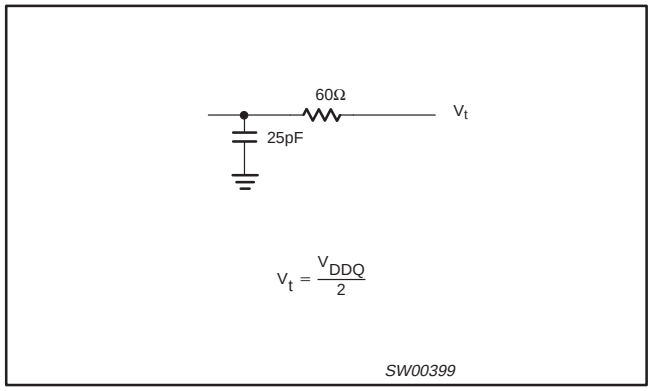
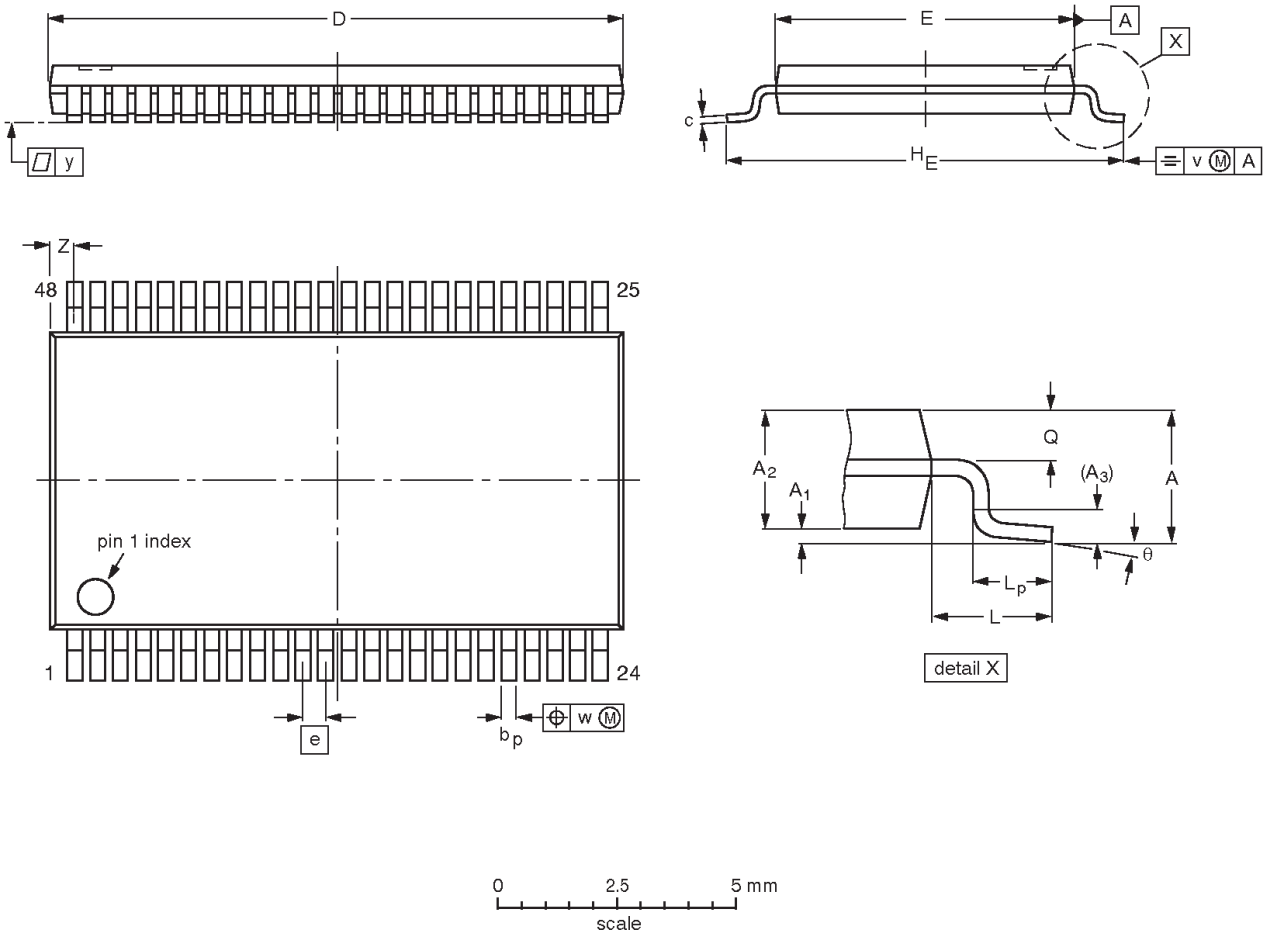


Figure 3. Jitter limit and measurement

TEST CIRCUIT



TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm SOT362-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

66–150MHz Phase Locked Loop Differential 1:10 SDRAM Clock Driver

PCK857

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

Date of release: 12-98

Document order number: 9397-750-04949

Let's make things better.

Philips Semiconductors

PHILIPS