Signetics

PCF8591
8-Bit A/D and D/A Converter

Objective Specification

Linear Products

DESCRIPTION

The PCF8591 is a single-chip, single-supply, low power 8-bit CMOS data acquisition device. It contains an 8-bit successive approximation analog to digital converter, a four channel analog multiplexer and a digital to analog converter. The four analog inputs can be programmed as two differential inputs or four single-ended inputs. PCF8591 has a serial I^2C interface which allows for a maximum bus frequency of 100k bits per second.

FEATURES

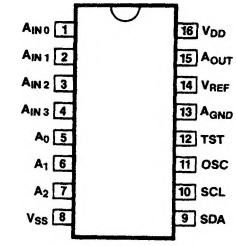
- **Single power supply**
- **Operating voltage 2.5V to 6V**
- **Low power consumption**
- **Serial I^2C bus**
- **Four analog inputs programmable as two differential or four single-ended**
- **On-chip sample-and-hold**
- **Auto-incremented channel selection**
- **8-bit successive approximation A/D conversion**
- **Multiplying DAC with one analog output**

APPLICATIONS

- **Control systems**
- **Low power converter for remote data acquisition**
- **Automotive**
- **Audio and TV**

PIN CONFIGURATION

D and N Packages



TOP VIEW

CD01381S

PIN NO.	SYMBOL	DESCRIPTION
1	A_{IN0}	Analog input (A/D converter)
2	A_{IN1}	Analog input (A/D converter)
3	A_{IN2}	Analog input (A/D converter)
4	A_{IN3}	Analog input (A/D converter)
5	A_0	Hardware address pin
6	A_1	Hardware address pin
7	A_2	Hardware address pin
8	V_{SS}	Negative supply
9	SDA	I^2C Bus data line
10	SCL	I^2C Bus clock line
11	OSC	Oscillator
12	EXT	External/internal switch for oscillator output
13	A_{GND}	Analog ground (reference ground)
14	V_{REF}	Reference voltage
15	A_{OUT}	Analog output (D/A converter)
16	V_{DD}	Positive supply

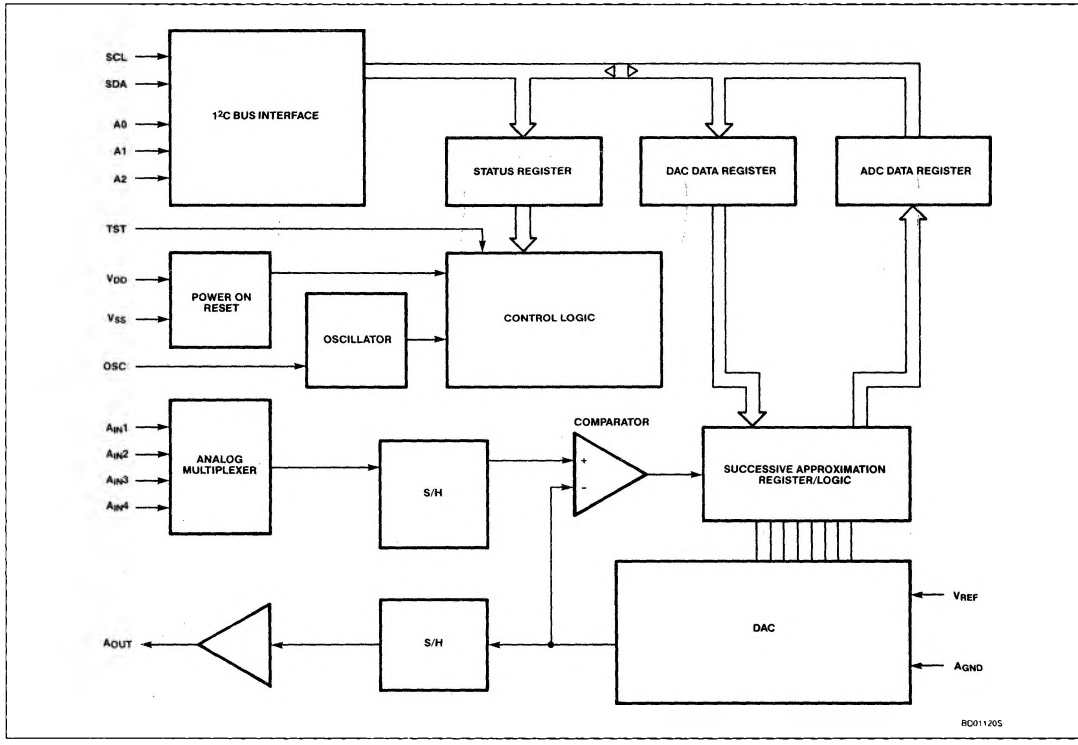
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to 85°C	PCF8591PN
16-Pin Plastic SO package	−40°C to 85°C	PCF8591TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +8.0	V
V_I	Voltage on any pin	−0.5 to V_{DD} +0.5	V
I_I	Input current DC	10	mA
I_O	Output current DC	20	mA
I_{DD}, I_{SS}	V_{DD} or V_{SS} current	50	mA
P_{TOT}	Power dissipation per package	300	mW
P_D	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5V to 6V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Supply						
V_{DD}	Supply voltage	Operating	2.5		6.0	V
I_{DD0}	Supply current	Standby $V_I = V_{SS}$ or V_{DD}; no load			15	μA
I_{DD1}	Supply current	Operating A_{OUT} off, f_{SCL} = 100kHz		125	250	μA
I_{DD2}	Supply current	A_{OUT} active, f_{SCL} = 100kHz		0.45	1.0	mA
V_{POR}	Power-on reset level[1]		0.8		2.0	V
Digital inputs/output SCL, SDA, A0, A1, A2						
V_{IL}	Input voltage	LOW	0		0.3 × V_{DD}	V
V_{IH}	Input voltage	HIGH	0.7 × V_{DD}		V_{DD}	V
I_I	Input current	Leakage $V_I = V_{SS}$ to V_{DD}			250	nA
C_I	Input capacitance				5	pF
I_{OH}	SDA output current	Leakage HIGH at $V_{OH} = V_{DD}$			250	nA
I_{OL}	SDA output current	LOW at V_{OL} = 0.4V	3.0			mA
Reference voltage inputs V_{REF}, A_{GND}						
V_{REF}	Voltage range	Reference	V_{AGND}		V_{DD}	V
V_{AGND}	Voltage range	Analog ground	V_{SS}		V_{REF}	V
I_I	Input current	Leakage			250	nA
R_{REF}	Input resistance	V_{REF} to A_{GND}		100		kΩ
Oscillator OSC, EXT						
I_I	Input current	Leakage			250	nA
f_{OSC}	Oscillator frequency		0.75		1.25	MHz

D/A CHARACTERISTICS V_{DD} = 5.0V; V_{SS} = 0V; V_{REF} = 5.0V; V_{AGND} = 0V; R_L = 10kΩ; C_L = 100pF; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Analog output						
V_{OA}	Output voltage range	No resistive load	V_{SS}		V_{DD}	V
V_{OA}	Output voltage range	R_L = 10kΩ	V_{SS}		0.9 V_{DD}	V
I_{LO}	Output current	Leakage A_{OUT} disabled			250	nA
Accuracy						
OS_e	Offset error	T_A = 25°C			50	mV
L_e	Linearity error				±1.5	LSB
G_e	Gain error	No resistive load			1	%
t_{DAC}	Settling time	To ½LSB full-scale step			90	μs
f_{DAC}	Conversion rate				11.1	kHz
SNRR	Supply noise rejection ratio	At f = 100Hz; V_{DD} = 0.1V_{P-P}		40		dB

A/D CHARACTERISTICS V_{DD} = 5.0V; V_{SS} = 0V; V_{REF} = 5.0V; V_{AGND} = 0V; R_{SOURCE} = 10kΩ; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Analog inputs						
V_{IA}	Input voltage range		V_{SS}		V_{DD}	V
I_{IA}	Input current	Leakage			100	nA
C_{IA}	Input capacitance			10		pF
C_{ID}	Input capacitance	Differential		10		pF
V_{IS}	Single-ended voltage	Measuring range	V_{AGND}		V_{REF}	V
V_{ID}	Differential voltage	Measuring range; $V_{FS} = V_{REF} - V_{AGND}$	$\frac{-V_{FS}}{2}$		$\frac{+V_{FS}}{2}$	V
Accuracy						
OS_e	Offset error	T_A = 25°C			20	mV
L_e	Linearity error				±1.5	LSB
G_e	Gain error				1	%
GS_e	Gain error	Small-signal ΔV_{IN} = 16LSB			5	%
CMRR SNRR	Common-mode rejection ratio Supply noise rejection	At f = 100Hz; $V_{DDN} = 0.1V_{P-P}$		60 40		dB dB
t_{ADC}	Conversion time				90	μs
f_{ADC}	Sampling/conversion rate				11.1	kHz

NOTE:
1. The power-on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.

FUNCTIONAL DESCRIPTION

Addressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be set as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figures 1 and 8).

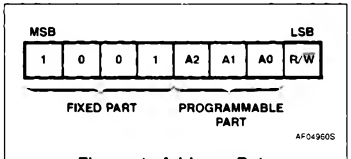


Figure 1. Address Byte

Control Byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Figure 2). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will always be channel 0. After a power-on reset condition, all bits of the control register are reset to 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high impedance state.

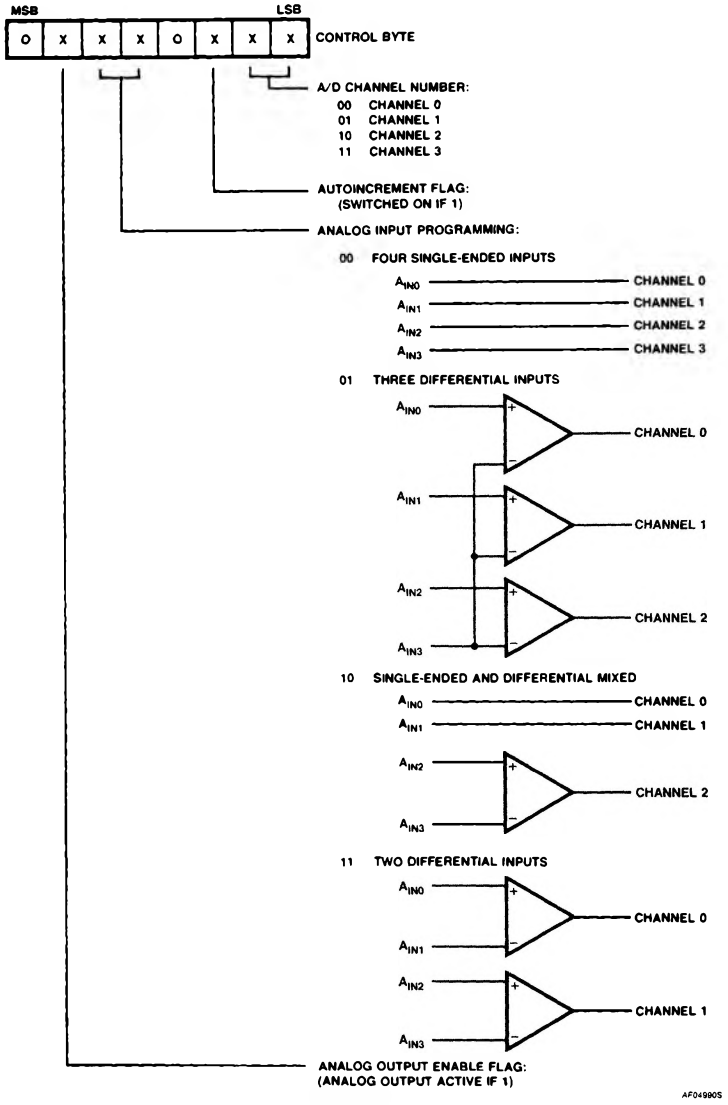


Figure 2. Control Byte

D/A Conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analog voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap decoder switches one of these taps to the DAC output line (see Figure 3).

The analog output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analog output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle, the unity gain amplifier is equipped with a track-and-hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analog output A_{OUT} is given by the formula shown in Figure 4. The waveforms of a D/A conversion sequence as shown in Figure 5.

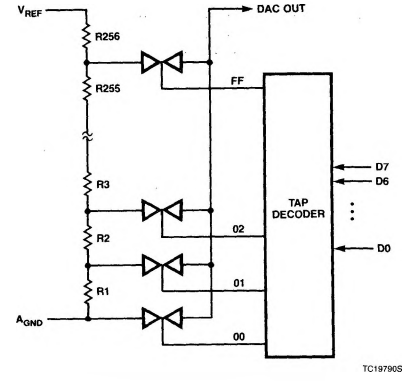


Figure 3. DAC Resistor Divider Chain

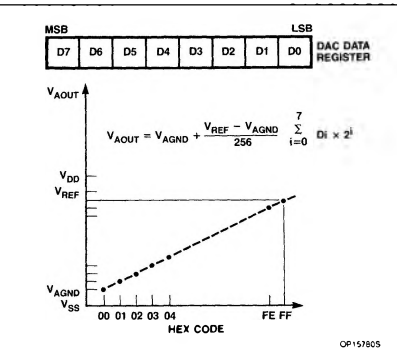


Figure 4. DAC Data and DC Conversion Characteristics

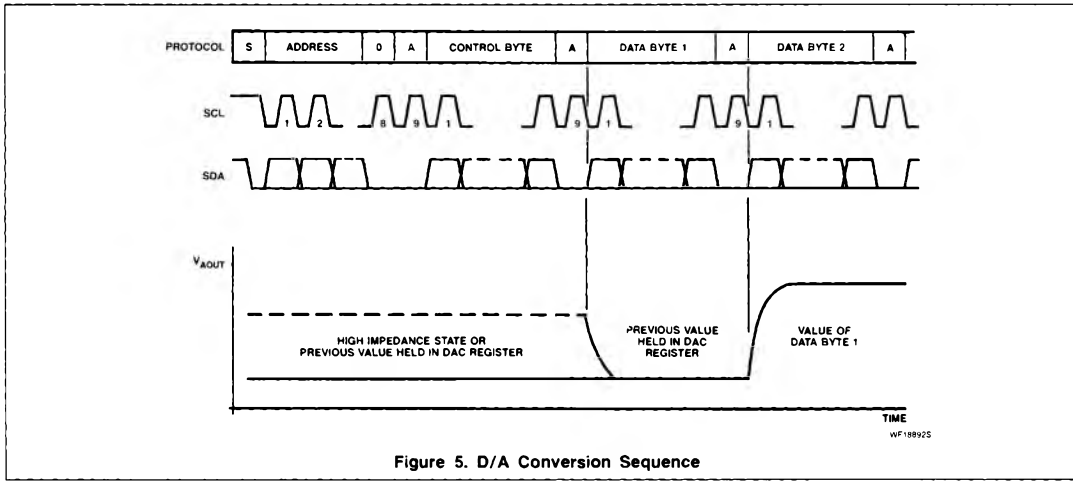


Figure 5. D/A Conversion Sequence

A/D Conversion

The A/D converter makes use of the successive-approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Figure 6).

Once a conversion cycle is triggered, an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Figure 7). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set, the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition, the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Figure 8.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

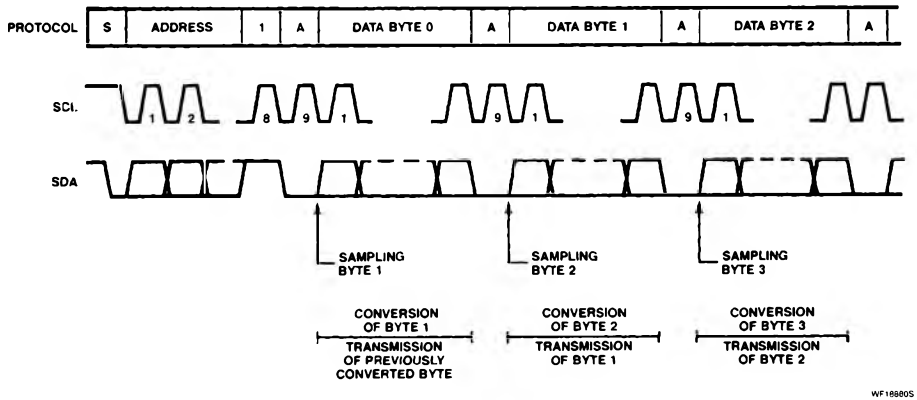
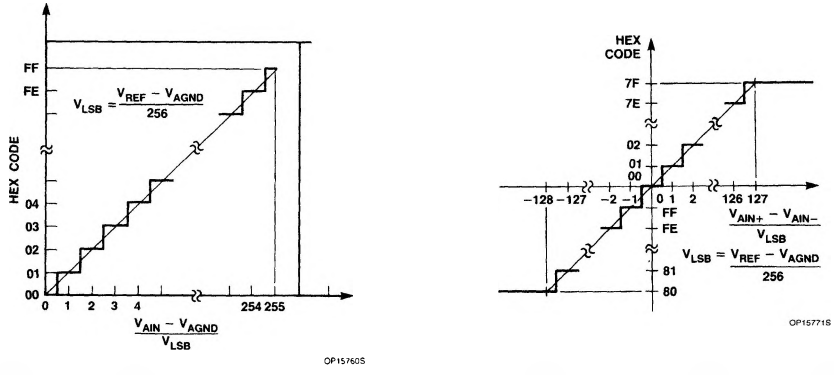


Figure 6. A/D Conversion Sequence



a. A/D Conversion Characteristics of Single-Ended Inputs **b. A/D Conversion Characteristics of Differential Inputs**

Figure 7

Reference Voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and A_{GND}). The A_{GND} pin has to be connected to the system analog ground and may have a DC offset with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and A_{GND} pins. This allows the use of the D/A converter as a one-quadrant multiplier (see Figure 4).

The A/D converter may also be used as a one- or two-quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

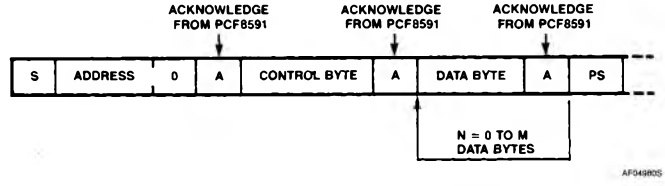
Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator, the OSC pin must be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

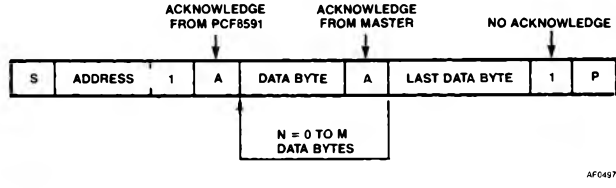
If the EXT_{TEST} pin is connected to V_{DD}, the oscillator output OSC is switched to a high impedance state, allowing the user to feed an external clock signal to OSC.

Bus Protocol

After a start condition, a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode, a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.



a. Bus Protocol for Write Mode, D/A Conversion



b. Bus Protocol for Read Mode, A/D Conversion

Figure 8

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the stop condition (P).

System Configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

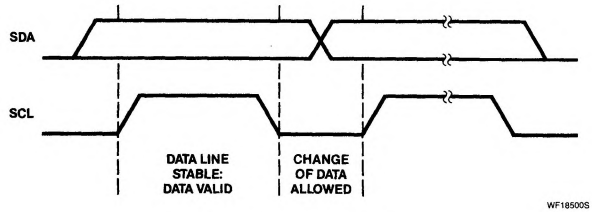


Figure 9. Bit Transfer

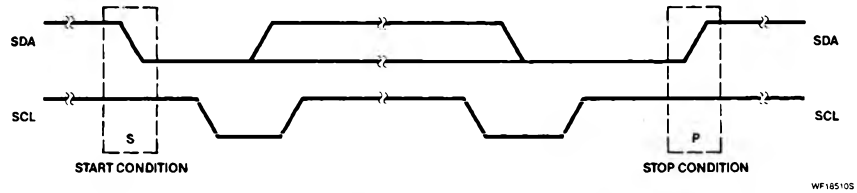


Figure 10. Definition of Start and Stop Condition

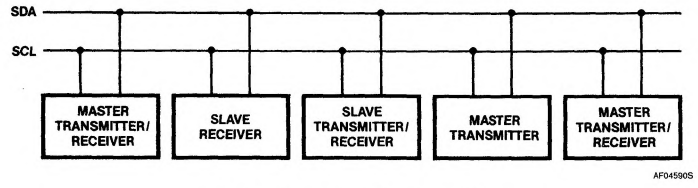


Figure 11. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. A master receiver must signal an end-of-data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

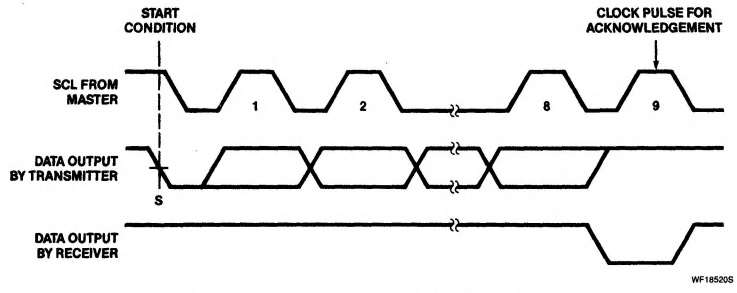


Figure 12. Acknowledgement on the I^2C Bus

Timing Specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
f_{SCL}	SCL clock frequency			100	kHz
t_{SW}	Tolerable spike width on bus			100	ns
t_{BUF}	Bus free time	4.0			μs
t_{SU}, t_{STA}	Start condition setup time	4.0			μs
t_{HD}, t_{STA}	Start condition hold time	4.7			μs
t_{LOW}	SCL LOW time	4.7			μs
t_{HIGH}	SCL HIGH time	4.0			μs
t_R	SCL and SDA rise time			1.0	μs
t_F	SCL and SDA fall time			0.3	μs
t_{SU}, t_{DAT}	Data setup time	250			ns
t_{HD}, t_{DAT}	Data hold time	0			ns
t_{VD}, t_{DAT}	SCL LOW to data out valid			3.4	μs
t_{SU}, t_{STO}	Stop condition setup time	4.0			μs

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analog inputs may also be connected to V_{GND} or V_{REF}.

In order to prevent excessive ground and supply noise, and to minimize cross-talk of the digital-to-analog signal paths, the user has to design the printed circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors (> 10μF) are recommended for power supply and reference voltage inputs.

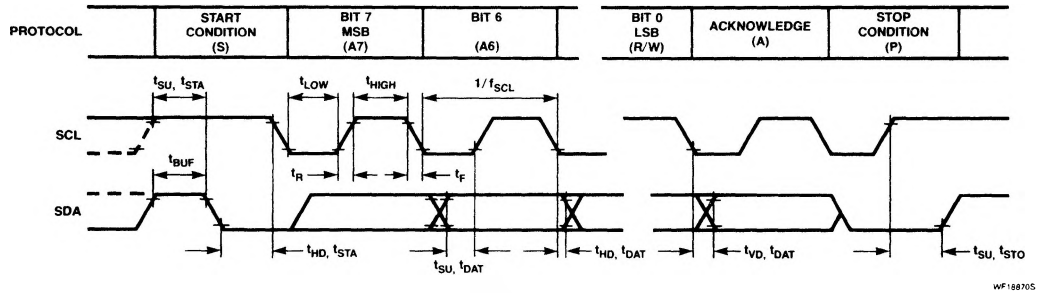


Figure 13. I²C Bus Timing Diagram

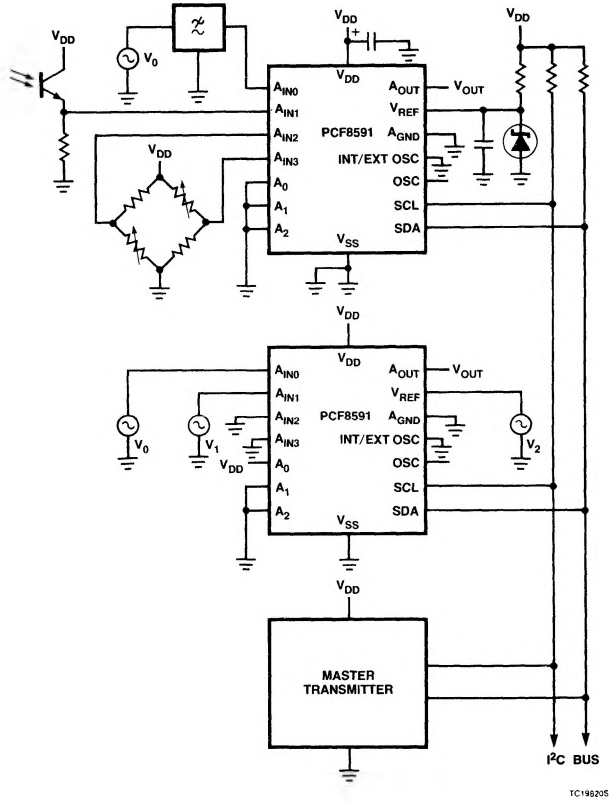
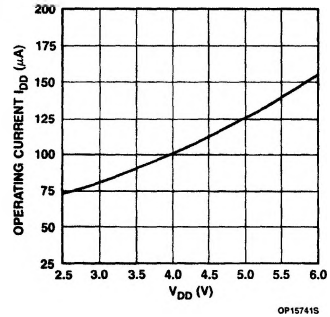


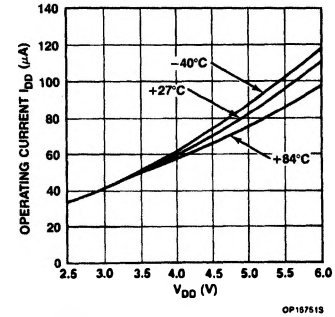
Figure 14. Application Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

Internal Oscillator

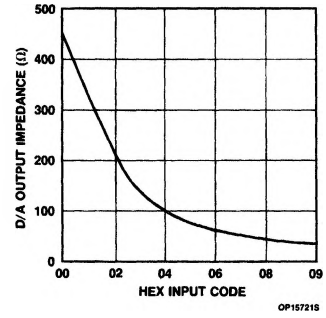


External Oscillator

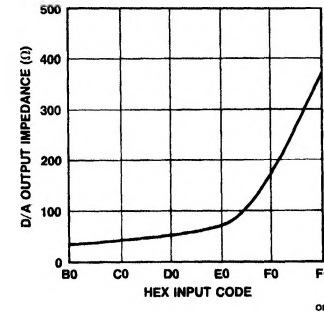


Operating Current vs. Supply Voltage (Analog Output Disabled)

Output Impedance near Negative Power Rail



Output Impedance near Positive Power Rail



NOTES:
The x-axis represents the hex input-code equivalent of the output voltage.
$V_{DD} = V_{REF} = 5.12V$ and $V_{SS} = V_{AGND}$

Output Impedance of Analog Ouput Buffer Near Power Rails