Signetics

PCF8574
8-Bit Remote I/O Expander

Product Specification

Linear Products

DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF8500 microcomputer families via the two-line serial bidirectional bus (I^2C). It can also interface microcomputers without a serial interface to the I^2C bus (as a slave function only). The device consists of an 8-bit quasi-bidirectional port and an I^2C interface.

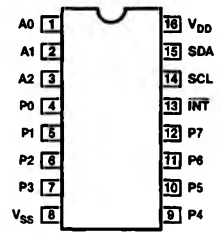
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I^2C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I^2C bus. This means that the PCF8574 can remain a simple slave device.

FEATURES

- **Operating supply voltage: 2.5V to 6V**
- **Low standby current consumption: max. 10μA**
- **Bidirectional expander**
- **Open-drain interrupt output**
- **8-bit remote I/O port for the I^2C bus**
- **Peripheral for the MAB8400 and PCF8500 microcomputer families**
- **Latched outputs with high current drive capability for directly driving LEDs**
- **Address by 3 hardware address pins for use of up to 8 devices (up to 16 possible with mask option)**

PIN CONFIGURATION

N, D Packages



TOP VIEW

CD07880S

PIN NO.	SYMBOL	DESCRIPTION
1	A0	Address inputs
2	A1	
3	A2	
4	P0	8-bit quasi-bidirectional I/O ports
5	P1	
6	P2	
7	P3	
8	V_{SS}	
9	P4	8-bit quasi-bidirectional I/O ports
10	P5	
11	P6	
12	P7	
13	$\overline{INT}$	Interrupt output
14	SCL	Serial clock line
15	SDA	Serial data line
16	V_{DD}	Positive supply

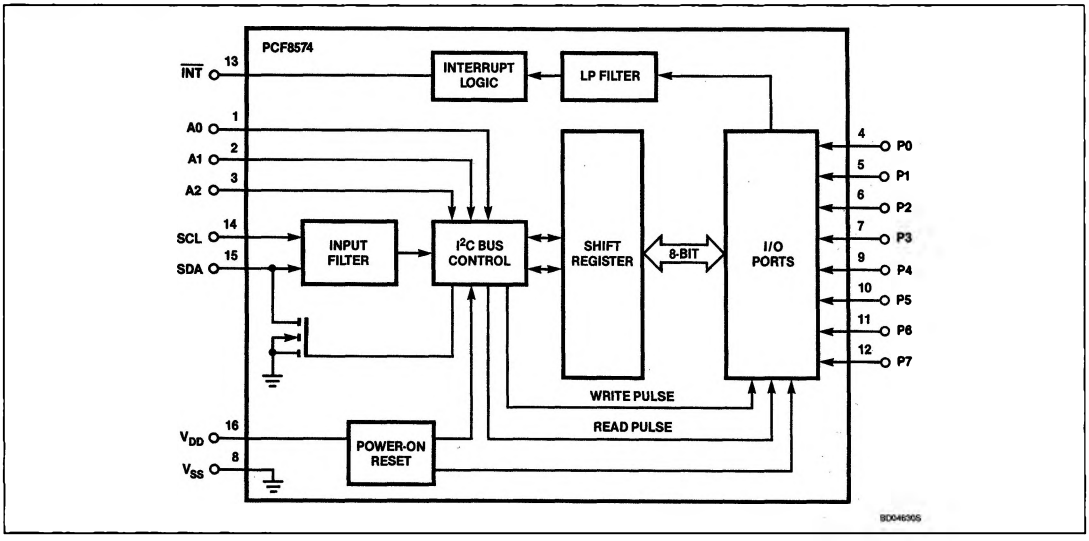
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP (SOT-38)	−40°C to +85°C	PCF8574PN
16-Pin Plastic SO package (SO16L; SOT-162A)	−40°C to +85°C	PCF8574TD

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.5 to +7	V
V_I	Input voltage range (any pin)	V_{SS} − 0.5 to V_{DD} + 0.5	V
$\pm I_I$	DC current into any input	20	mA
$\pm I_O$	DC current into any output	25	mA
$\pm I_{DD}$; I_{SS}	V_{DD} or V_{SS} current	100	mA
P_{TOT}	Total power dissipation	400	mW
P_O	Power dissipation per output	100	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range	−40 to +85	°C

BLOCK DIAGRAM



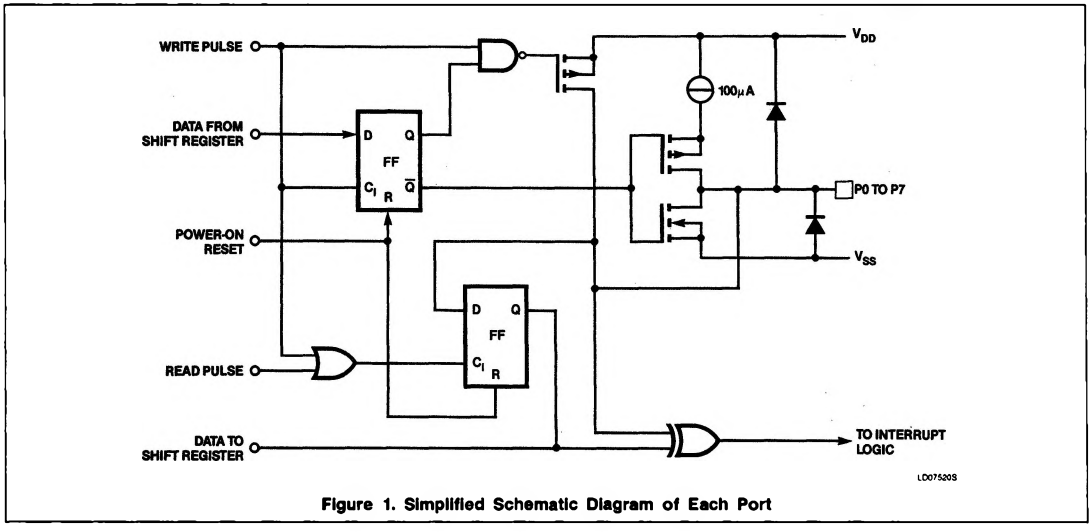


Figure 1. Simplified Schematic Diagram of Each Port

DC ELECTRICAL CHARACTERISTICS V_{DD} = 2.5 to 6V; V_{SS} = 0V; T_A = −40°C to +85°C, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
Supply (Pin 16)					
V_{DD}	Supply voltage	2.5		6	V
I_{DD} I_{DDO}	Supply current at V_{DD} = 6V; no load, inputs at V_{DD}, V_{SS} operating standby			100 10	μA μA
V_{REF}	Power-on reset voltage level[1]		1.3	2.4	V
Input SCL; Input/output SDA (Pins 14; 15)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5	V
I_{OL}	Output current LOW at V_{OL} = 0.4V	3			mA
$\|I_{LI}\|$	Input/output leakage current			100	nA
f_{SCL}	Clock frequency (See Figure 6)			100	kHz
t_S	Tolerable spike width at SCL and SDA input			100	ns
C_I	Input capacitance (SCL, SDA) at $V_I = V_{SS}$			7	pF
I/O ports (Pins 4 to 7; 9 to 12)					
V_{IL}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5V	V
$\pm I_{IHL}$	Maximum allowed input current through protection diode at $V_I \geq V_{DD}$ or $\leq V_{SS}$			400	μA
I_{OL}	Output current LOW at V_{OL} = 1V; V_{DD} = 2.5V	5			mA
$-I_{OH}$	Output current HIGH at $V_{OH} = V_{SS}$ (current source only)	30	100	300	μA
$-I_{OHt}$	Transient pull-up current HIGH during acknowledge (see Figure 14) at $V_{OH} = V_{SS}$		0.5		mA
$C_{I/O}$	Input/output capacitance			10	pF
Port timing; $C_L \leq$ 100pF (see Figures 10 and 11)					
t_{PV}	Output data valid			4	μs
t_{PS}	Input data setup	0			μs
t_{PH}	Input data hold	4			μs
Interrupt $\overline{INT}$ (Pin 13)					
I_{OL}	Output current LOW at V_{OL} = 0.4V	1.6			mA
$\|I_{OH}\|$	Output current HIGH at $V_{OH} = V_{DD}$			100	nA
$\overline{INT}$ timing; $C_L \leq$ 100pF (see Figure 11)					
t_{IV} t_{IR}	Input data valid Reset delay			4 4	μs μs
Select inputs A0, A1, A2 (Pins 1 to 3)					
V_{IH}	Input voltage LOW	−0.5V		$0.3V_{DD}$	V
V_{IH}	Input voltage HIGH	$0.7V_{DD}$		V_{DD} + 0.5V	V
$\|I_L\|$	Input leakage current at $V_I = V_{DD}$ or V_{SS}			100	nA

NOTE:

1. The power-on reset circuit resets the I^2C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse, as changes in the data line at this time will be interpreted as control signals.

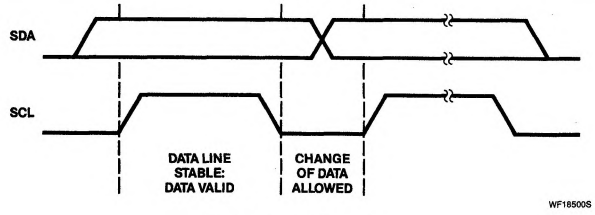


Figure 2. Bit Transfer

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

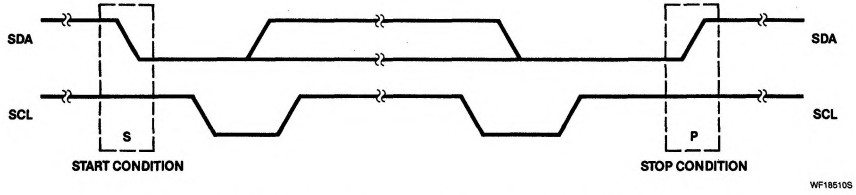


Figure 3. Definition of Start and Stop Conditions

System Configuration

A device generating a message is a "transmitter"; a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

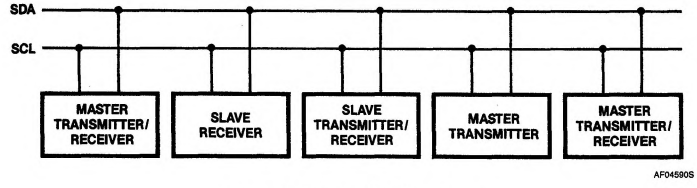


Figure 4. System Configuration

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge. Related clock pulse, setup and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

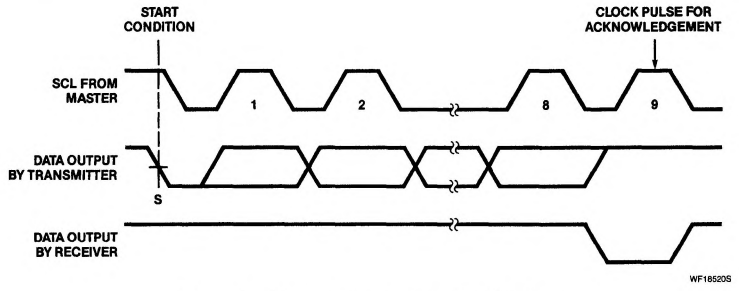


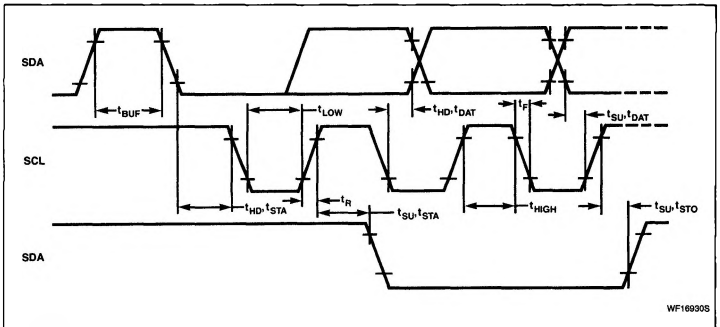
Figure 5. Acknowledgement on the I^2C Bus

Timing Specifications

Within the I^2C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8574 operates in both modes and the timing requirements are as follows:

High-Speed Mode

Masters generate a bus clock with a maximum frequency of 100kHz. Detailed timing is shown in Figure 6.

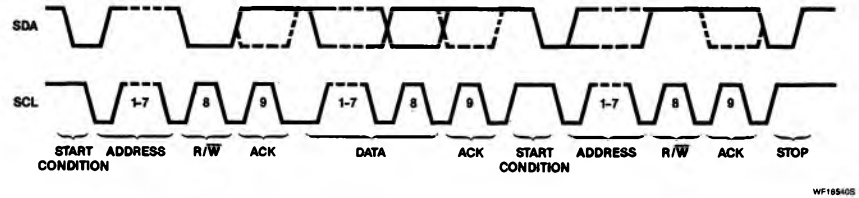


Where:

t_{BUF}	$t \geq t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD};t_{STA}$	$t \geq t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4.7μs	Clock LOW period
$t_{HIGHmin}$	4μs	Clock HIGH period
$t_{SU};t_{STA}$	$t \geq t_{LOWmin}$	Start condition set-up time; only valid for repeated start code
$t_{HD};t_{DAT}$	$t \geq 0\mu s$	Data hold time
$t_{SU};t_{DAT}$	$t \geq 250ns$	Data setup time
t_R	$t \leq 1\mu s$	Rise time of both the SDA and SCL line
t_F	$t \leq 300ns$	Fall time of both the SDA and SCL line
$t_{SU};t_{STO}$	$t \geq t_{LOWmin}$	Stop condition setup time

NOTE:
All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

Figure 6. Timing of the High-Speed Mode



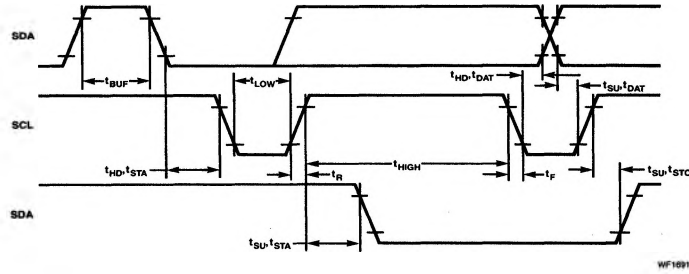
Where:

Clock t_{LOWmin}	4.7μs
$t_{HIGHmin}$	4μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1:1 (LOW-to-HIGH)
Maximum number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Figure 7. Complete Data Transfer in the High-Speed Mode

Low-Speed Mode

Masters generate a bus clock with a maximum frequency of 2kHz; a minimum LOW period of 105μs and a minimum HIGH period of 365μs. The mark-to-space ratio is 1:3 LOW-to-HIGH. Detailed timing is shown in Figure 8.



Where:

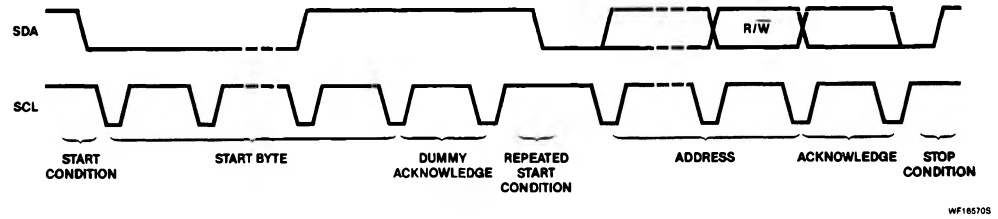
t_{BUF}	$t \geq 105\mu s$ (t_{LOWmin})
$t_{HD};\ t_{STA}$	$t \geq 365\mu s$ ($t_{HIGHmin}$)
t_{LOW}	130μs ± 25μs
t_{HIGH}	390μs ± 25μs
$t_{SU};\ t_{STA}$	130μs ± 25μs*
$t_{HD};\ t_{DAT}$	$t \geq 0\mu s$
$t_{SU};\ t_{DAT}$	$t \geq 250ns$
t_R	$t \leq 1\mu s$
t_F	$t \leq 300ns$
$t_{SU};\ t_{STO}$	130μs ± 25μs

NOTES:

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

* Only valid for repeated start code.

Figure 8. Timing of the Low-Speed Mode



Where:

Clock t_{LOWmin}	130µs ± 25µs
$t_{HIGHmin}$	390µs ± 25µs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Figure 9. Complete Data Transfer in the Low-Speed Mode

FUNCTIONAL DESCRIPTION

Addressing (See Figures 10 and 11)

Each bit of the PCF8574 I/O port can be independently used as an input or an output.

Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

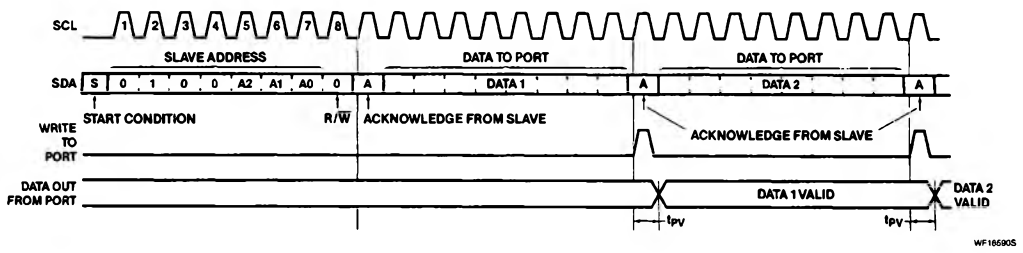
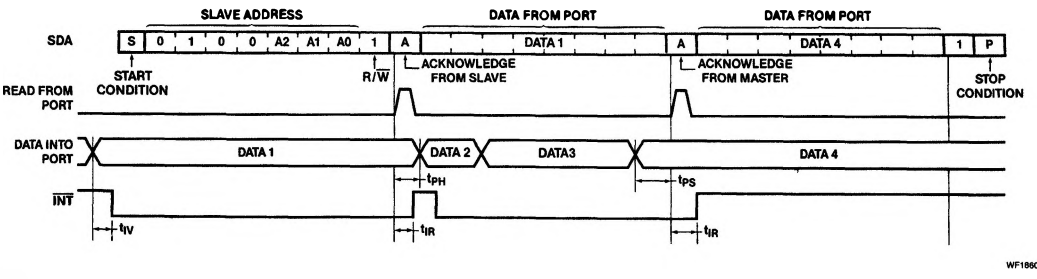


Figure 10. WRITE Mode (Output Port)



NOTE:
A LOW-to-HIGH transition of SDA while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Figure 11. READ Mode (Input Port)

Interrupt (See Figures 12 and 13)

The PCF8574 provides an open-drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{IV} the signal $\overline{INT}$ is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt. Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit.

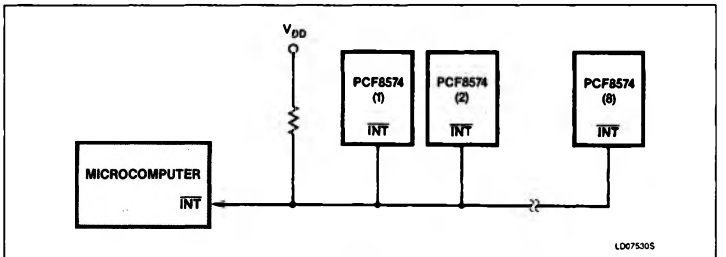


Figure 12. Application of Multiple PCF8574s With Interrupt

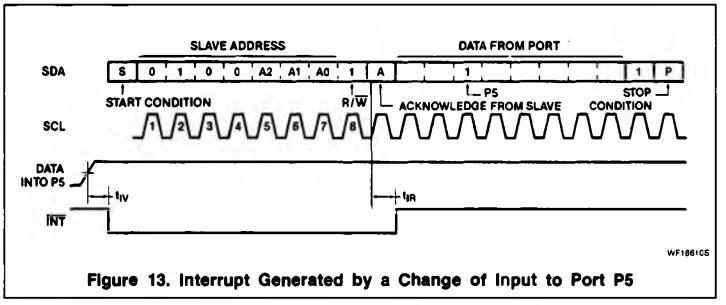


Figure 13. Interrupt Generated by a Change of Input to Port P5

Quasi-Bidirectional I/O Ports (See Figure 14)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW-to-HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

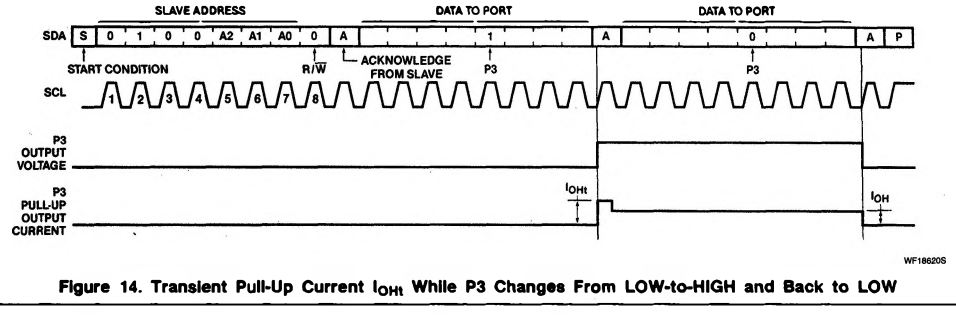


Figure 14. Transient Pull-Up Current I_{OHt} While P3 Changes From LOW-to-HIGH and Back to LOW