DATA SHEET

PCF21XXC family
LCD drivers

Product specification

File under Integrated Circuits, IC12

1995 May 03

PHILIPS

LCD drivers

PCF21XXC family

FEATURES

- Supply voltage 2.25 to 6.0 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Stand-alone or expanded system
- Power-on reset clear
- LCD segments
  - 40 (PCF2100C)
  - 64 (PCF2111C)
  - 32 (PCF2112C)
- Multiplex rate
  - 1 : 2 (PCF2100C)
  - 1 : 2 (PCF2111C)
  - 1 : 1 (PCF2112C)
- Word length
  - 22 bits (PCF2100C)
  - 34 bits (PCF2111C)
  - 34 bits (PCF2112C).

GENERAL DESCRIPTION

The members of the PCF21XXC family are single-chip, silicon gate CMOS circuits. A 3-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

The PCF21XXC family chips have the same function and performance as those of the PCF21XX family. The voltage is reduced from 6.5 to 6.0 V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD1}	supply current 1	outputs open; CBUS inactive	–	20	50	μA
I_{DD2}	supply current 2	outputs open; CBUS inactive; $T_{amb} = 25\ ^\circ C$	–	20	30	μA
P_O	power dissipation per output		–	–	100	mW
T_{amb}	operating ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–65	–	+150	°C

ORDERING INFORMATION

| TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF2100CP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCF2100CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
PCF2111CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2111CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
PCF2112CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF2112CT	VSO40	plastic very small outline package; 40 leads	SOT158-1
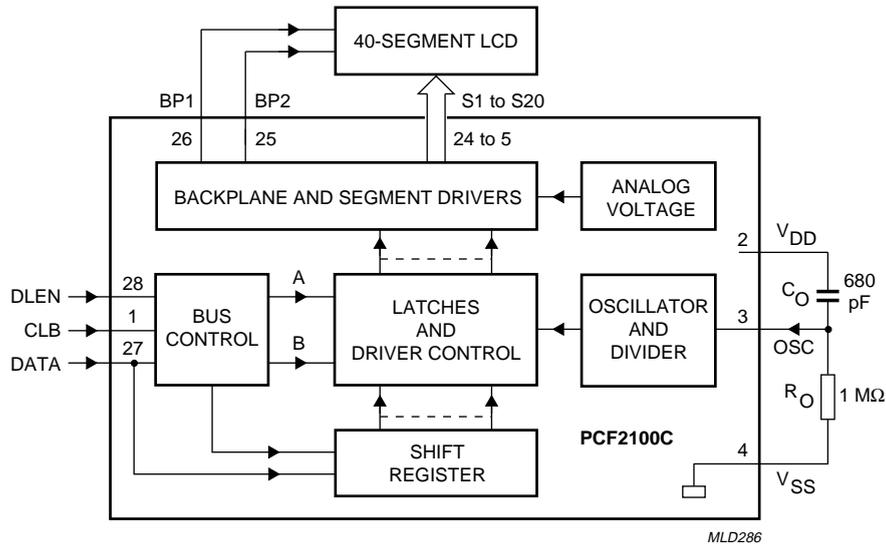
BLOCK DIAGRAMS

Fig.1 Block diagram; PCF2100C.

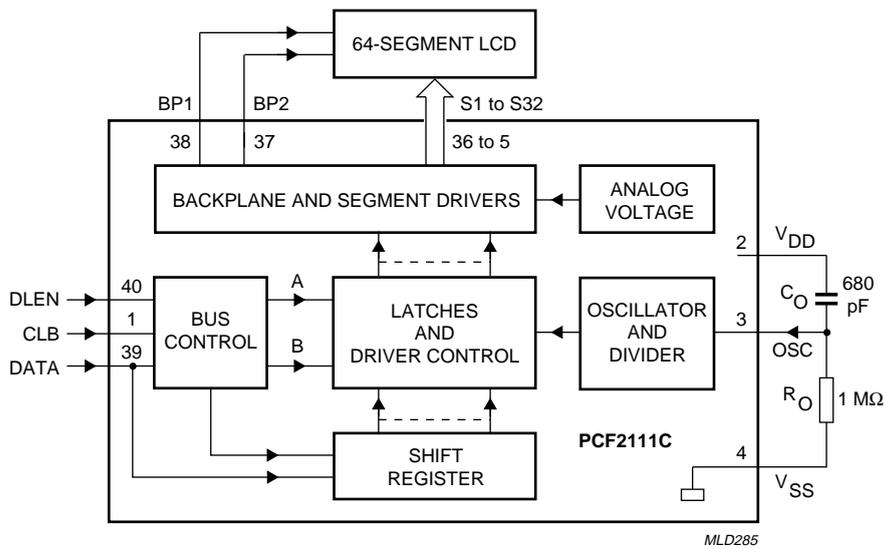Fig.2 Block diagram; PCF2111C.
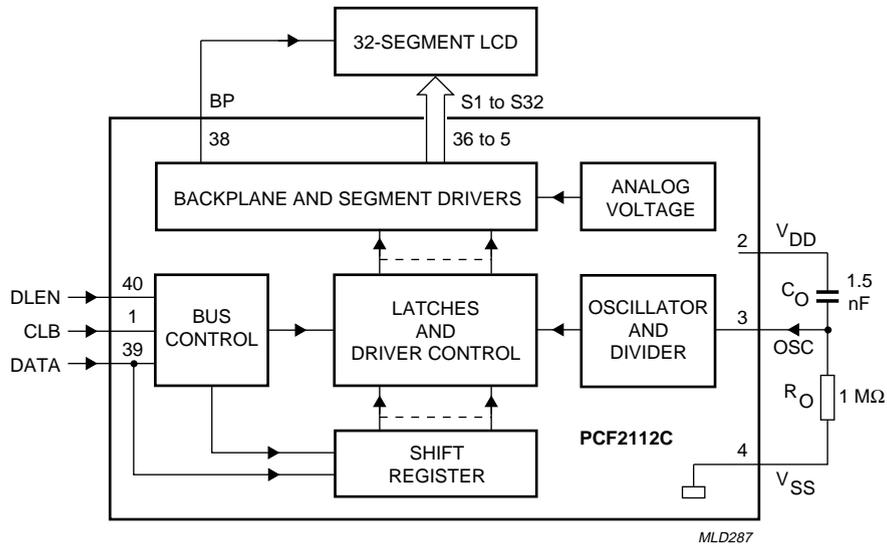
Fig.3 Block diagram; PCF2112C.

LCD drivers

PCF21XXC family

PINNING

PCF2100C

SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S20	5	LCD driver output 20
S19	6	LCD driver output 19
S18	7	LCD driver output 18
S17	8	LCD driver output 17
S16	9	LCD driver output 16
S15	10	LCD driver output 15
S14	11	LCD driver output 14
S13	12	LCD driver output 13
S12	13	LCD driver output 12
S11	14	LCD driver output 11
S10	15	LCD driver output 10
S9	16	LCD driver output 9
S8	17	LCD driver output 8
S7	18	LCD driver output 7
S6	19	LCD driver output 6
S5	20	LCD driver output 5
S4	21	LCD driver output 4
S3	22	LCD driver output 3
S2	23	LCD driver output 2
S1	24	LCD driver output 1
BP2	25	backplane driver output 2
BP1	26	backplane driver output 1
DATA	27	date input line (CBUS)
DLEN	28	data input line enable (CBUS)
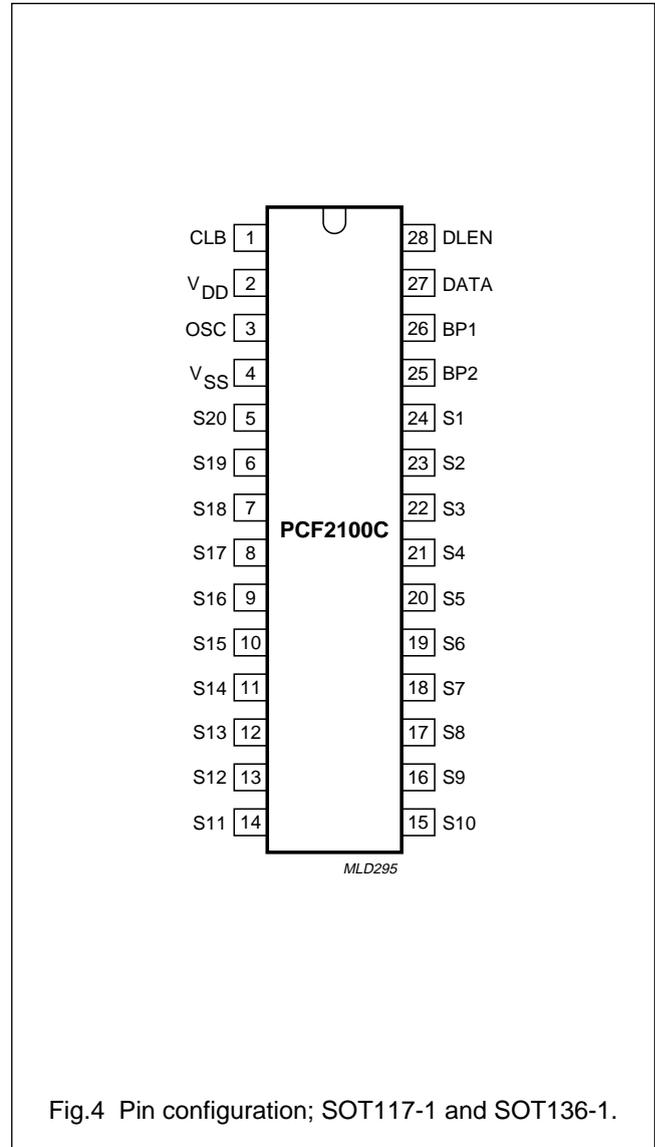
Fig.4 Pin configuration; SOT117-1 and SOT136-1.

LCD drivers

PCF21XXC family

PCF2111C

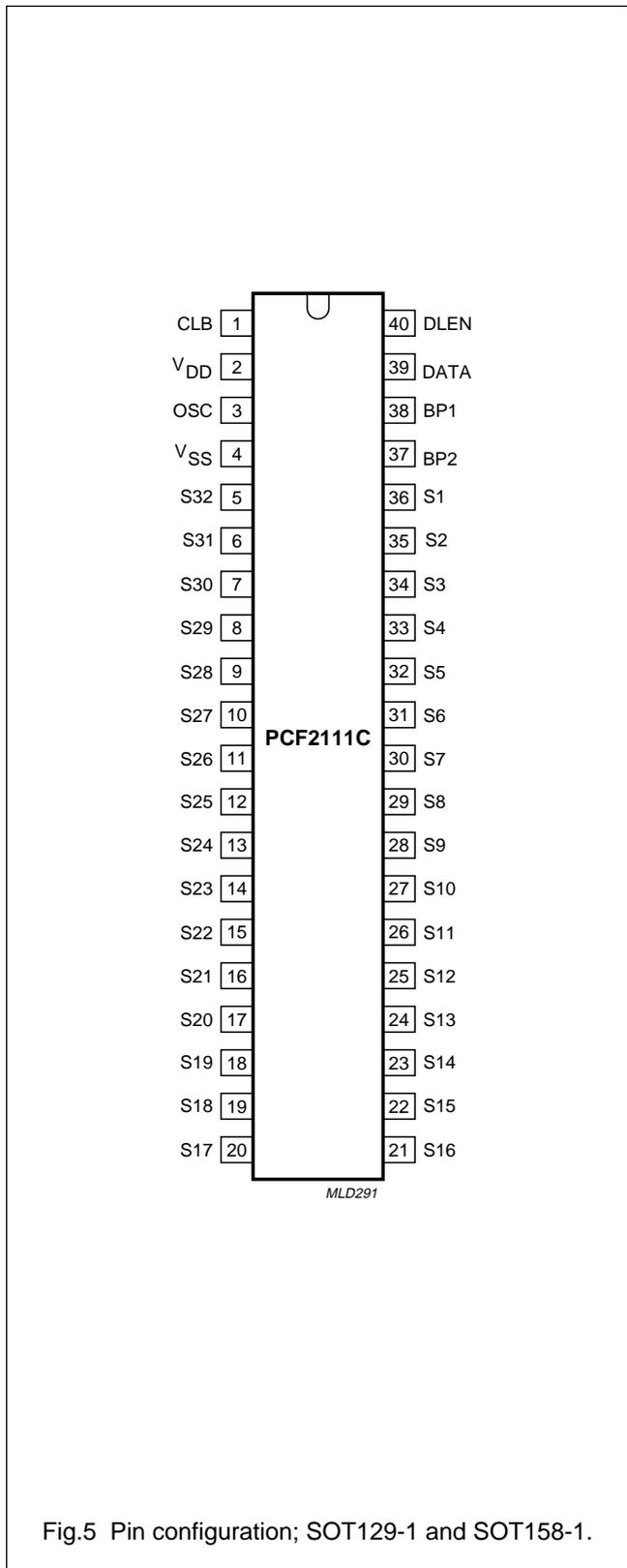| SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
BP2	37	backplane driver output 2
BP1	38	backplane driver output 1
DATA	39	date input line (CBUS)
DLEN	40	data input line enable (CBUS)

Fig.5 Pin configuration; SOT129-1 and SOT158-1.

LCD drivers   PCF21XXC family

PCF2112C

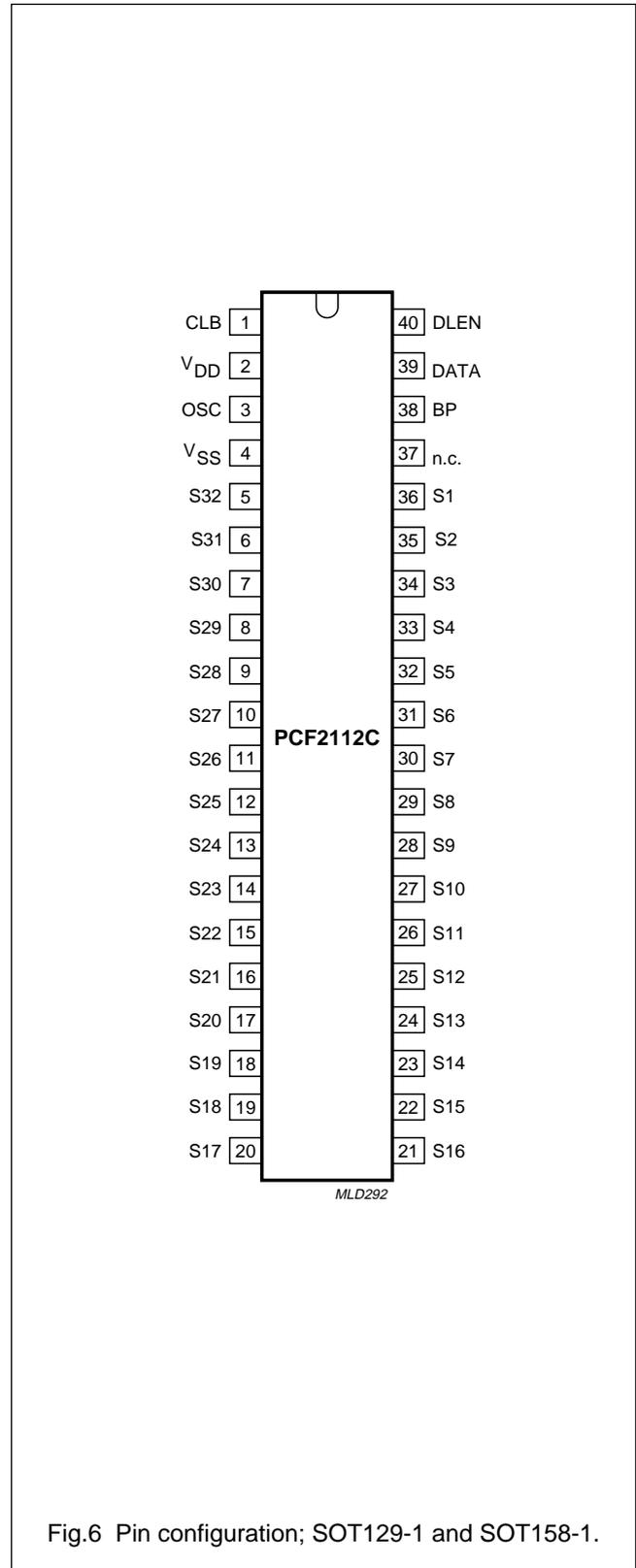| SYMBOL	PIN	DESCRIPTION
CLB	1	clock burst input (CBUS)
V_{DD}	2	supply voltage
OSC	3	oscillator input
V_{SS}	4	supply voltage ground
S32	5	LCD driver output 32
S31	6	LCD driver output 31
S30	7	LCD driver output 30
S29	8	LCD driver output 29
S28	9	LCD driver output 28
S27	10	LCD driver output 27
S26	11	LCD driver output 26
S25	12	LCD driver output 25
S24	13	LCD driver output 24
S23	14	LCD driver output 23
S22	15	LCD driver output 22
S21	16	LCD driver output 21
S20	17	LCD driver output 20
S19	18	LCD driver output 19
S18	19	LCD driver output 18
S17	20	LCD driver output 17
S16	21	LCD driver output 16
S15	22	LCD driver output 15
S14	23	LCD driver output 14
S13	24	LCD driver output 13
S12	25	LCD driver output 12
S11	26	LCD driver output 11
S10	27	LCD driver output 10
S9	28	LCD driver output 9
S8	29	LCD driver output 8
S7	30	LCD driver output 7
S6	31	LCD driver output 6
S5	32	LCD driver output 5
S4	33	LCD driver output 4
S3	34	LCD driver output 3
S2	35	LCD driver output 2
S1	36	LCD driver output 1
n.c.	37	not connected
BP	38	backplane driver output
DATA	39	date input line (CBUS)
DLEN	40	data input line enable (CBUS)

Fig.6 Pin configuration; SOT129-1 and SOT158-1.

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA bit is HIGH.

PCF2100C

When DATA bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA bit 21 LOW, the B-latches (BP2) are loaded. CLB pulse 23 transfers data from the shift register to the selected latches.

PCF2111C

When DATA bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA bit 33 LOW, the B-latches (BP2) are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

PCF2112C

When DATA bit 33 is HIGH, the latches are loaded. CLB pulse 35 transfers data from the shift register to the selected latches.

Bus control logic

The following tests are carried out by the bus control logic:

1. Test on leading zero
2. Test on number of DATA bits
3. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.
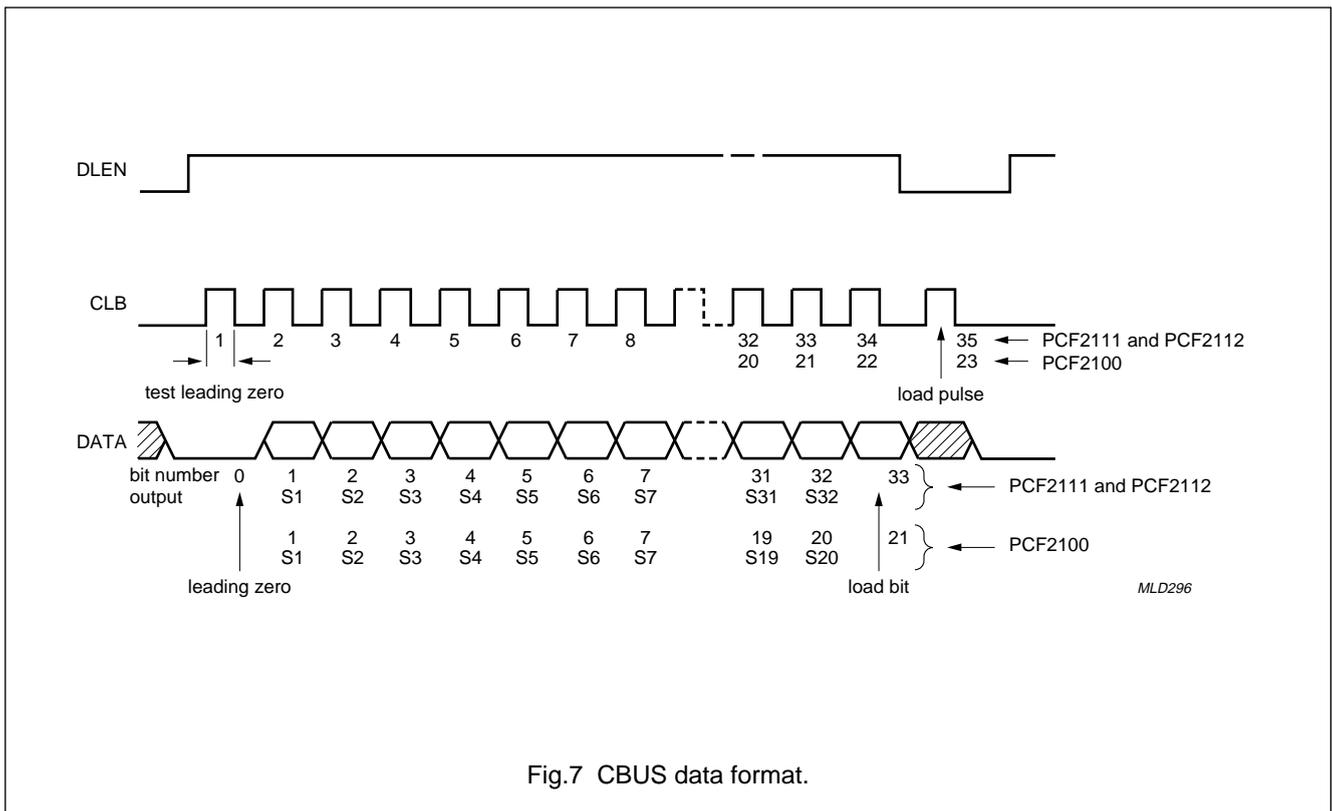
Fig.7 CBUS data format.
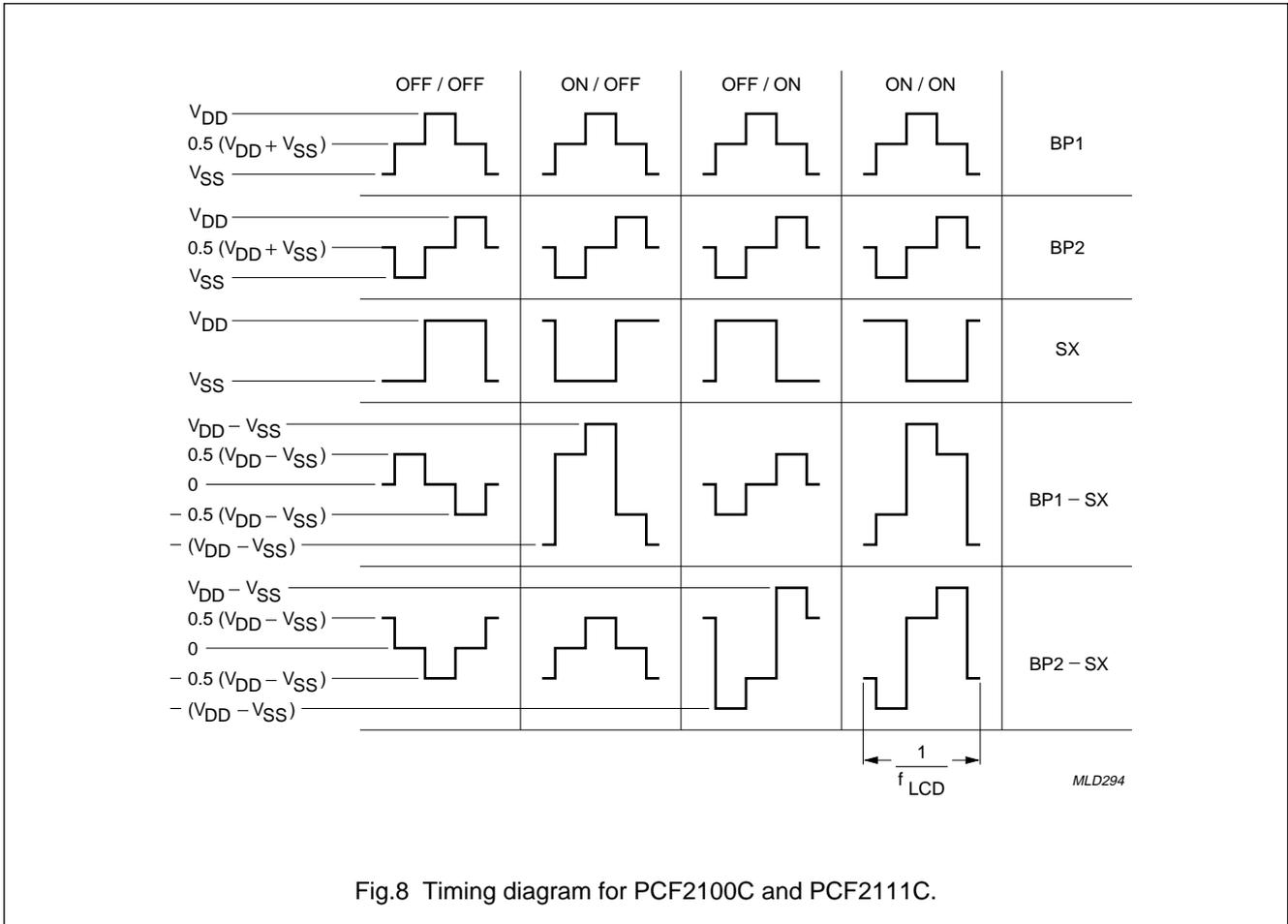
Timing

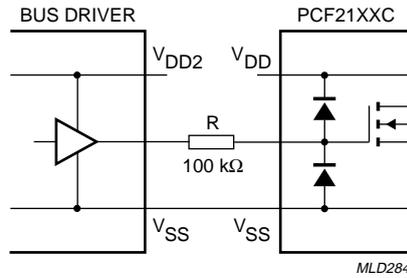Fig.8 Timing diagram for PCF2100C and PCF2111C.
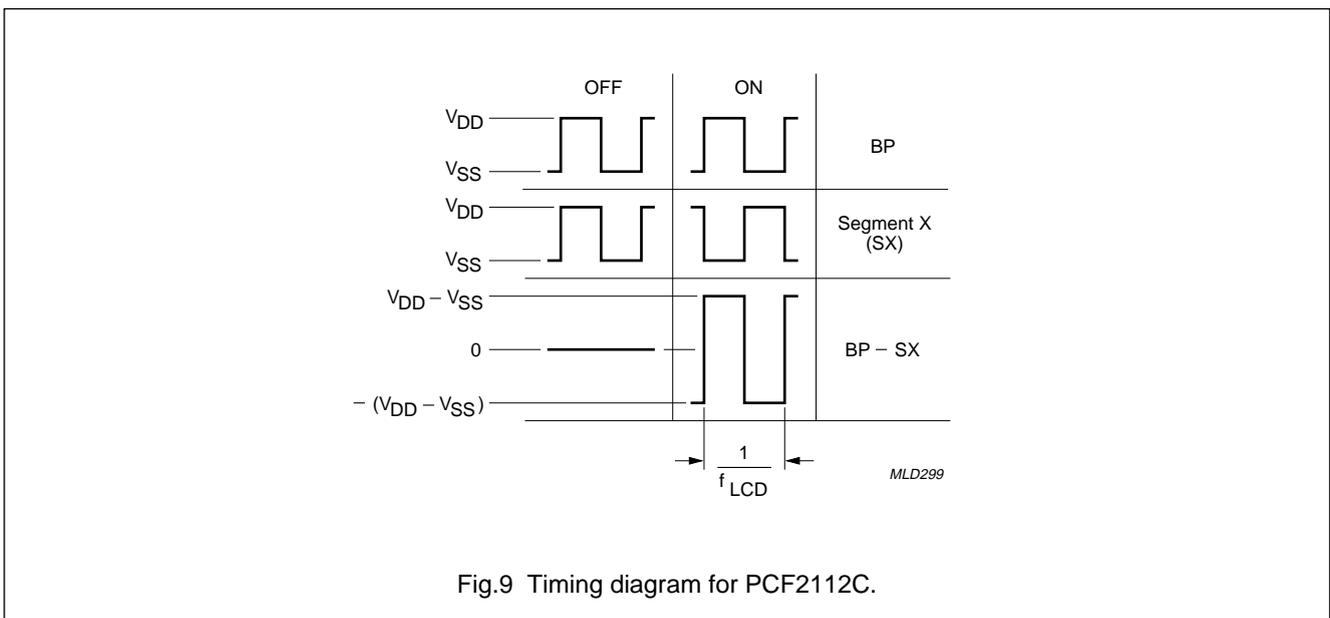
Fig.9 Timing diagram for PCF2112C.

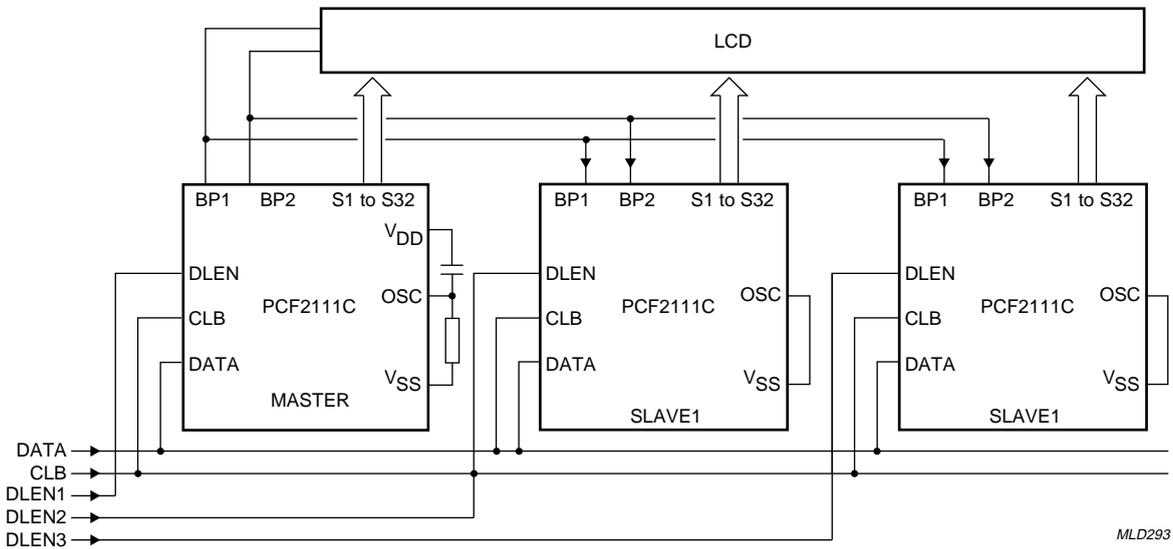LCD drivers

PCF21XXC family

Input circuitry

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0.5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current ≤ 40 µA.

Fig.10 Input circuitry.

Expansion

By connecting OSC to V_{SS} the BP pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XXC family up to the BP drive capability of the master. The PCF2112C can only function as a master for other PCF2112Cs.

Fig.11 Expansion possibility (using PCF2111C).

LCD drivers

PCF21XXC family

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		−0.5	+8.0	V
V_I	input voltage DLEN, CLB, DATA and OSC		$V_{SS} − 0.5$	$V_{DD} + 0.5$	V
V_O	output voltage BP1, BP2 and S1 to S32		$V_{SS} − 0.5$	$V_{DD} + 0.5$	V
I_{DD}, I_{SS}	supply current		−50	+50	mA
I_I	DC input current		−20	+20	mA
I_O	DC output current		−25	+25	mA
P_{tot}	total power dissipation per package	note 1	–	500	mW
P_O	power dissipation per output		–	100	mW
T_{stg}	storage temperature		−65	+150	°C

Note

1. Derate by 7.7 mW/K when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.
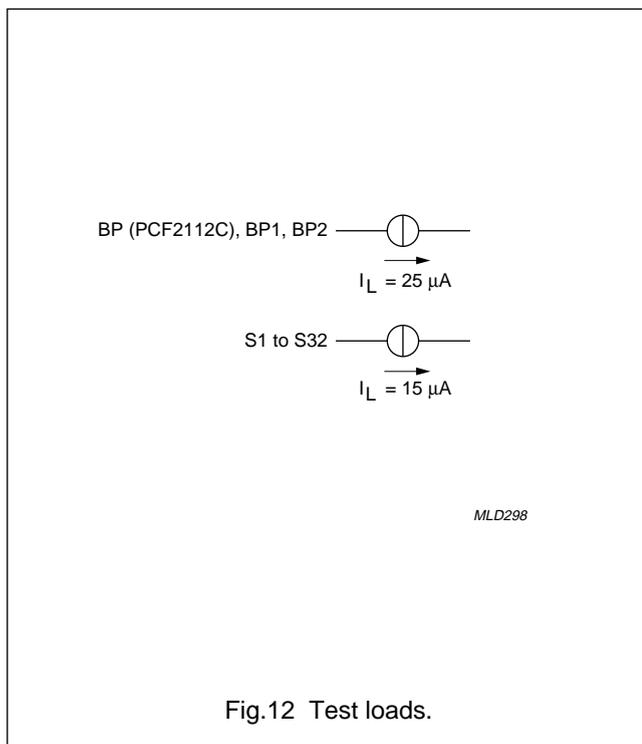
ESD in accordance with *"MIL STD 883C, Method 3015"*.

LCD drivers

PCF21XXC family

DC CHARACTERISTICS
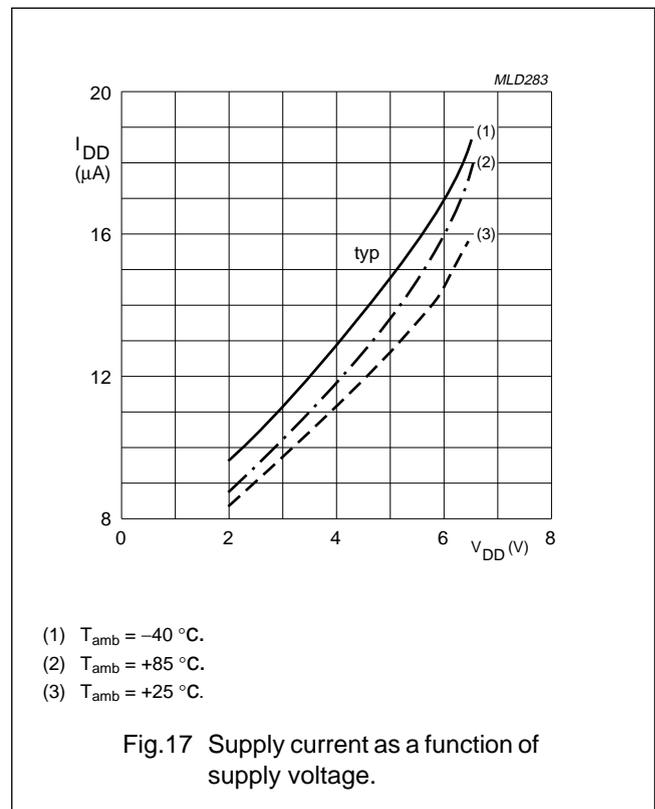
V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.25	–	6.0	V
I_{DD}	supply current	note 1	–	20	50	µA
		note 1; T_{amb} = 25 °C	–	20	30	µA
V_{POR}	power-on reset voltage level	note 2	–	1.0	1.6	V
Inputs CLB, DATA and DLEN						
V_{IL}	LOW level input voltage		–	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	–	V
I_{LI}	input leakage current	V_I = V_{SS} or V_{DD}	–	–	±1	µA
C_I	input capacitance	note 3	–	–	10	pF
Input OSC						
I_{osc}	oscillator start-up current	V_I = V_{SS}	0.5	1.2	5.0	µA
LCD outputs						
V_{BP}	DC voltage of backplane drivers		–	±20	–	mV
$Z_{O(BP)}$	backplane driver output impedance	note 4; V_{DD} = 5 V	–	0.5	5.0	kΩ
$Z_{O(S)}$	segment driver output impedance	note 4; V_{DD} = 5 V	–	1	7	kΩ

Notes

1. Outputs open; CBUS inactive.

2. Resets all logic, when V_{DD} < V_{POR}.

3. Periodically sampled (not 100% tested).

4. Outputs measured one at a time.

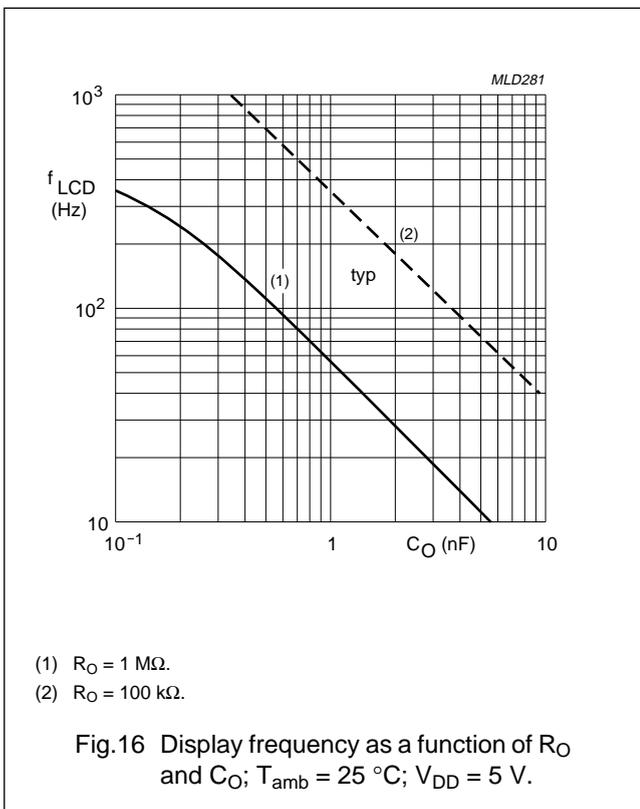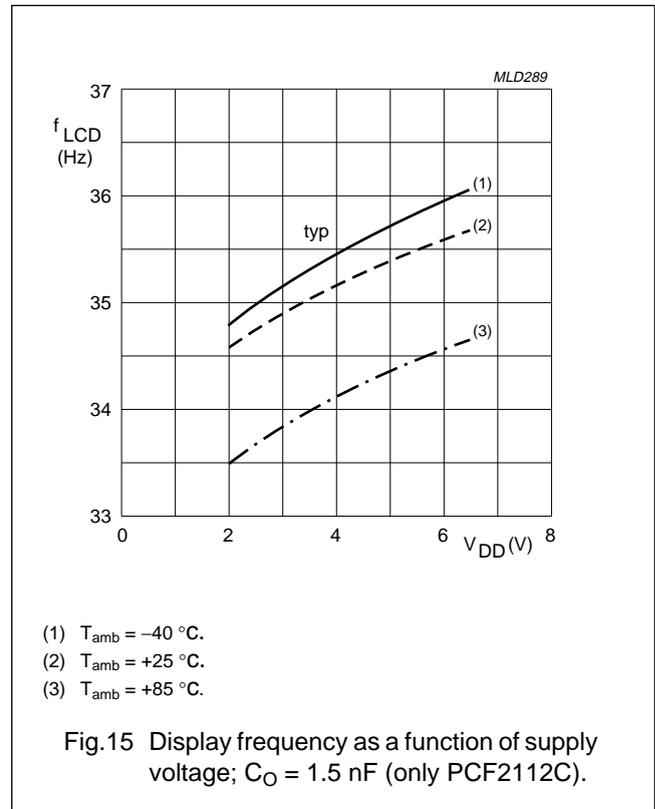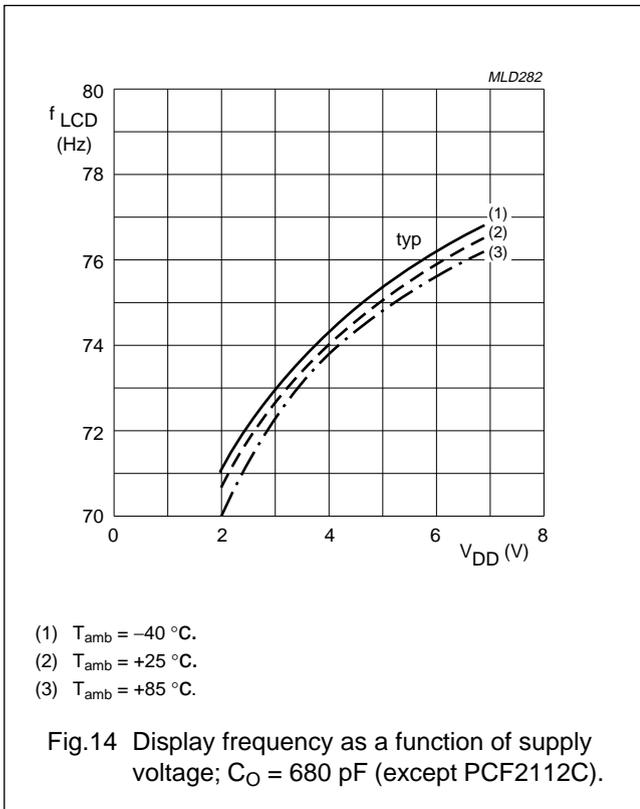LCD drivers

PCF21XXC family

AC CHARACTERISTICS

V_{DD} = 2.25 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +80 °C; R_O = 1 MΩ; C_O = 680 pF; all timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs CLB, DATA and DLEN						
t_{SUDA}	data set-up time		3	–	–	μs
t_{HDDA}	data hold time		3	–	–	μs
t_{SUEN}	enable set-up time		1	–	–	μs
t_{SUDI}	disable set-up time		2	–	–	μs
t_{SULD}	load pulse set-up time		2.5	–	–	μs
t_{BUSY}	busy time		3	–	–	μs
t_{WH}	CLB HIGH time		1	–	–	μs
t_{WL}	CLB LOW time		5	–	–	μs
t_{CLB}	CLB cycle time		10	–	–	μs
t_r	rise time		–	–	10	μs
t_f	fall time		–	–	10	μs
LCD timing						
f_{LCD}	LCD frame frequency					
	PCF2100C, PCF2111C		60	75	100	Hz
	PCF2112C	C_O = 1.5 nF	30	35	50	Hz
t_{BS}	transfer time with test loads	V_{DD} = 5 V	–	20	100	μs
t_{PLCD}	driver delay time with test loads	V_{DD} = 5 V	–	20	100	μs

BP (PCF2112C), BP1, BP2

I_L = 25 μA

S1 to S32

I_L = 15 μA

MLD298

Fig.12 Test loads.

Fig.13 CBUS timing.

(1) Load pulse 23 for PCF2100C.
(2) Load pulse 35 for PCF2111C and PCF2112C (see Fig.7).

LCD drivers

PCF21XXC family

(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +25$ °C.
(3) $T_{amb} = +85$ °C.

Fig.14 Display frequency as a function of supply voltage; $C_O = 680$ pF (except PCF2112C).

(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +25$ °C.
(3) $T_{amb} = +85$ °C.

Fig.15 Display frequency as a function of supply voltage; $C_O = 1.5$ nF (only PCF2112C).

(1) $R_O = 1$ MΩ.
(2) $R_O = 100$ kΩ.

Fig.16 Display frequency as a function of R_O and C_O; $T_{amb} = 25$ °C; $V_{DD} = 5$ V.

(1) $T_{amb} = -40$ °C.
(2) $T_{amb} = +85$ °C.
(3) $T_{amb} = +25$ °C.

Fig.17 Supply current as a function of supply voltage.

(1) T_{amb} = +85 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = −40 °C.

Fig.18 Output resistance of backplane
and segments.

(1) T_{amb} = −40 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.19 LOW level output current as a function
of supply voltage (only PCF2112C).

LCD drivers

PCF21XXC family

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil)
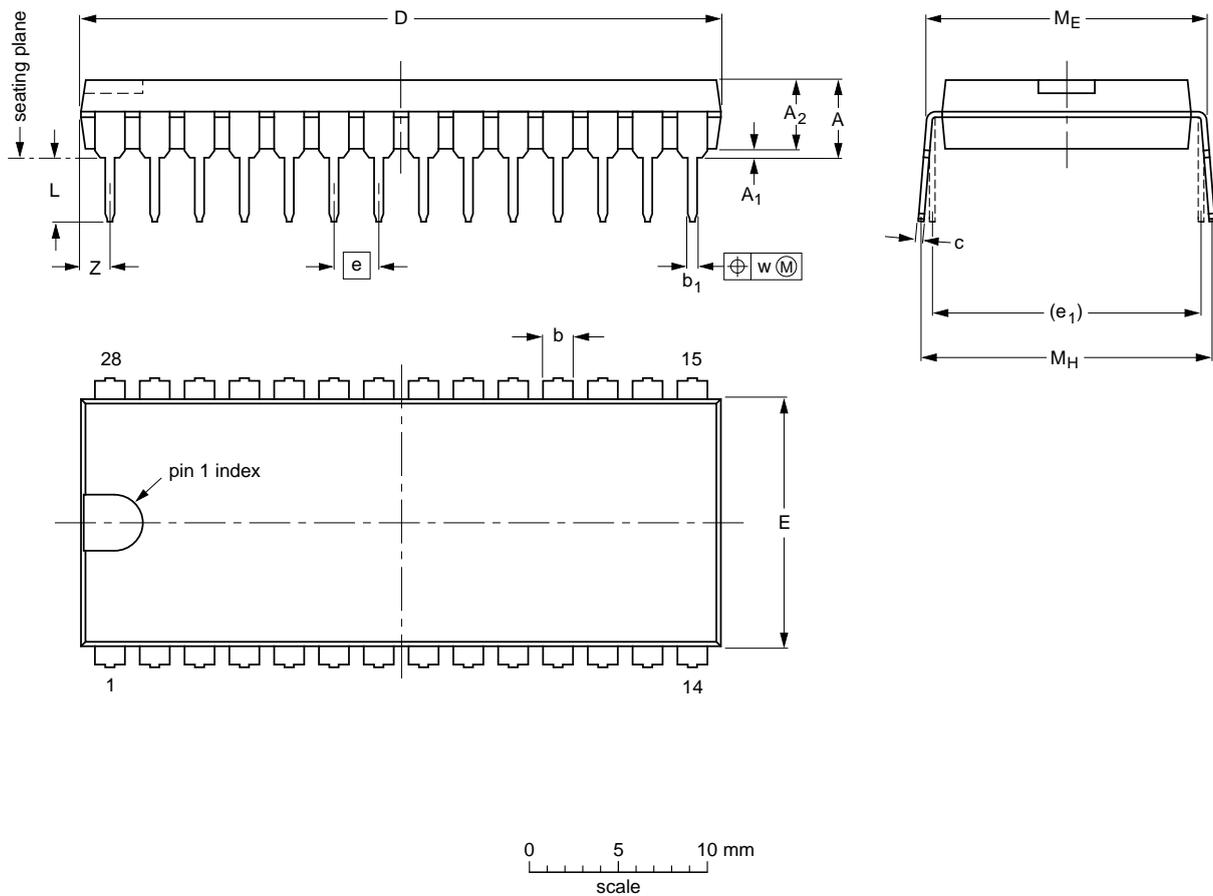
SOT117-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D(1)	E(1)	e	e₁	L	M_E	M_H	w	Z(1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				92-11-17 95-01-14

LCD drivers

PCF21XXC family

DIP40: plastic dual in-line package; 40 leads (600 mil)
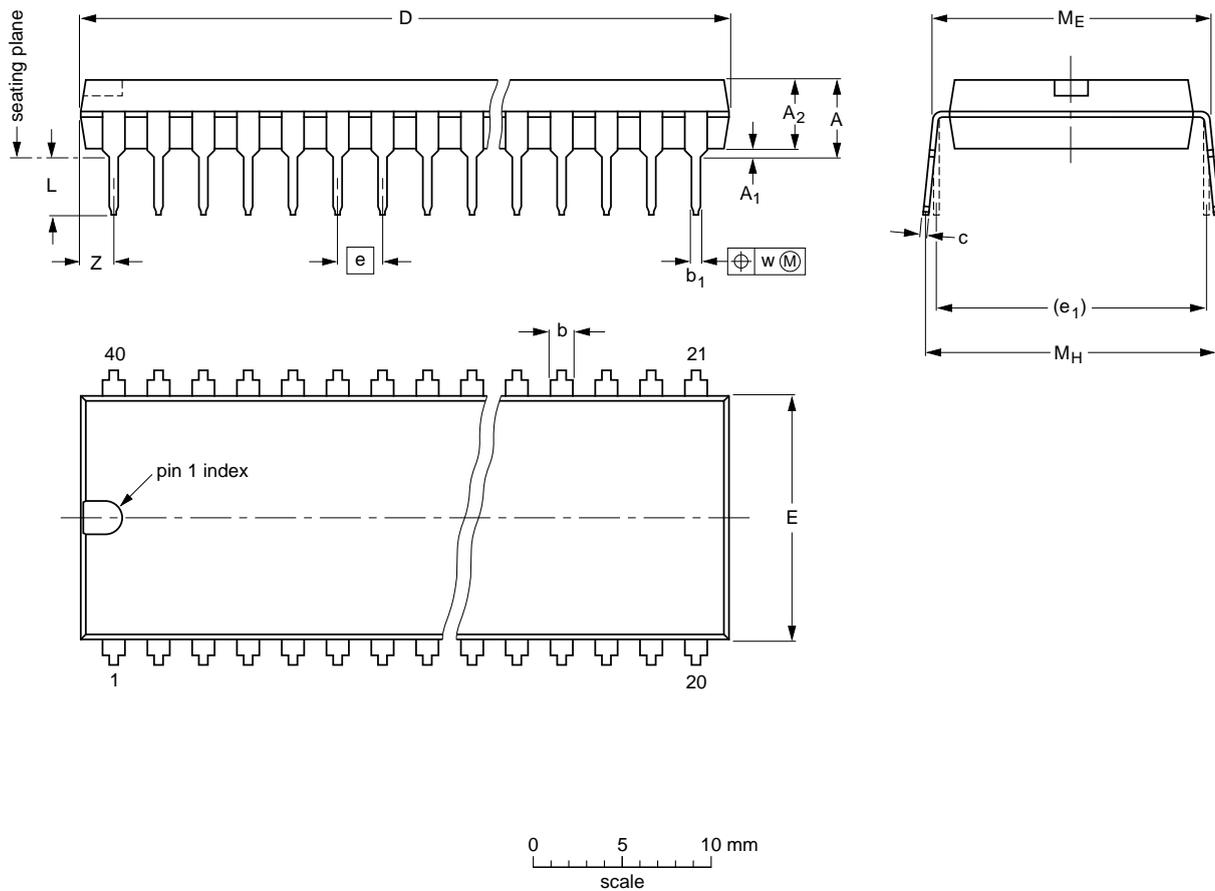
SOT129-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D [1]	E [1]	e	e₁	L	M_E	M_H	w	Z [1] max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				92-11-17 95-01-14

LCD drivers

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SO28: plastic small outline package; 28 leads; body width 7.5 mm
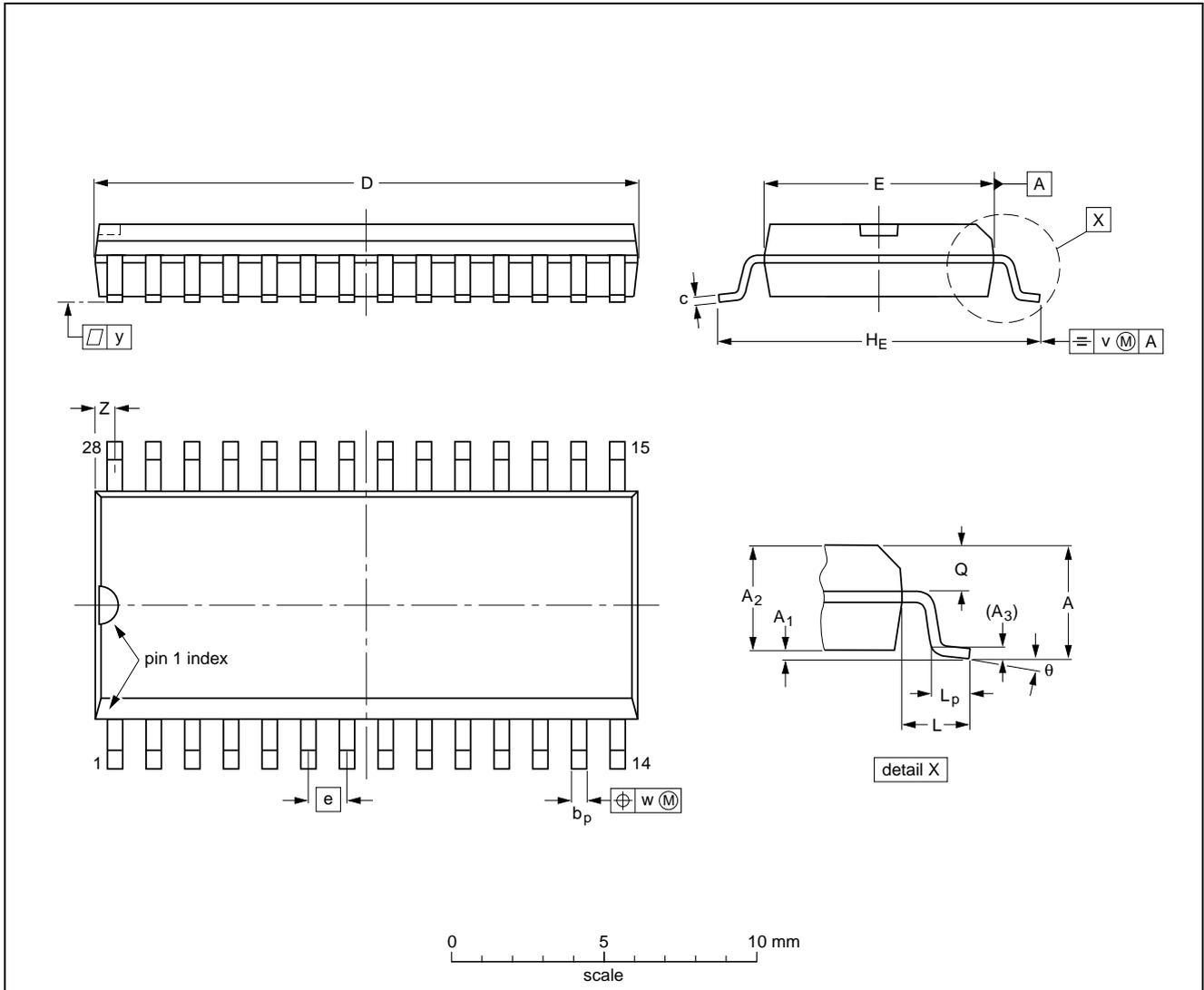
SOT136-1

scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

LCD drivers

PCF21XXC family

VSO40: plastic very small outline package; 40 leads
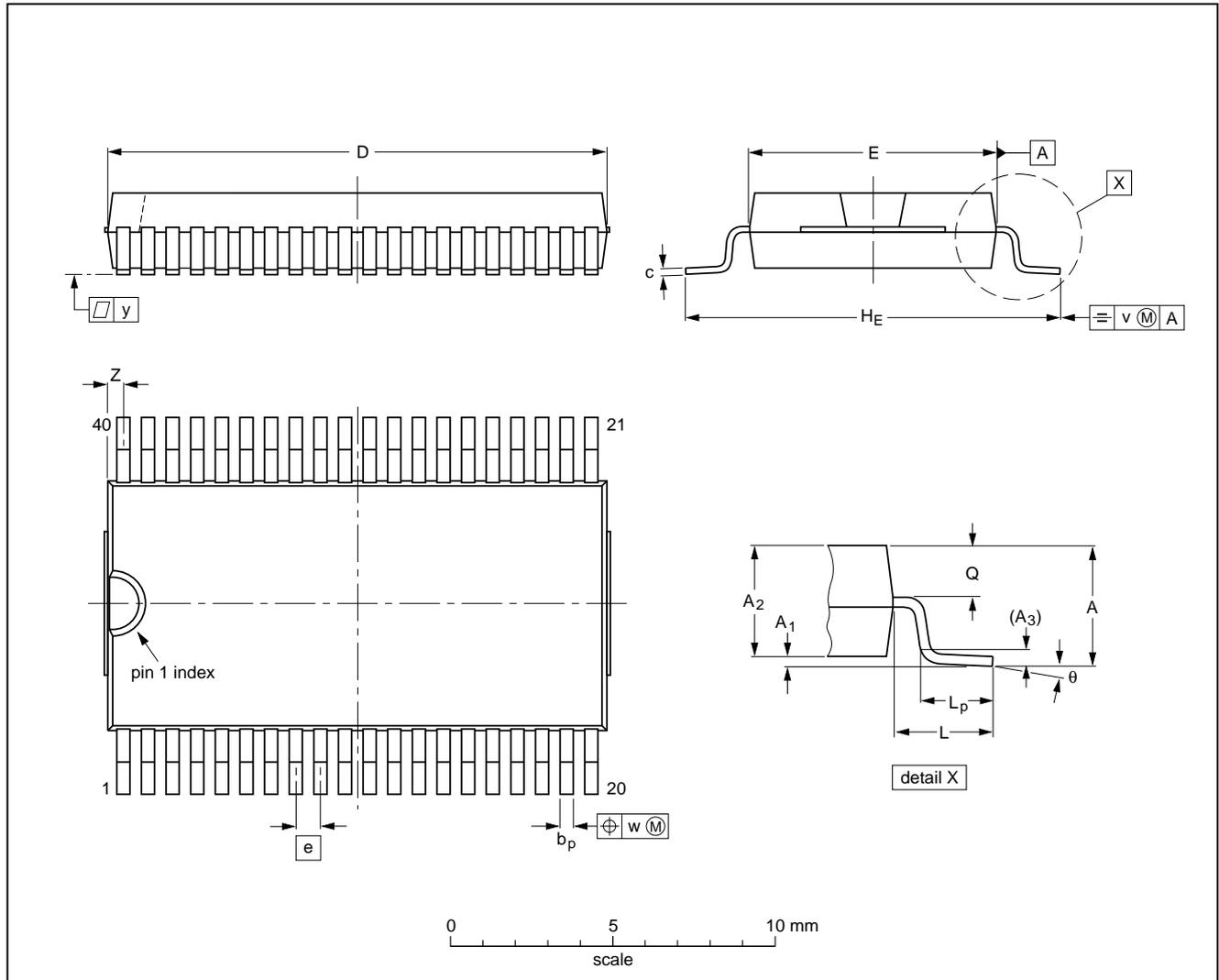
SOT158-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[2]	e	Hₑ	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	2.70	0.3 / 0.1	2.45 / 2.25	0.25	0.42 / 0.30	0.22 / 0.14	15.6 / 15.2	7.6 / 7.5	0.762	12.3 / 11.8	2.25	1.7 / 1.5	1.15 / 1.05	0.2	0.1	0.1	0.6 / 0.3	7° / 0°
inches	0.11	0.012 / 0.004	0.096 / 0.089	0.010	0.017 / 0.012	0.0087 / 0.0055	0.61 / 0.60	0.30 / 0.29	0.03	0.48 / 0.46	0.089	0.067 / 0.059	0.045 / 0.041	0.008	0.004	0.004	0.024 / 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						92-11-17 / 95-01-24

LCD drivers

PCF21XXC family

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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NOTES

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