DATA SHEET

PCE84C486; PCE84C487
Microcontrollers for digital auto-sync and VST TV controller applications

Objective specification
File under Integrated Circuits, IC14

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Philips Semiconductors

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CONTENTS

1 FEATURES

1.1 General

- CMOS 8-bit CPU (enhanced 8048 CPU) with 4 kbytes system ROM and 128 bytes system RAM
- One 8-bit timer/event counter (T1) and one 8-bit counter (T3) triggered by external input
- Three single level vectored interrupt sources: external (INTN), counter/timer and I^2C-bus
- 2 directly testable inputs T0 and T1
- On-chip oscillator clock frequency: 1 to 10 MHz
- On-chip Power-on-reset with low power detector
- The PCE84C486 has eleven quasi-bidirectional I/O lines, the PCE84C487 has twelve. The configuration of each I/O line individually selected by mask option
- Idle and Stop modes for reduced power consumption
- Operating temperature: –25 to +85 °C
- Operating voltage: 4.5 to 5.5 V
- Packages: SDIP32 for the PCE84C486; SDIP42 for the PCE84C487.

1.2 Special

- Master-slave I^2C-bus interface
- Four 6-bit Pulse Width Modulated outputs
- Four 7-bit Pulse Width Modulated outputs
- Four 8-bit Pulse Width Modulated outputs (PCE84C487 only)
- One 14-bit Pulse Width Modulated output
- Two 4-bit Analog-to-Digital Converter (ADC) channels
- 14 derivative I/O ports
- Watchdog Timer.

2 GENERAL DESCRIPTION

The PCE84C486 and PCE84C487 are low-cost microcontrollers and have been designed for use with auto-sync monitors, handling mode detection, digital control and Voltage Synthesized Tuning (VST). These microcontrollers have no on-chip OSD function.

The term PCE84C48X is used throughout this data sheet to refer to both devices. Differences between the PCE84C486 and the PCE84C487 are highlighted throughout the document.

The PCE84C48X is a member of the 84CXXX CMOS microcontroller family. The device uses the PCE84CXX processor core and has 4 kbytes of ROM and 128 bytes of RAM. I/O requirements are catered for with 11 general purpose bidirectional I/O lines (the PCE84C487 has 12) plus 12 function combined I/O lines (the PCE84C487 has 16). Nine PWM analog outputs (the PCE84C487 has 13) are available for analog control purposes and also a two channel 4-bit ADC. The device has an 8-bit counter (T3), for use in pulse counting applications and also an 8-bit timer/counter (T1) with programmable clock. A Watchdog timer, a master-slave I^2C-bus interface and 2 directly testable lines are also available on-chip.

The block diagram of the PCE84C486 is shown in Fig.1; the block diagram of the PCE84C487 is shown in Fig.2.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCE84C486	SDIP32	plastic shrink dual in-line package; 32 leads (400 mil)	SOT232-1
PCE84C487	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1

4 BLOCK DIAGRAMS

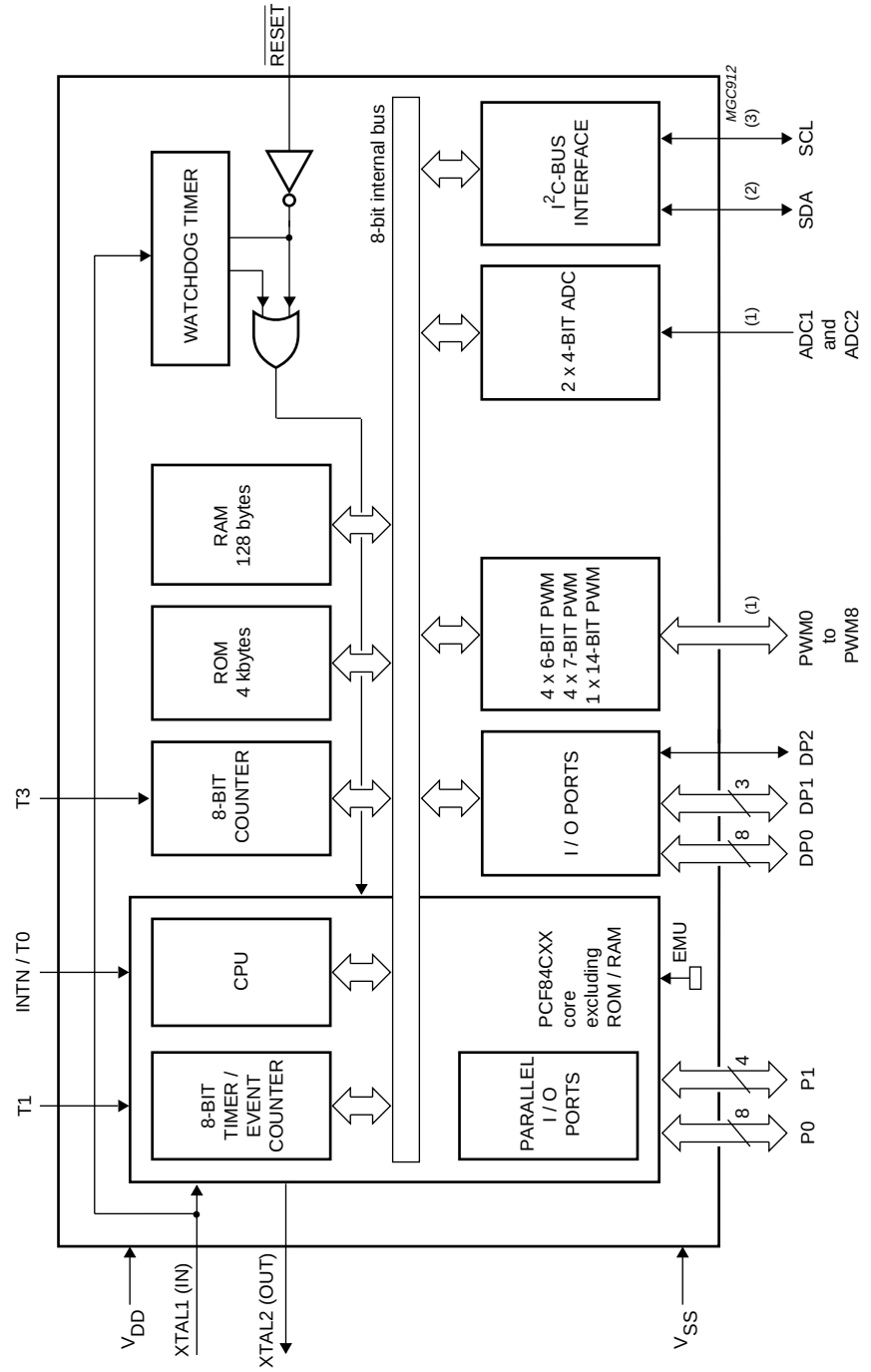


Fig.1 PCE84C486 block diagram.

(1) Alternative functions of DP0 and DP1.
(2) Alternative functions of DP2.
(3) Alternative function of P1.

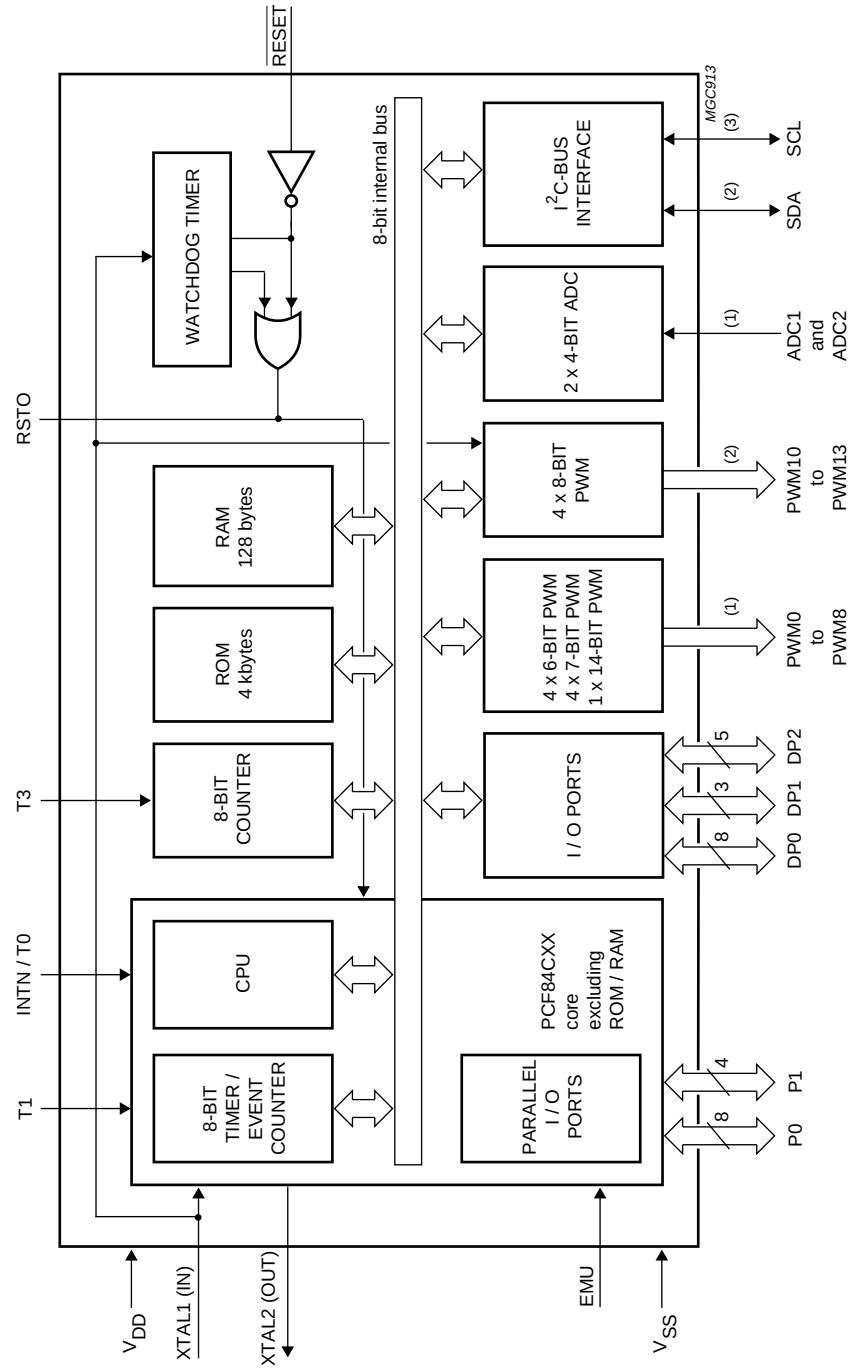


Fig.2 PCE84C487 block diagram.

(1) Alternative functions of DP0 and DP1.
(2) Alternative function of DP2.
(3) Alternative function of P1.

5 PINNING INFORMATION

5.1 Pinning

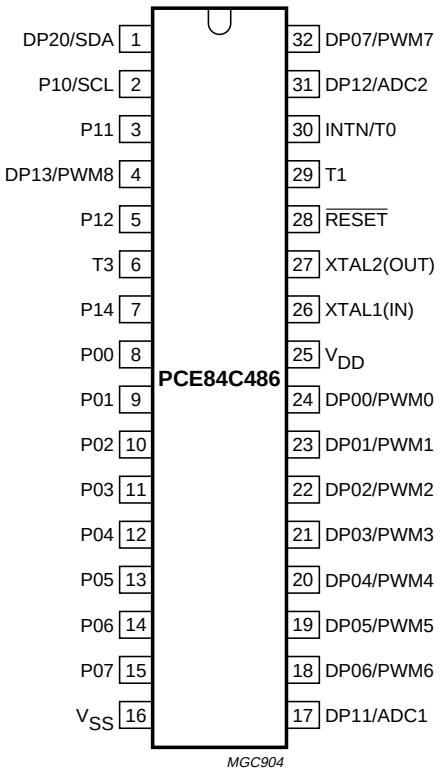


Fig.3 Pin configuration - PCE84C486.

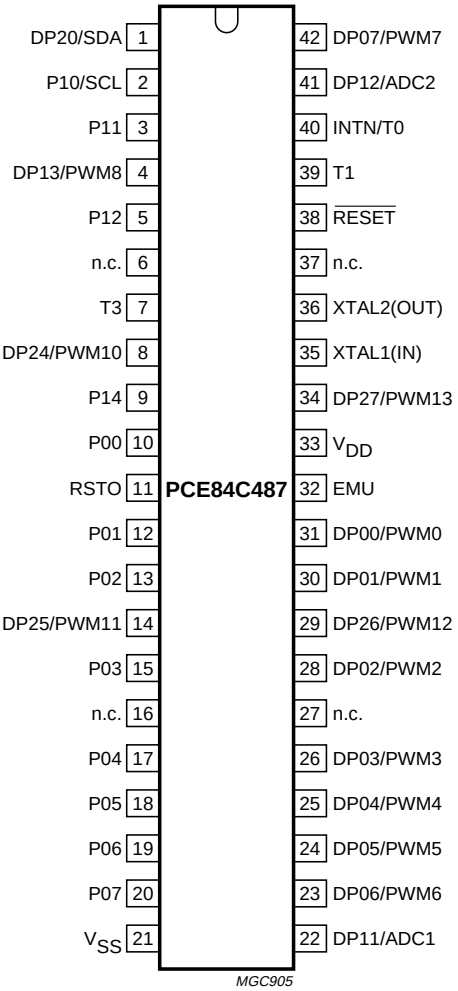


Fig.4 Pin configuration - PCE84C487.

5.2 Pin description

Table 1 SDIP32 package

SYMBOL	PIN	DESCRIPTION
DP20/SDA	1	Derivative port line 20 or I^2C-bus data line.
P10/SCL	2	Port line 10 or I^2C-bus clock line or emulation input $\overline{DXWR}$.
P11	3	Port line 11 or emulation input $\overline{DXRD}$.
DP13/PWM8	4	Derivative I/O port 13 or PWM8 output.
P12	5	Port line 12 or emulation input DXALE.
T3	6	8-bit counter input (Schmitt trigger).
P14	7	Port line 14 or emulation output DXINT.
P00 to P07	8 to 15	General I/O port lines.
V_{SS}	16	Ground pin.
DP11/ADC1	17	Derivative I/O port 11 or ADC Channel 1input.
DP00/PWM0 to DP07/PWM7	24 to 18, 32	Derivative I/O ports or 6 and 7-bit PWM outputs.
V_{DD}	25	Power supply.
XTAL1 (IN)	26	Oscillator input pin for system clock.
XTAL2 (OUT)	27	Oscillator output pin for system clock.
$\overline{RESET}$	28	Reset input; active LOW input initializes device.
T1	29	Direct testable pin or event counter input.
INTN/T0	30	External interrupt or direct testable pin.
DP12/ADC2	31	Derivative I/O port 12 or ADC Channel 2 input.

Table 2 SDIP42 package

SYMBOL	PIN	DESCRIPTION
DP20/SDA	1	Derivative port line 20 or I^2C-bus data line.
P10/SCL	2	Port line 10 or I^2C-bus clock line or emulation input $\overline{DXWR}$.
P11	3	Port line 11 or emulation input $\overline{DXRD}$.
DP13/PWM8	4	Derivative I/O port 13 or PWM8 output.
P12	5	Port line 12 or emulation input DXALE.
n.c.	6	Not connected.
T3	7	8-bit counter input (Schmitt trigger).
DP24/PWM10 to DP27/PWM13	8, 14, 29, 34	Derivative I/O ports or 8-bit PWM outputs.
P14	9	Port line 14 or emulation output DXINT.
P00 to P07	10, 12, 13, 15, 17, 18, 19, 20	General I/O port lines.
RSTO	11	Used for emulation purposes only. This active HIGH output is the result of the OR operation carried out internally on the $\overline{RESET}$ input and the Watchdog Timer reset line.
n.c.	16	Not connected.
V_{SS}	21	Ground pin.
DP11/ADC1	22	Derivative I/O port 11 or ADC channel 1 input.
DP04/PWM4 to DP07/PWM7	25, 24, 23, 42	Derivative I/O ports or 6-bit PWM outputs.
n.c.	27	Not connected.
DP00/PWM0 to DP03/PWM3	31, 30, 28, 26	Derivative I/O ports or 7-bit PWM outputs.
EMU	32	Emulation mode control input, normally LOW.
V_{DD}	33	Power supply.
XTAL1 (IN)	35	Oscillator input pin for system clock.
XTAL2 (OUT)	36	Oscillator output pin for system clock.
n.c.	37	Not connected.
$\overline{RESET}$	38	Reset input; active LOW input initializes device.
T1	39	Direct testable pin or event counter input.
INTN/T0	40	External interrupt or direct testable pin.
DP12/ADC2	41	Derivative I/O port 12 or ADC Channel 2 input.

6 RESET

To initialize the microcontroller to a defined state a reset operation is performed. A reset can be generated in three ways:

- applying an external signal to the $\overline{\text{RESET}}$ pin
- via Power-on-reset circuitry
- by the Watchdog Timer.

6.1 External reset using the $\overline{\text{RESET}}$ pin

An active LOW signal from an external logic device will reset the device. The signal must be maintained long enough to allow V_{DD} to reach its f_{xtal}-dependent minimum operating voltage.

6.2 Power-on-reset

A Power-on-reset can be generated using an external RC circuit. To avoid overload of the internal diode, an external diode should be added in parallel if $C_{RESET} \geq 2.2\ \mu F$. The RC circuit is shown in Fig.5.

6.3 Watchdog Timer reset

An overflow of the Watchdog Timer will cause the device to be reset. The operation of the Watchdog Timer is described in Chapter 12.

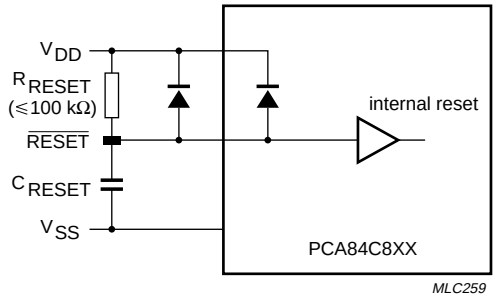


Fig.5 External components for $\overline{\text{RESET}}$ pin.

6.4 Reset trip level

The RESET trip voltage level for both the PCE84C486 and PCE84C487 is masked to 1.3 V.

6.5 Reset status

- Derivative Registers reset status; see Table 8 for details
- Program Counter 00H
- Memory Bank 0
- Register Bank 0
- Stack Pointer 00H
- All interrupts disabled
- Timer/event counter 1 stopped and cleared
- Timer pre-scaler modulo-32 (PS = 0)
- Timer flag cleared
- Serial I/O interface disabled (ESO = 0) and in slave receiver mode
- Idle and Stop mode cleared.

7 ANALOG (DC) CONTROL

The PCE84C486 has nine Pulse Width Modulated outputs (PWM0 to PWM8) and the PCE84C487 has thirteen Pulse Width Modulated outputs (PWM0 to PWM8 and PWM10 to PWM13). These outputs are used for analog control purposes e.g. brightness, contrast, H-shift, V-shift, H-width, V-size, pin-cushion, trapezium, R (or G or B) gain control, sound volume etc. Each PWM output generates a pulse pattern with a programmable duty cycle.

The PWM outputs are specified below:

- PWM0 to PWM3: 4 PWM outputs with 7-bit resolution
- PWM4 to PWM7: 4 PWM outputs with 6-bit resolution
- PWM8: 1 PWM output with 14-bit resolution
- PWM10 to PWM13: 4 PWM outputs with 8-bit resolution.

The 6 and 7-bit PWM outputs are described in Section 7.1; the 8-bit PWM outputs are described in Section 7.2 and the 14-bit PWM output is described in Section 7.3. A typical PWM output application is described in Section 7.4.

7.1 6 and 7-bit PWM outputs

The block diagram for the 6 and 7-bit PWM outputs is shown in Fig.6.

Pulse Width Modulated outputs PWM0 to PWM7 share the same pins as Derivative Port lines DP00 to DP07, respectively. Selection of the pin function as either a PWM output or a Derivative Port line is achieved using the appropriate PWMnE bit in the PWME1 Register (see Table 8).

The polarity of the 6 and 7-bit PWM outputs is programmable and is selected by the P7LVL or the P6LVL bit in the CON2 Register (see Table 8). The state of the P7LVL bit determines the polarity of the 7-bit PWMs; the state of the P6LVL bit determines the polarity of the 6-bit PWMs.

The duty cycle of each PWM output is dependent upon the programmable contents of its associated data latch (PWM0 to PWM7 Registers respectively). As the clock frequency of each PWM circuit is $\frac{1}{3} \times f_{xtal}$, the pulse width of the pulse generated can be calculated as shown below.

$$\text{Pulse width} = \frac{3 \times (\text{PWMn})}{f_{xtal}}$$

Where (PWMn) is the decimal value held in the data latch.

The maximum repetition frequency (f_{PWM}) of the 6 and 7-bit PWM outputs is shown below.

For the 6-bit PWM outputs: $f_{PWM} = \frac{f_{xtal}}{192}$

For the 7-bit PWM outputs: $f_{PWM} = \frac{f_{xtal}}{384}$

7.2 8-bit PWM outputs

The block diagram for the 8-bit PWM outputs is shown in Fig.8.

The 8-bit PWM outputs PWM10 to PWM13 (only available with the PCE84C487) share the same pins as Derivative Port lines DP24 to DP27, respectively. Selection of the pin function as either a PWM output or a Derivative Port line is achieved using the appropriate PWMnE bit in the PWME2 Register (see Table 8). In the PCE84C486 the contents of the PWME2 register should be set so that these PWM outputs are disabled (i.e 00H).

The polarity of the 8-bit PWM outputs is programmable and is selected by the P8LVL bit in the CON2 Register.

The duty cycle of each 8-bit PWM output is dependent upon the programmable contents of its associated data latch (PWM10 to PWM13 Registers respectively). As the clock frequency of each PWM circuit is f_{xtal}, the pulse width of the pulse generated can be calculated as shown below.

$$\text{Pulse width} = \frac{(\text{PWMn})}{f_{xtal}}$$

Where (PWMn) is the decimal value held in the data latch.

The maximum repetition frequency (f_{PWM}) of the 8-bit PWM outputs is shown below.

$$f_{PWM} = \frac{f_{xtal}}{256}$$

An 8-bit PWM output is driven HIGH when the value held in its data latch is 00H. This is different to the 6 and 7-bit PWM outputs which are driven LOW when their data latches contain 00H.

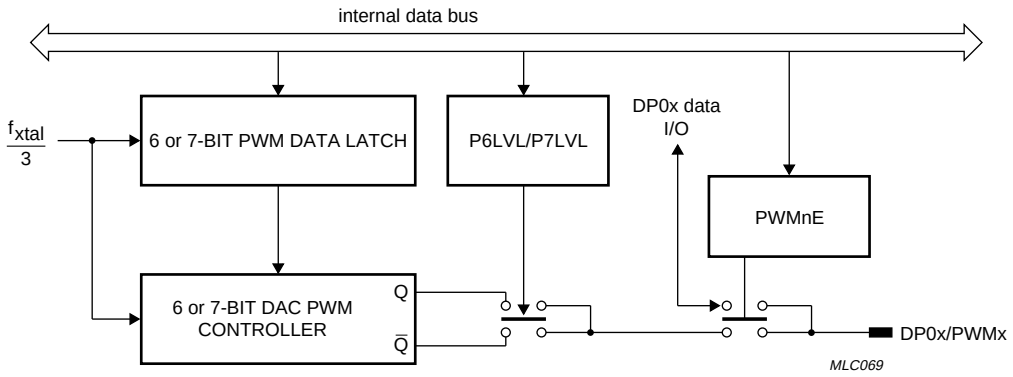


Fig.6 Block diagram for 6 and 7-bit PWMs.

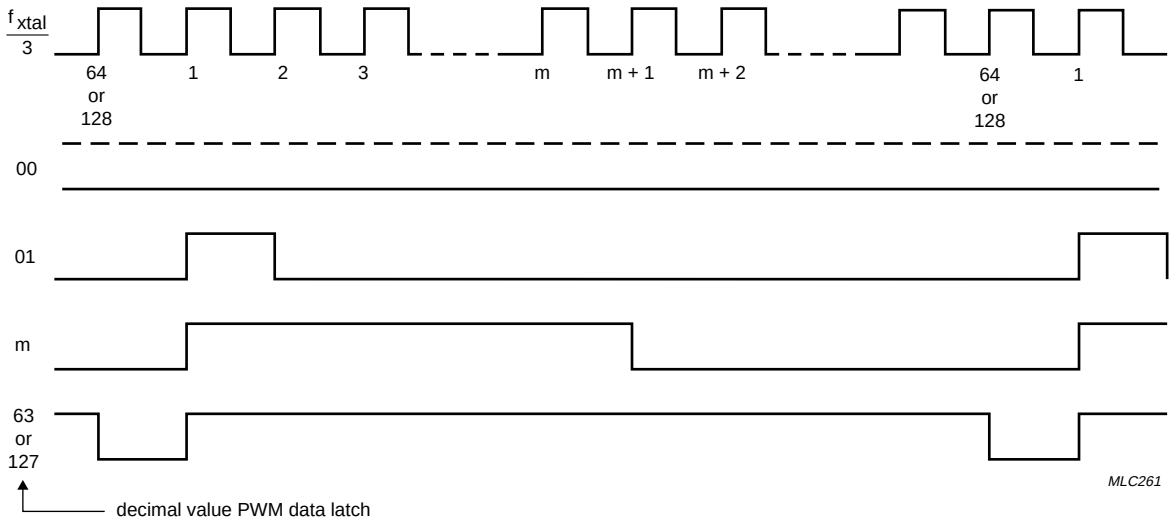


Fig.7 Typical non-inverted output pulse patterns for 6 or 7-bit PWM outputs.

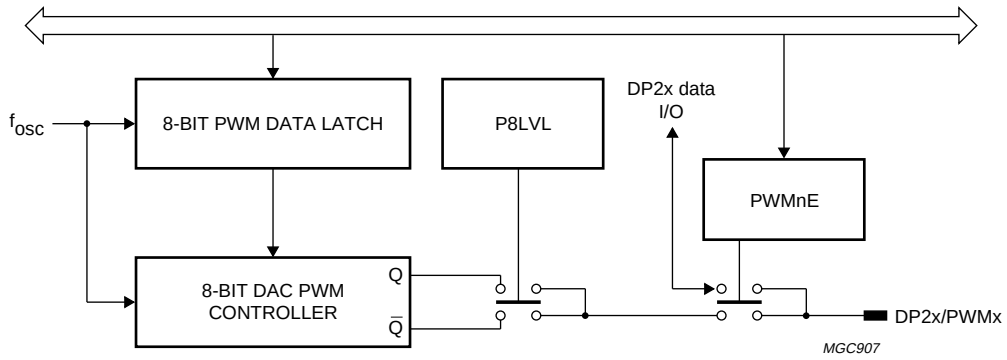


Fig.8 Block diagram for 8-bit PWMs.

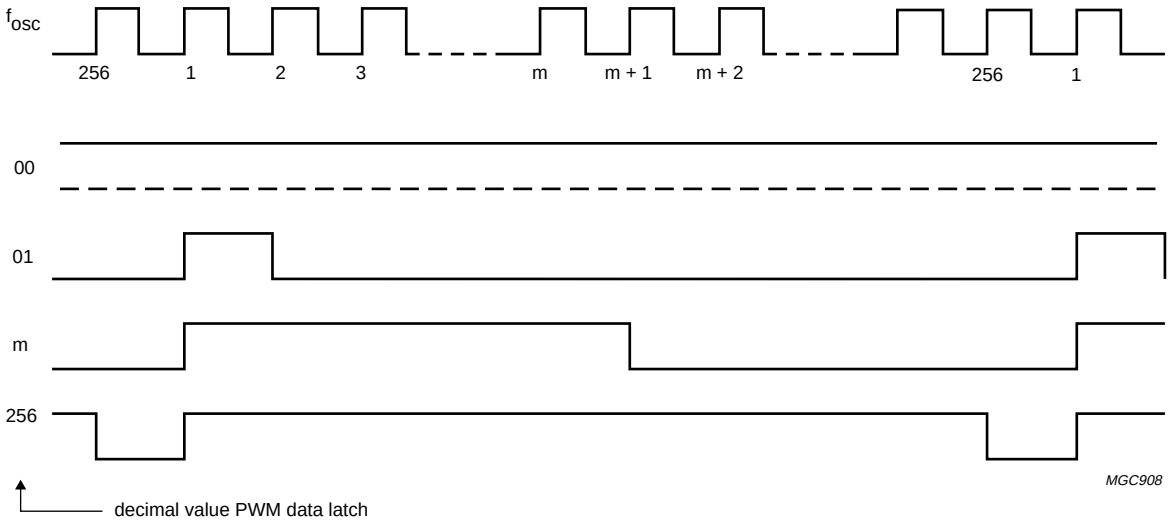


Fig.9 Typical non-inverted output pulse patterns for 8-bit PWM outputs.

7.3 14-bit PWM output (PWM8)

The 14-bit PWM output can be used to generate the Automatic Frequency Control (AFC) signal used in VST applications.

PWM8 shares the same pin as Derivative Port line DP13. Selection of the pin function as either a PWM output or as a Derivative Port line is achieved using the PWM8E bit in Register 22.

The Block diagram for the 14-bit PWM output is shown in Fig.10 and comprises:

- Two 7-bit latches: PWM8L (Register 18) and PWM8H (Register 19)
- 14-bit data latch (PWMREG)
- 14-bit counter
- Coarse pulse controller
- Fine pulse controller
- Mixer.

Data is loaded into the 14-bit data latch (PWMREG) from the two 7-bit data latches (PWM8H and PWM8L) when PWM8L is written to. The contents of PWMREG determine the active time of the PWM8 output. The upper seven bits of PWMREG are used by the coarse pulse controller and determine the coarse pulse width; the lower seven bits are used by the fine pulse controller and determine in which subperiods fine pulses will be added. The outputs OUT1 and OUT2 of the coarse and fine pulse controllers are 'ORED' in the mixer to give the PWM8 output. The polarity of the PWM8 output is programmable and is selected by the P8LVL bit in Register 23.

As the 14-bit counter is clocked by $\frac{1}{3} \times f_{xtal}$, the repetition times of the coarse and fine pulse controllers may be calculated as shown below.

Coarse controller repetition time: $t_{sub} = \frac{384}{f_{xtal}}$

Fine controller repetition time: $t_r = \frac{49152}{f_{xtal}}$

Figure 11 shows typical PWM8 outputs, with coarse adjustment only, for different values held in PWM8H. Note that the PWM8 coarse controller output is the same as the 7-bit PWM outputs except the polarity is reversed.
Figure 12 shows typical PWM8 outputs, with coarse and fine adjustment, after the coarse and fine pulse controller outputs have been 'ORED' by the mixer.

7.3.1 Coarse adjustment

An active HIGH pulse is generated in every subperiod; the pulse width being determined by the contents of PWM8H. The coarse output (OUT1) is LOW at the start of each subperiod and will remain LOW until the time $[3/f_{xtal} \times (PWM8H + 1)]$ has elapsed. The output will then go HIGH and remain HIGH until the start of the next subperiod. The coarse pulse width may be calculated as shown below.

$$\text{Pulse duration} = (127 - PWM8H) \times \frac{3}{f_{xtal}}$$

7.3.2 Fine adjustment

Fine adjustment is achieved by generating an additional pulse in specific subperiods. The pulse is added at the start of the selected subperiod and has a pulse width of $3/f_{xtal}$. The contents of PWM8L determine in which subperiods a fine pulse will be added. It is the logic 0 state of the value held in PWM8L that actually selects the subperiods. When more than one bit is a logic 0 then the subperiods selected will be a combination of those subperiods specified in Table 3. For example, if PWM8L = 111 1010 then this is a combination of:

- PWM8L = 111 1110: subperiod 64 and
- PWM8L = 111 1011: subperiods 16, 48, 80 and 112.

Pulses will be added in subperiods 16, 48, 64, 80 and 112. This example is illustrated in Fig.13.

When PWM8L holds 111 1111 fine adjustment is inhibited and the PWM8 output is determined only by the contents of PWM8H.

Table 3 Additional pulse distribution

PWM8L	ADDITIONAL PULSE IN SUBPERIOD
111 1110	64
111 1101	32 and 96
111 1011	16, 48, 80 and 112
111 0111	8, 24, 40, 56, 72, 88, 104 and 120
110 1111	4, 12, 20, 28, 36, 44, 52...116 and 124
101 1111	2, 6, 10, 14, 18, 22, 26, 30...122 and 126
011 1111	1, 3, 5, 7, 9, 11, 13, 15, 17...125 and 127

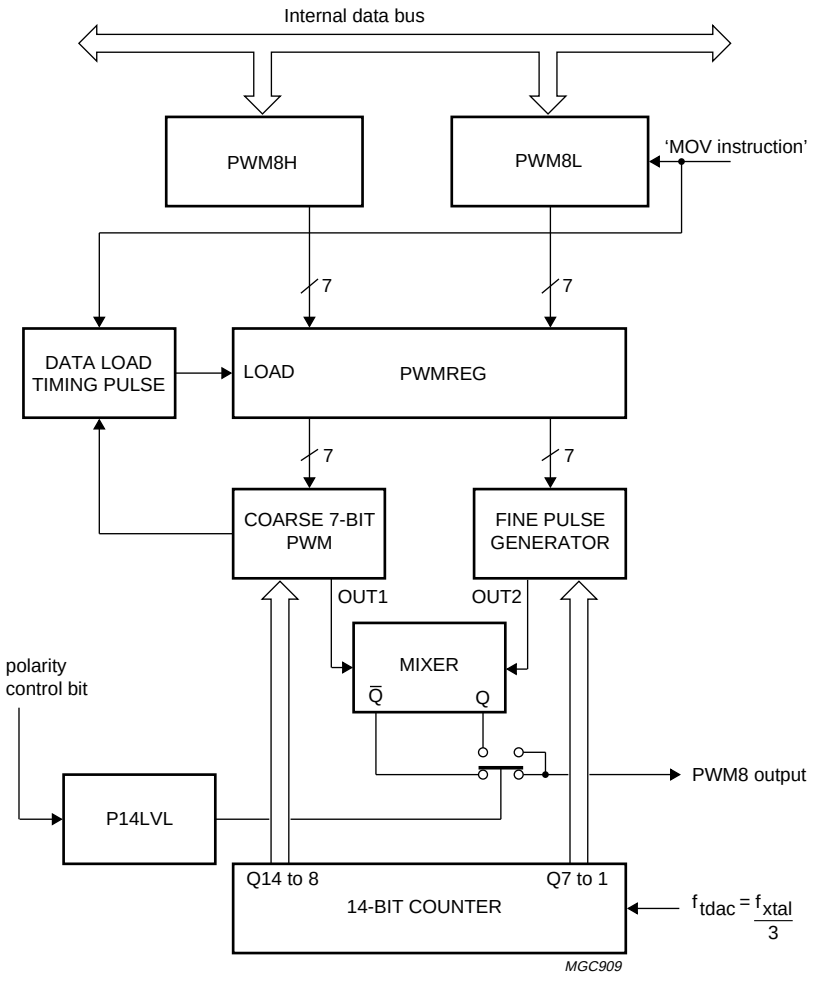


Fig.10 14-bit PWM Block diagram.

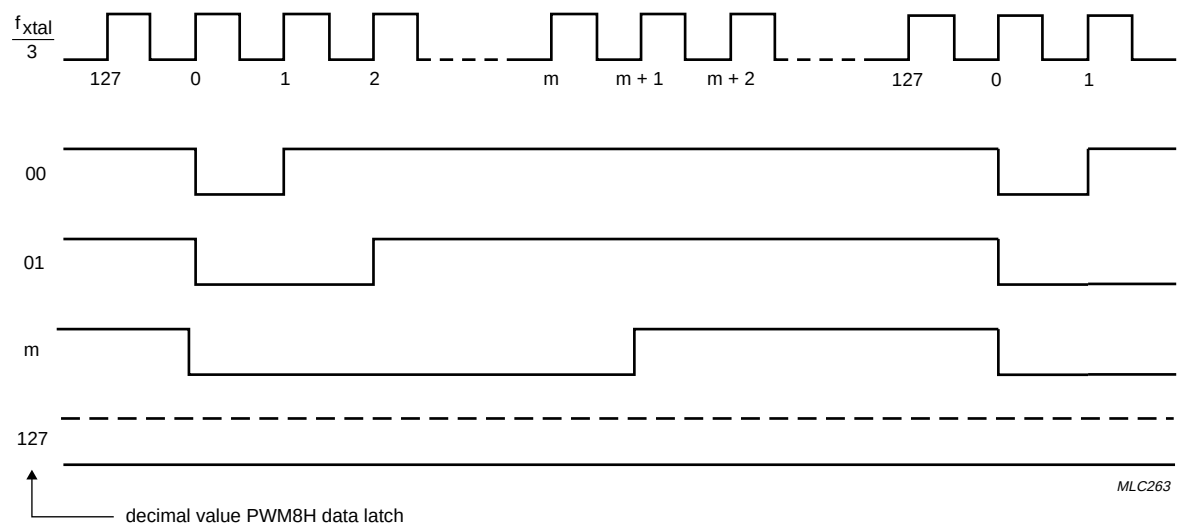


Fig.11 Non-inverted PWM8 output patterns - Coarse adjustment only.

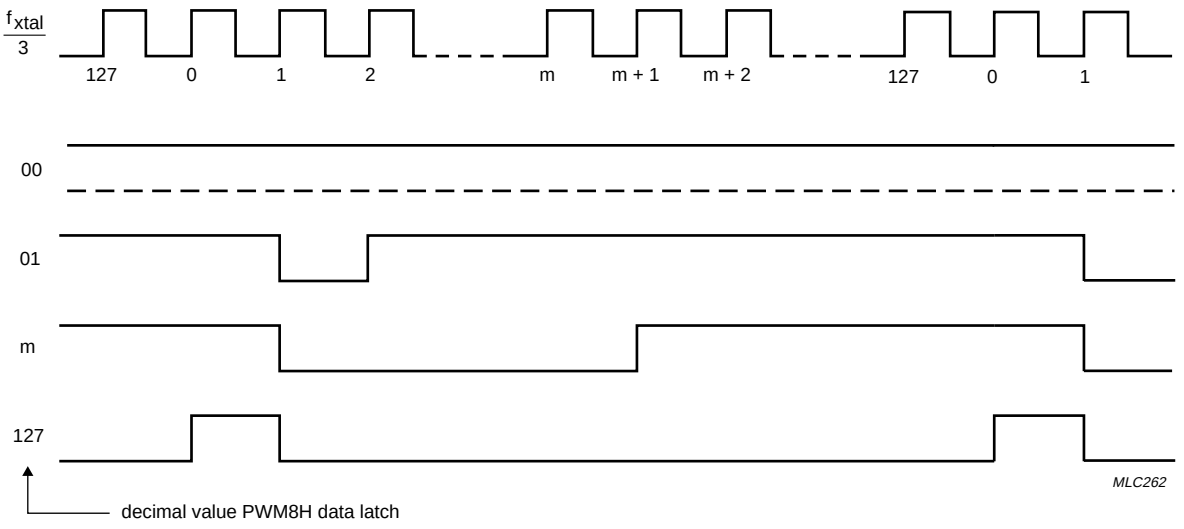


Fig.12 Non-inverted PWM8 output patterns - Coarse and Fine adjustment.

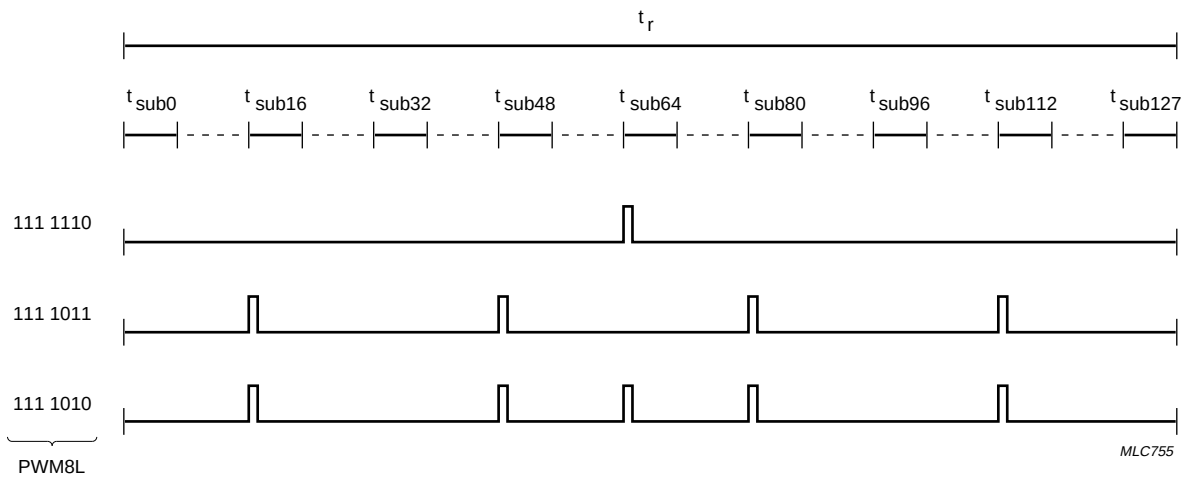


Fig.13 Fine adjustment output (OUT2).

7.4 A typical PWM output application

A typical PWM application is shown in Fig.14. R1 and C1 form an integration network the time constant of which should be at least 5 times greater than the repetition period of the PWM output pattern. In order to smooth a changing PWM output a high value of C1 should be chosen. The value of C1 will normally be in the range 1 to 10 μF. The potential divider chain formed by R2 and R3 is used only when the output voltage is to be offset. The output voltages for this application are calculated using Equations (1) and (2).

$$V_{max} = \frac{R3 \times \text{supply voltage}}{R3 + \frac{R1 \times R2}{R1 + R2}} \quad (1)$$

$$V_{min} = \frac{\frac{R1 \times R3}{R1 + R3} \times \text{supply voltage}}{R2 + \frac{R1 \times R3}{R1 + R3}} \quad (2)$$

The loop from the PWM pin through R1 and C1 to V_{SS} will radiate high frequency energy pulses. In order to limit the effect of this unwanted radiation source, the loop should be kept short and a high value of R1 selected. The value of R1 will normally be in the range 3.3 to 100 kΩ. It is good practice to avoid sharing V_{SS} with the return leads of other sensitive signals.

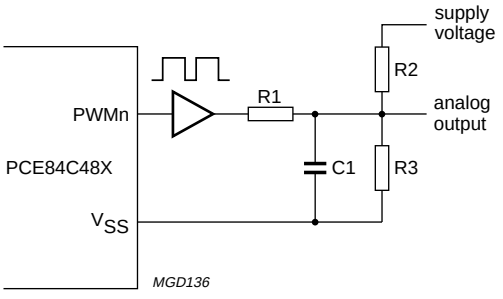


Fig.14 Typical PWM output circuit.

8 ANALOG-TO-DIGITAL CONVERTER (ADC)

The two-channel ADC comprises a 4-bit Digital-to-Analog Converter (DAC); a comparator; an analog channel selector and control circuitry. As the digital input to the 4-bit DAC is loaded by software (a subroutine in the program), it is known as a software ADC. The block diagram is shown in Fig.15.

The ADC inputs ADC1 and ADC2 share the same pins as Derivative Port lines DP11 and DP12 respectively. Selection of the pin function as either an ADC input or as a Derivative Port line is achieved using bits ADCE1 and ADCE2 in Register 22. When ADCEn = 1, the ADC function is enabled.

The 4-bit DAC analog output voltage (V_{ref}) is determined by the decimal value of the data held in bits DAC0 to DAC3 of Register 20. V_{ref} is calculated as shown in Equation (3) and Table 4 lists the V_{ref} values assuming V_{DD} = 5 V.

$$V_{ref} = \frac{V_{DD}}{16} \times (\text{DAC value} + 1) \quad (3)$$

When the analog input voltage is higher than V_{ref}, the COMP bit in Register 20 will be HIGH.

Table 4 Selection of V_{ref}

DAC3	DAC2	DAC1	DAC0	V_{ref} (V)
0	0	0	0	0.3125
0	0	0	1	0.6250
0	0	1	0	0.9375
0	0	1	1	1.2500
0	1	0	0	1.5625
0	1	0	1	1.8750
0	1	1	0	2.1875
0	1	1	1	2.5000
1	0	0	0	2.8125
1	0	0	1	3.1250
1	0	1	0	3.4375
1	0	1	1	3.7500
1	1	0	0	4.0625
1	1	0	1	4.3750
1	1	1	0	4.6875
1	1	1	1	5.0000

The ADC channel selector is controlled by the ADCS1 and ADCS0 bits in Register 20. The channels are selected as shown in Table 5.

Table 5 Selection of ADC channel

ADCS1	ADCS0	CHANNEL SELECTED
0	0	not allowed
0	1	ADC1
1	0	ADC2
1	1	not allowed

8.1 Conversion algorithm

There are many algorithms available to achieve the ADC conversion. The algorithm described below and shown in Fig.16 uses an iteration process.

1. Enable and then select the ADC channel for conversion. Channel selection is achieved using bits ADCS1 and ADCS0 in Register 20.
2. Set the digital input to the DAC to 1000. The digital input to the DAC is selected using bits DAC3 to DAC0 in Register 20.
3. Determine the result of the compare operation. This is achieved by reading the COMP bit in Register 20 using the instruction MOV A, D20H. If COMP = 1; the analog input voltage is higher than the reference voltage (V_{ref}). If COMP = 0; the analog input voltage is lower than the reference voltage (V_{ref}).
4. If COMP = 1; then the analog input voltage is higher than the reference voltage (V_{ref}) and therefore the digital input to the DAC needs to be increased. Set the input to the DAC to 1100.
5. If COMP = 0; then the analog input voltage is lower than the reference voltage (V_{ref}) and therefore the digital input to the DAC needs to be decreased. Set the input to the DAC to 0100.
6. Determine the result of the compare operation by reading the COMP bit in Register 20.

7. For the DAC = 1100 case

   If COMP = 1; then the analog input voltage is still greater than V_{ref} and therefore the digital input to the DAC needs to be increased again. Set the input to the DAC to 1110.

   If COMP = 0; then the analog input voltage is now less than V_{ref} and therefore the digital input to the DAC needs to be decreased. Set the input to the DAC to 1010

8. For the DAC = 0100 case

   If COMP = 1; then the analog input voltage is now greater than V_{ref} and therefore the digital input to the DAC needs to be increased. Set the input to the DAC to 0110.

   If COMP = 0; then the analog input voltage is still lower than V_{ref} and therefore the digital input to the DAC needs to be decreased again. Set the input to the DAC to 0010.

9. The operations detailed in 6, 7 and 8 above are repeated and each time the digital input to the DAC is changed accordingly; as dictated by the state of the COMP bit. The complete process is shown in Fig.16. Each time the DAC input is changed the number of values which the analog input can take is reduced by half. In this manner the actual analog value is honed into. The value of the analog input (V_A) is determined using Equation (4):

$$V_A = \frac{V_{DD}}{16} \times (\text{DAC value} + 1) \quad (4)$$

As the conversion time of each compare operation is greater than 6 μs but less than 9 μs; a NOP instruction is recommended to be used in between the instructions that change the value of V_{ref}; select the ADC channel and read the COMP bit.

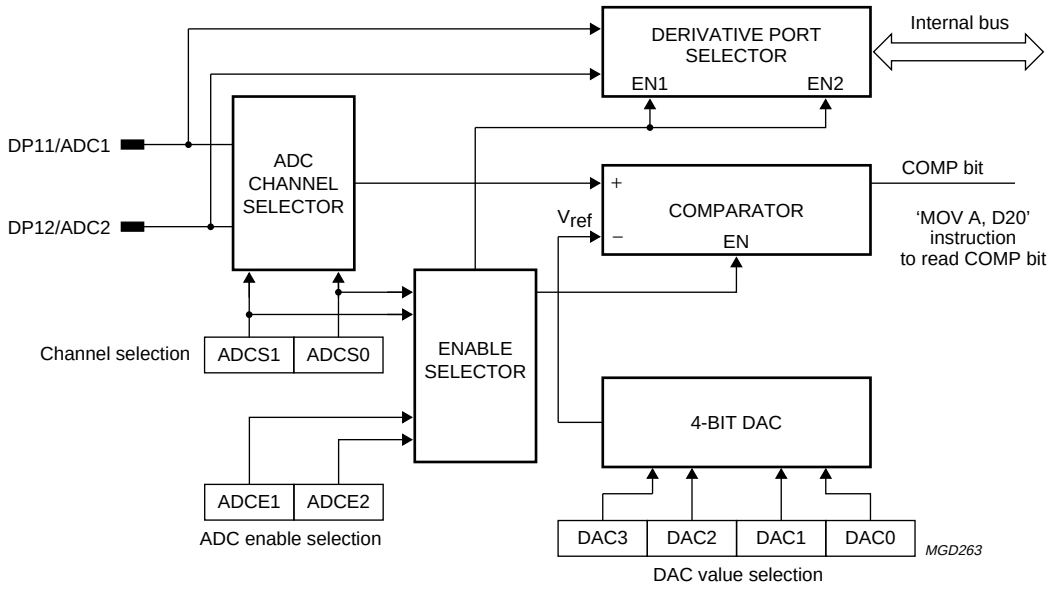


Fig.15 Block diagram of 2 channel ADC.

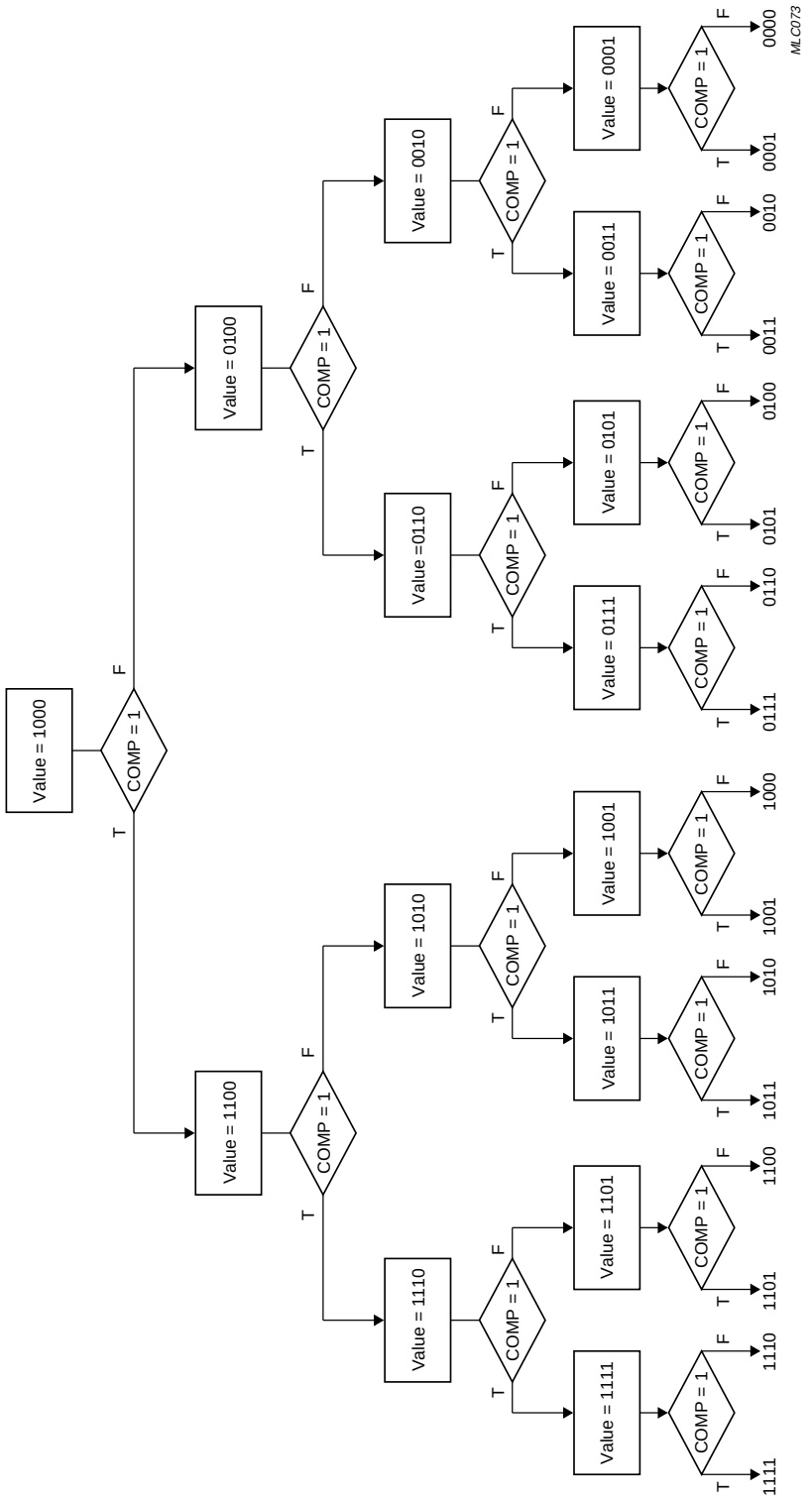


Fig.16 Example of converting algorithm for software ADC.

8.2 A typical application for keypad detection

The ADC channels of the PCE84C48X can be used in keypad applications to detect and identify the operation of individual keys. The circuit for a 14-key application is shown in Fig.17.

When no key is depressed the input voltage at the ADC input pin will be greater than $^{15}/_{16}V_{DD}$ and if the DAC value selected is 1110 then the COMP bit will be HIGH. When any key is depressed the input voltage at the ADC input pin will change, and as each key will generate its own unique input voltage, this can be measured by the ADC channel and the actual key depressed can then be identified.

The input voltage generated by the operation of any key (ignoring the effect of the 100 kΩ resistor) can be calculated as follows:

$$V_{ADCn} = \left[\frac{(n-0.5)}{16}\right] \times V_{DD}$$

Where n is the key number and can take any integer value in the range 1 to 14.

The input voltage at the ADC input will be influenced by the tolerance of the resistors and the length of the cable connecting the keypad to the monitor. In the worse case situation this may reduce the number of keys that can be uniquely detected and identified.

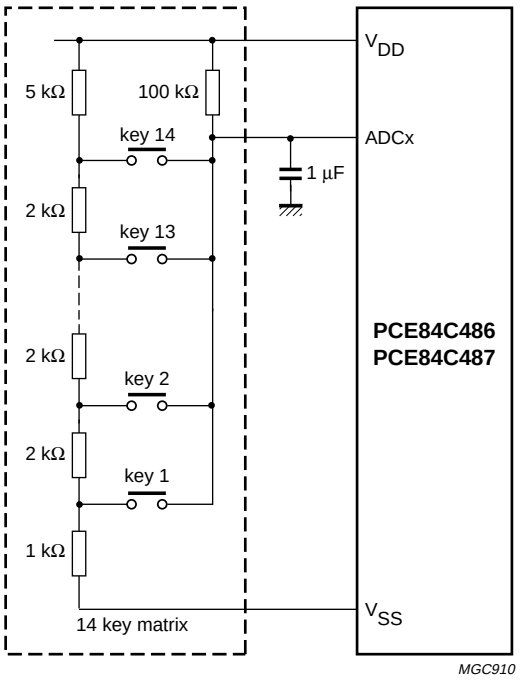


Fig.17 A typical ADC application for keypad detection.

9 I²C-BUS INTERFACE

The PCE84C48X has an on-chip I²C-bus interface that can be used in master or slave mode. Full details of the I²C-bus are given in the document *"The I²C-bus and how to use it"*. This document may be ordered using the code 9398 393 40011.

The I²C-bus interface lines SDA and SCL share the same pins as port lines DP20 and P10 respectively. Selection of the pin function as either an I²C-bus line or a port line is achieved using the SDAE and SCLE bits in Derivative Register 22. Only port Option 2 is available for both of these pins.

10 8-BIT COUNTER (T3)

The main application for this counter is in the frequency measurement of the Hsync signal.

The block diagram of the 8-bit counter is shown in Fig.22. A Schmitt trigger is used at the input for noise rejection and also to shape the input signal into a square wave. The T3 input is sampled at a frequency of $\frac{1}{3} \times f_{osc}$ by the sample clock which synchronizes the internal T3 clock and the read operation of Derivative Register 24. The rising edge of the input increments the ripple counter by 1.

The contents of T3 may be read using the instruction MOV A, D24H. As soon as the data is read, the counter is reset to zero. A counter overflow or Power-on-reset also resets the counter contents to zero.

If the rising and falling edges of the input pulse are less than 30 ns then the minimum pulse width that the T3 input will recognise is $3/f_{osc}$ + 100 ns. If the system clock is 10 MHz then the minimum pulse width is 400 ns. In some display modes, the active pulse width of the Hsync signal can be less than 400 ns; in this situation some external application circuitry may be required.

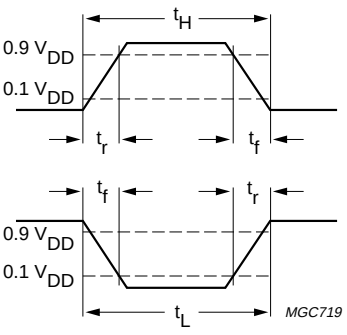


Fig.18 T3 input waveform.

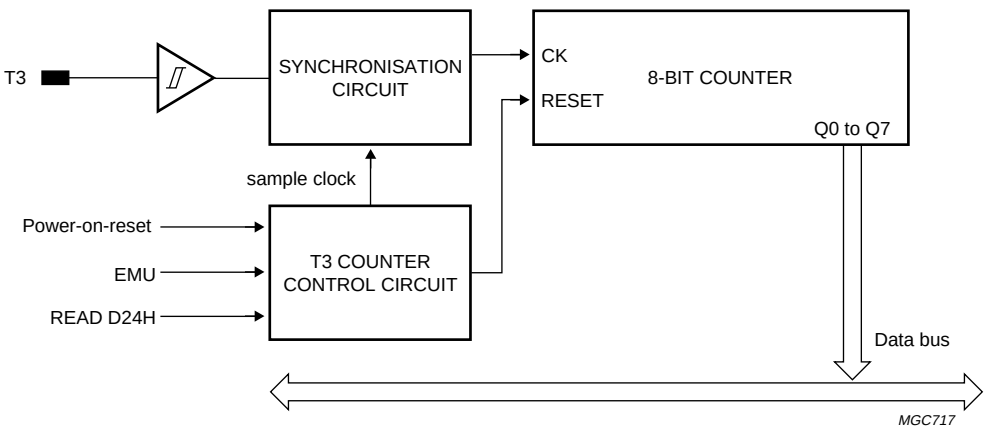


Fig.19 Block diagram of the 8-bit counter (T3).

11 WATCHDOG TIMER (WDT)

The purpose of the Watchdog Timer is to reset the microcontroller, within a reasonable period of time, if it enters an erroneous processor state. Erroneous processor states can be caused by noise or RFI.

The Watchdog Timer consists of a 23-bit counter which is clocked at a frequency of f_{osc}. During a Power-on-reset the contents of the counter are cleared. The counter contents are then incremented by '1' every oscillator clock cycle. If the maximum count is exceeded, the counter overflows and the microcontroller is reset. In order to prevent a counter overflow and its resulting reset operation, the user program must clear the contents of the Watchdog Timer before its maximum count is exceeded. During normal processing, the contents of the Watchdog Timer are cleared by writing a logic 1 to Derivative Register 45H (this is a dummy register).

The maximum time period (t_p) which the counter may run and not cause a reset operation, is calculated as shown below.

$$t_p = \frac{1}{f_{osc}} \times 2^{22}$$

In the Idle mode the oscillator is still running and the Watchdog Timer remains active. In the Stop mode however, the oscillator is stopped and the operation of the Watchdog Timer is halted but its contents are retained. Therefore, it may be advisable for the user to clear the contents of the Watchdog Timer before the Stop mode is entered, in order to avoid an unexpected reset operation after the device is woken-up.

The operational voltage range of the Watchdog Timer is 2 to 5.5 V.

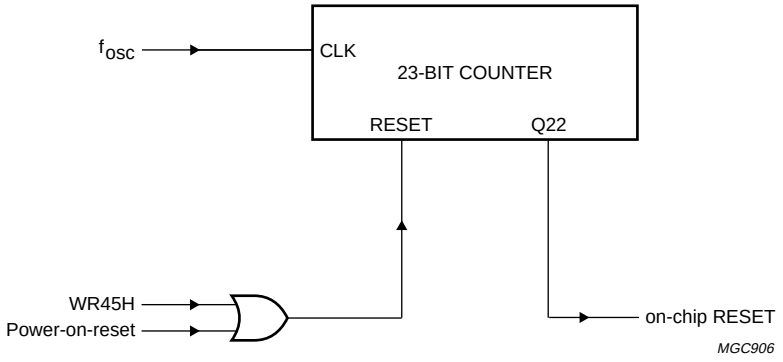


Fig.20 The Watchdog Timer.

12 OUTPUT PORTS

Each I/O port line may be individually configured using one of three mask options. The three I/O mask options are specified below:

Option 1 Standard input/output with switched pull-up current source; this is shown in Fig.24.

Option 2 Input/output with open-drain output; this is shown in Fig.25.

Option 3 Push-pull output; this is shown in Fig.26.

The state of each output port after a Power-on-reset can also be selected using the mask options. All port mask options are given in Section 13.1.

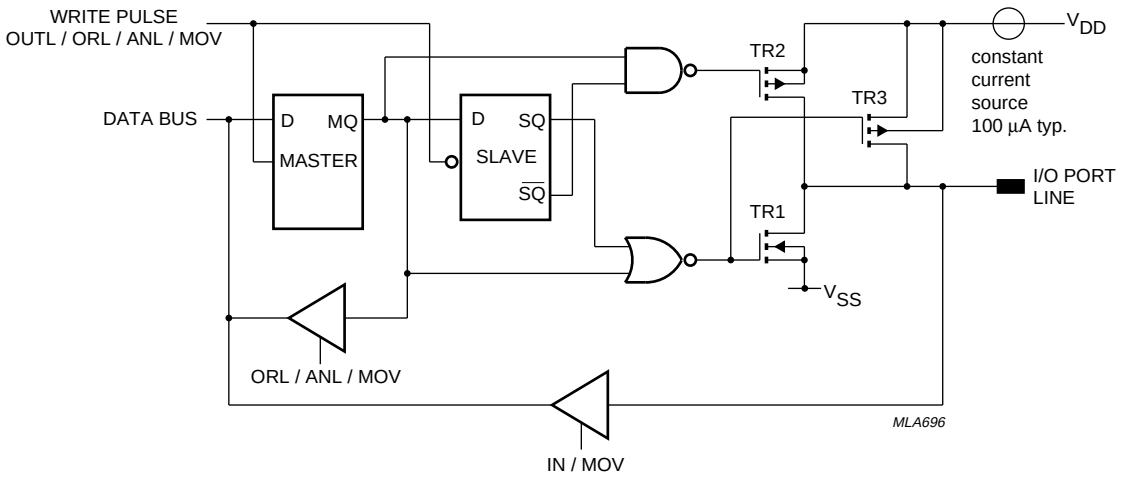


Fig.21 Standard I/O with pull-up transistor source (Option 1).

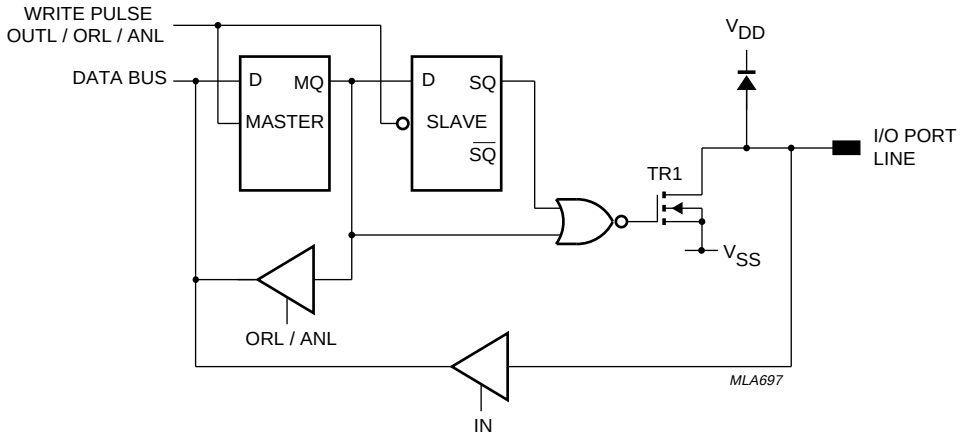


Fig.22 Open-drain I/O without pull-up transistor (Option 2).

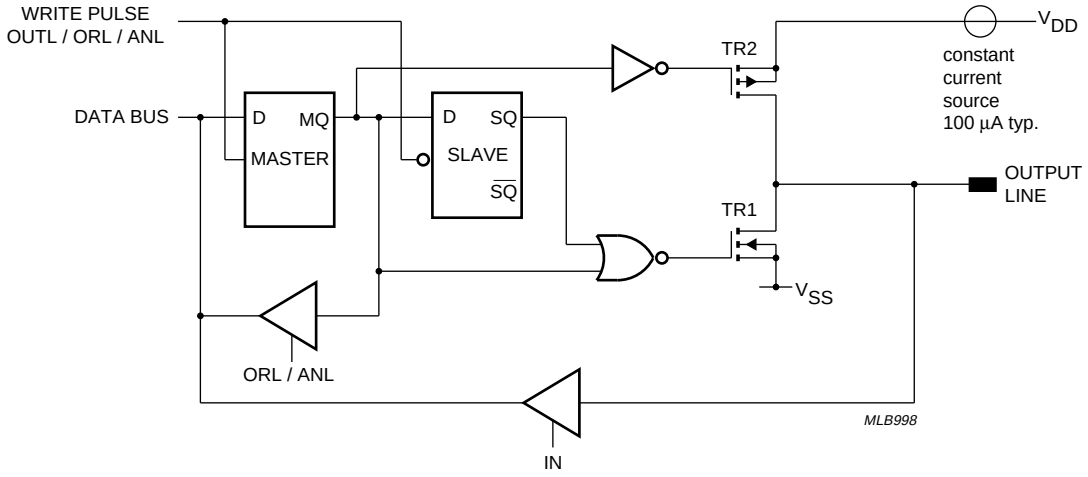


Fig.23 Push-pull output with pull-up transistor (Option 3).

12.1 Mask options

Table 6 lists the port mask options available for the PCE84C486; Table 7 lists the port mask options available for the PCE84C487.

Table 6 Port options - PCE84C486

PORT	PIN	OPTION	
		CONFIGURATION	RESET STATE
P00	8	1, 2 or 3	HIGH or LOW
P01	9	1, 2 or 3	HIGH or LOW
P02	10	1, 2 or 3	HIGH or LOW
P03	11	1, 2 or 3	HIGH or LOW
P04	12	1, 2 or 3	HIGH or LOW
P05	13	1, 2 or 3	HIGH or LOW
P06	14	1, 2 or 3	HIGH or LOW
P07	15	1, 2 or 3	HIGH or LOW
P10	2	1, 2 or 3	HIGH or LOW
P11	3	1, 2 or 3	HIGH or LOW
P12	5	1, 2 or 3	HIGH or LOW
P14	7	1, 2 or 3	HIGH or LOW
DP00	24	1, 2 or 3	HIGH or LOW
DP01	23	1, 2 or 3	HIGH or LOW
DP02	22	1, 2 or 3	HIGH or LOW
DP03	21	1, 2 or 3	HIGH or LOW
DP04	20	1, 2 or 3	HIGH or LOW
DP05	19	1, 2 or 3	HIGH or LOW
DP06	18	1, 2 or 3	HIGH or LOW
DP07	32	1, 2 or 3	HIGH or LOW
DP11	17	1, 2 or 3	HIGH or LOW
DP12	31	1, 2 or 3	HIGH or LOW
DP13	4	1, 2 or 3	HIGH or LOW
DP20	1	2	HIGH

Table 7 Port options - PCE84C487

PORT	PIN	OPTION	
		CONFIGURATION	RESET STATE
P00	10	1, 2 or 3	HIGH or LOW
P01	12	1, 2 or 3	HIGH or LOW
P02	13	1, 2 or 3	HIGH or LOW
P03	15	1, 2 or 3	HIGH or LOW
P04	17	1, 2 or 3	HIGH or LOW
P05	18	1, 2 or 3	HIGH or LOW
P06	19	1, 2 or 3	HIGH or LOW
P07	20	1, 2 or 3	HIGH or LOW
P10	2	1, 2 or 3	HIGH or LOW
P11	3	1, 2 or 3	HIGH or LOW
P12	5	1, 2 or 3	HIGH or LOW
P14	9	1, 2 or 3	HIGH or LOW
DP00	31	1, 2 or 3	HIGH or LOW
DP01	30	1, 2 or 3	HIGH or LOW
DP02	28	1, 2 or 3	HIGH or LOW
DP03	26	1, 2 or 3	HIGH or LOW
DP04	25	1, 2 or 3	HIGH or LOW
DP05	24	1, 2 or 3	HIGH or LOW
DP06	23	1, 2 or 3	HIGH or LOW
DP07	42	1, 2 or 3	HIGH or LOW
DP11	22	1, 2 or 3	HIGH or LOW
DP12	41	1, 2 or 3	HIGH or LOW
DP13	4	1, 2 or 3	HIGH or LOW
DP20	1	2	HIGH
DP24	8	1, 2 or 3	HIGH or LOW
DP25	14	1, 2 or 3	HIGH or LOW
DP26	29	1, 2 or 3	HIGH or LOW
DP27	34	1, 2 or 3	HIGH or LOW

13 DERIVATIVE REGISTERS

The PCE84C486 has 22 Derivative Registers and the PCE84C487 has 26 Derivative Registers. Both devices have one dummy register associated with the Watchdog Timer; this resides at address 45H. The Derivative Port I/O registers are located at addresses 00 to 05H. When DP0TR, DP1TR and DP2TR are read the data is read directly from the pin. However, when DP0R, DP1R and DP2R are read the data is read from the port latch (see Figs 24 to 26 for the port configuration).

As the PCE84C486 has no 8-bit PWM outputs the PWME2 Register (address 44H) is not used and its contents must be set to 00H. Registers PWME2, PWM10 to PWM13 and the 4 MSBs of Registers DP2TR and DP2R are only available in the PCE84C487.

Table 8 Register map (see note 1)

ADDR (HEX)	REG	7	6	5	4	3	2	1	0	R/W
00	DP0TR (terminal)	DP07 (X)	DP06 (X)	DP05 (X)	DP04 (X)	DP03 (X)	DP02 (X)	DP01 (X)	DP00 (X)	R
01	DP1TR (terminal)	– (X)	– (X)	– (X)	– (X)	DP13 (X)	DP12 (X)	DP11 (X)	–	R
02	DP2TR (terminal)	DP27 (X)	DP26 (X)	DP25 (X)	DP24 (X)	– (X)	– (X)	– (X)	DP20 (X)	R
03	DP0R (latch)	DP07 (1)	DP06 (1)	DP05 (1)	DP04 (1)	DP03 (1)	DP02 (1)	DP01 (1)	DP00 (1)	RW
04	DP1R (latch)	– (X)	– (X)	– (X)	– (X)	DP13 (1)	DP12 (1)	DP11 (1)	– (1)	RW
05	DP2R (latch)	DP27 (1)	DP26 (1)	DP25 (1)	DP24 (1)	– (X)	– (X)	– (X)	DP20 (1)	RW
10	PWM0	– (X)	PWM06 (0)	PWM05 (0)	PWM04 (0)	PWM03 (0)	PWM02 (0)	PWM01 (0)	PWM00 (0)	RW
11	PWM1	– (X)	PWM16 (0)	PWM15 (0)	PWM14 (0)	PWM13 (0)	PWM12 (0)	PWM11 (0)	PWM10 (0)	RW
12	PWM2	– (X)	PWM26 (0)	PWM25 (0)	PWM24 (0)	PWM23 (0)	PWM22 (0)	PWM21 (0)	PWM20 (0)	RW
13	PWM3	– (X)	PWM36 (0)	PWM35 (0)	PWM34 (0)	PWM33 (0)	PWM32 (0)	PWM31 (0)	PWM30 (0)	RW
14	PWM4	– (X)	– (X)	PWM45 (0)	PWM44 (0)	PWM43 (0)	PWM42 (0)	PWM41 (0)	PWM40 (0)	RW
15	PWM5	– (X)	– (X)	PWM55 (0)	PWM54 (0)	PWM53 (0)	PWM52 (0)	PWM51 (0)	PWM50 (0)	RW
16	PWM6	– (X)	– (X)	PWM65 (0)	PWM64 (0)	PWM63 (0)	PWM62 (0)	PWM61 (0)	PWM60 (0)	RW
17	PWM7	– (X)	– (X)	PWM75 (0)	PWM74 (0)	PWM73 (0)	PWM72 (0)	PWM71 (0)	PWM70 (0)	RW
18	PWM8L	– (X)	PWM86L (0)	PWM85L (0)	PWM84L (0)	PWM83L (0)	PWM82L (0)	PWM81L (0)	PWM80L (0)	RW
19	PWM8H	– (X)	PWM86H (0)	PWM85H (0)	PWM84H (0)	PWM83H (0)	PWM82H (0)	PWM81H (0)	PWM80H (0)	RW

ADDR (HEX)	REG	7	6	5	4	3	2	1	0	R/W
20	ADCCN	– (X)	ADCS1 (0)	ADCS0 (0)	DAC3 (0)	DAC2 (0)	DAC1 (0)	DAC0 (0)	COMP(2) (0)	RW
21	PWME1	PWM7E (0)	PWM6E (0)	PWM5E (0)	PWM4E (0)	PWM3E (0)	PWM2E (0)	PWM1E (0)	PWM0E (0)	RW
22	CON1	PWM8E (0)	SCLE (0)	SDAE (0)	ADCE2 (0)	ADCE1 (0)	0(3)	– (X)	– (X)	RW
23	CON2	– (X)	– (X)	– (X)	– (X)	P8LVL (0)	P14LVL (0)	P7LVL (0)	P6LVL (0)	RW
24	T3CON	T3B7 (0)	T3B6 (0)	T3B5 (0)	T3B4 (0)	T3B3 (0)	T3B2 (0)	T3B1 (0)	T3B0 (0)	R
40	PWM10	PWM107 (0)	PWM106 (0)	PWM105 (0)	PWM104 (0)	PWM103 (0)	PWM102 (0)	PWM101 (0)	PWM100 (0)	RW
41	PWM11	PWM117 (0)	PWM116 (0)	PWM115 (0)	PWM114 (0)	PWM113 (0)	PWM112 (0)	PWM111(0)	PWM110 (0)	RW
42	PWM12	PWM127 (0)	PWM126 (0)	PWM125 (0)	PWM124 (0)	PWM123 (0)	PWM122 (0)	PWM121 (0)	PWM120 (0)	RW
43	PWM13	PWM137 (0)	PWM136 (0)	PWM135 (0)	PWM134 (0)	PWM133 (0)	PWM132 (0)	PWM131 (0)	PWM130 (0)	RW
44	PWME2	– (X)	– (X)	– (X)	– (X)	PWM13E (0)	PWM12E (0)	PWM11E (0)	PWM10E (0)	RW

Notes

1. Values within parethesis show the bit state after a reset operation. ‘X’ denotes an undefined state.
2. This bit is Read only.
3. This bit must be set to logic 0.

14 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 34)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	+8.0	V
V_I	input voltage on any pin with respect to ground (V_{SS})	–0.3	V_{DD} + 0.3	V
I_{OH}	maximum source current for all port lines	–	–10.0	mA
I_{OL}	maximum sink current for all port lines	–	30.0	mA
P_{tot}	total power dissipation	–	1	W
T_{amb}	operating ambient temperature	–25	+85	°C
T_{stg}	storage temperature	–55	+125	°C

15 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = −25 to +85 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		4.5	5.0	5.5	V
I_{DD}	operating supply current	f_{xtal} = 10 MHz; V_{DD} = 5 V	–	5	10	mA
		f_{xtal} = 6 MHz; V_{DD} = 5 V	–	3.5	7	mA
		Stop; f_{xtal} = 10 MHz	–	3	6	mA
		Stop; f_{xtal} = 6 MHz	–	1.5	4	mA
I_{LU}	latch-up current for all pins		50	–	–	mA
V_{POR}	Power-on-reset voltage level		0.7	1.3	1.9	V
Ports P0; P1; DP0; DP1 and DP2 inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	–	–	±10	µA
Port P0 outputs						
V_{OL}	LOW level output voltage	V_{DD} = 5 V; I_{OL} = 10 mA	–	–	1.2	V
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA
DP00/PWM0 to DP07/PWM7; DP24/PWM10 to DP27/PWM13 as derivative ports						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA
DP00/PWM0 to DP07/PWM7; DP24/PWM10 to DP27/PWM13 as PWM outputs						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	0.7	1.5	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–0.7	–1.5	–	mA
P10 to P12 and P14 outputs						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA
DP20/SDA and DP21/SCL outputs						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	3.0	–	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA

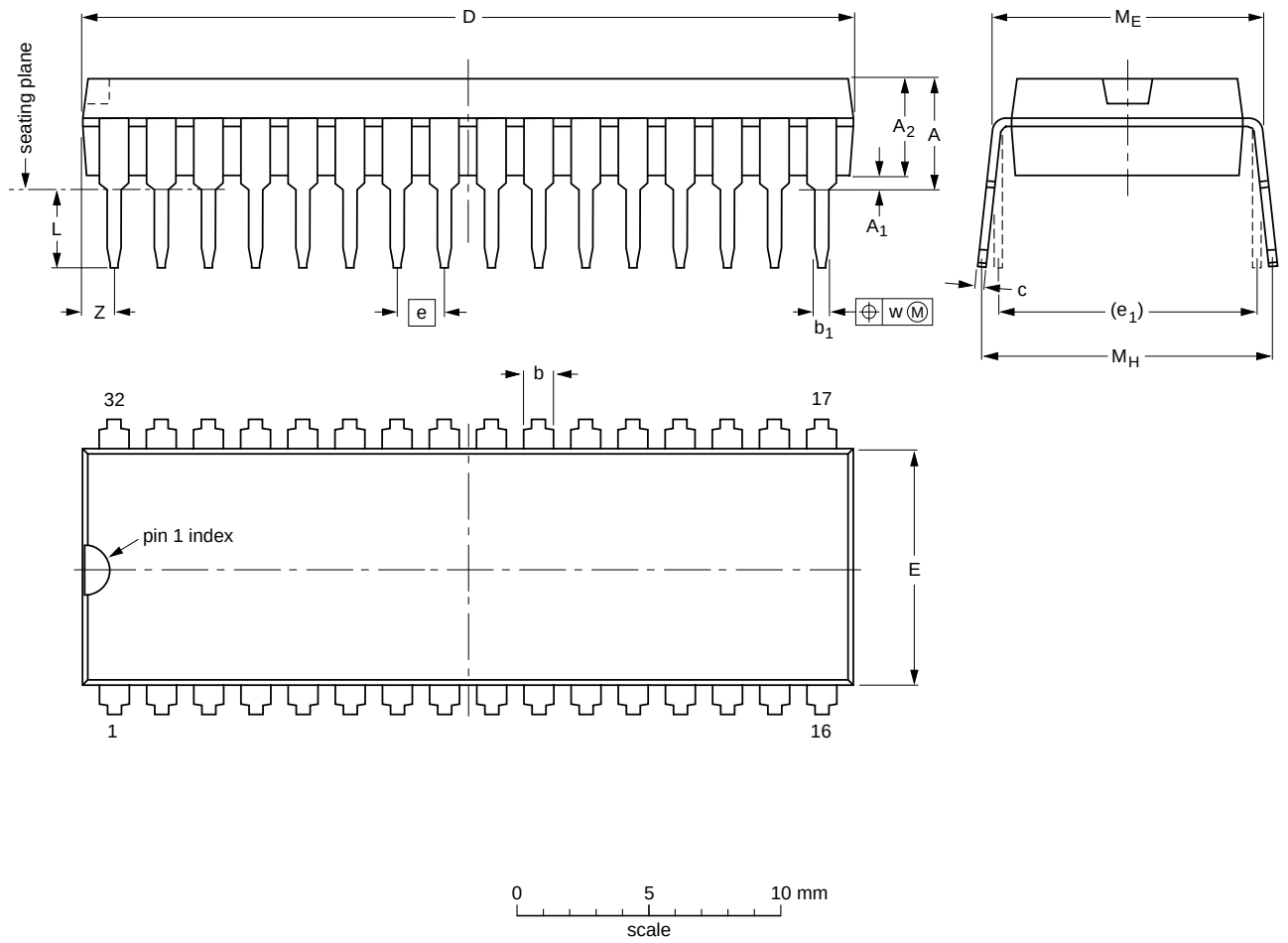
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DP13/PWM8 as PWM8 output						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	1.4	3.0	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–1.4	–3.0	–	mA
DP11/ADC1 or DP12/ADC2 as derivative output ports						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_{OL} = 0.4 V	5.0	12.0	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA
TEST/EMU; $\overline{\text{RESET}}$; INTN/T0; T1 and T3						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	–1.0	–	+1.0	µA

16 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	Crystal oscillator frequency	V_{DD} = 5 V; T_{amb} = –25 to +85 °C				
	Option 1: g_m = 0.4 mS		1	–	6	MHz
	Option 2: g_m = 1.2 mS		4	–	10	MHz
f_{PXE}	PXE resonator frequency	V_{DD} = 5 V; T_{amb} = –25 to +85 °C				
	Option 2: g_m = 1.2 mS		1	–	5	MHz
C_{xtal1}	external capacitance at XTAL1 (IN) pin (PXE resonator)	V_{DD} = 5 V; T_{amb} = –25 to +85 °C	–	30	100	pF
C_{xtal2}	external capacitance at XTAL2 (OUT) pin (PXE resonator)	V_{DD} = 5 V; T_{amb} = –25 to +85 °C	–	30	100	pF
t_{T3}	minimum pulse width period at T3 input	rising or falling edge of T3 pulse < 30 ns	0.4	–	–	µs
Analog-to-Digital (software) Converter						
V_{AI}	DP11/ADC1 or DP12/ADC2 comparator analog input voltage		V_{SS}	–	V_{DD}	V
V_{AE}	conversion error range		–	–	±½	LSB
T_{AFC}	conversion time (from any change in ADC input i.e. channel select, voltage level or enable/disable)		–	–	7	µs

17 PACKAGE OUTLINES

SDIP32: plastic shrink dual in-line package; 32 leads (400 mil) **SOT232-1**



DIMENSIONS (mm are the original dimensions)

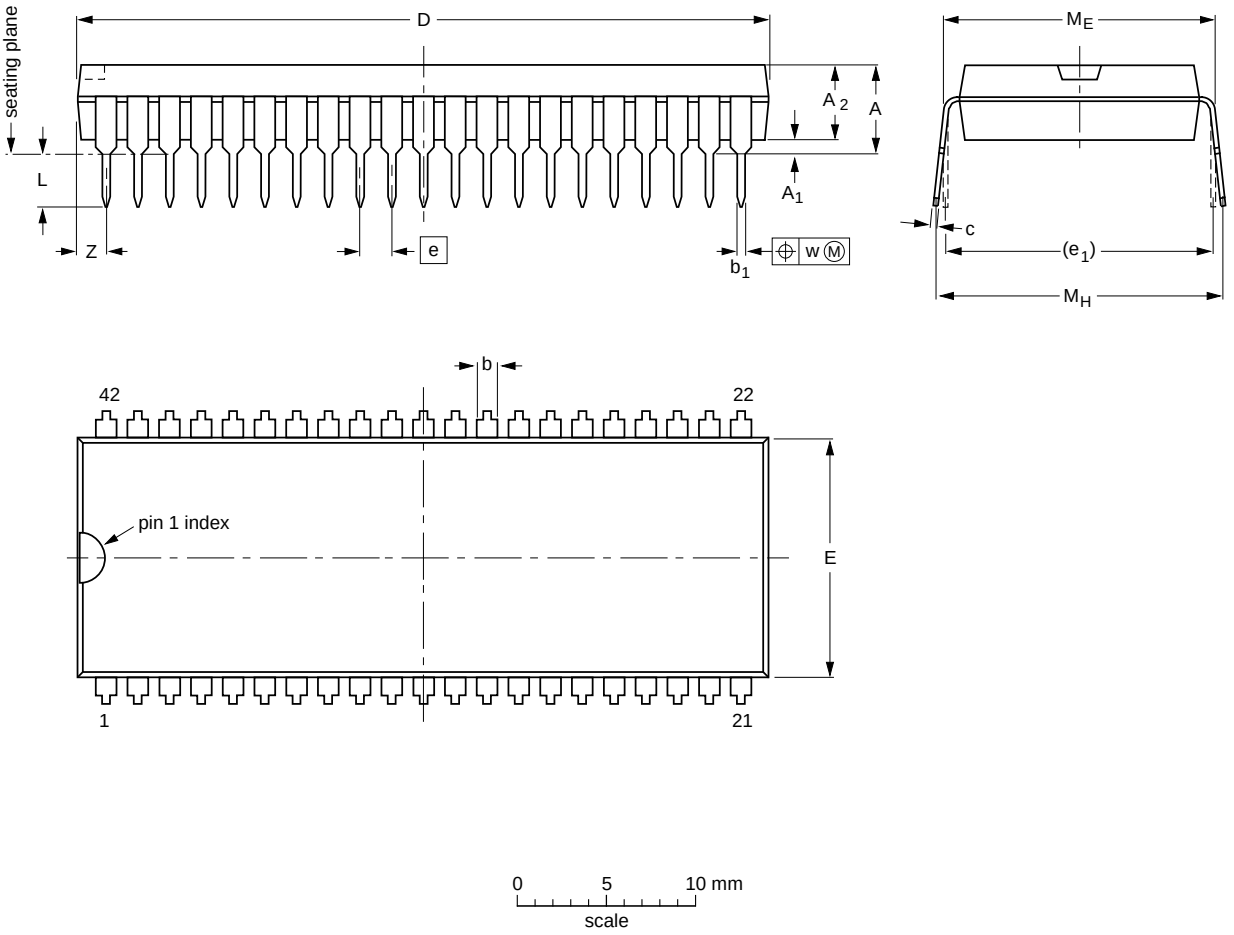
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	29.4 28.5	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT232-1						~~92-11-17~~ 95-02-04

SDIP42: plastic shrink dual in-line package; 42 leads (600 mil) **SOT270-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.08	0.51	4.0	1.3 0.8	0.53 0.40	0.32 0.23	38.9 38.4	14.0 13.7	1.778	15.24	3.2 2.9	15.80 15.24	17.15 15.90	0.18	1.73

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT270-1						~~90-02-13~~ 95-02-04

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 SDIP

18.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

18.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

21 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

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