DATA SHEET

PCA8514
Stand-alone OSD

Product specification
File under Integrated Circuits, IC14

1995 Nov 27

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Display RAM: 256 × 12 bits
- Display character fonts: 128 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 16 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$ or $\frac{1}{128}$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends upon the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address auto-post-increment when writing data
- Fast I^2C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camcorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: –20 to +70 °C
- Package: SDIP24 or SO24.

2 GENERAL DESCRIPTION

The PCA8514 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I^2C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camcorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8514P	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA8514T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

4 BLOCK DIAGRAM

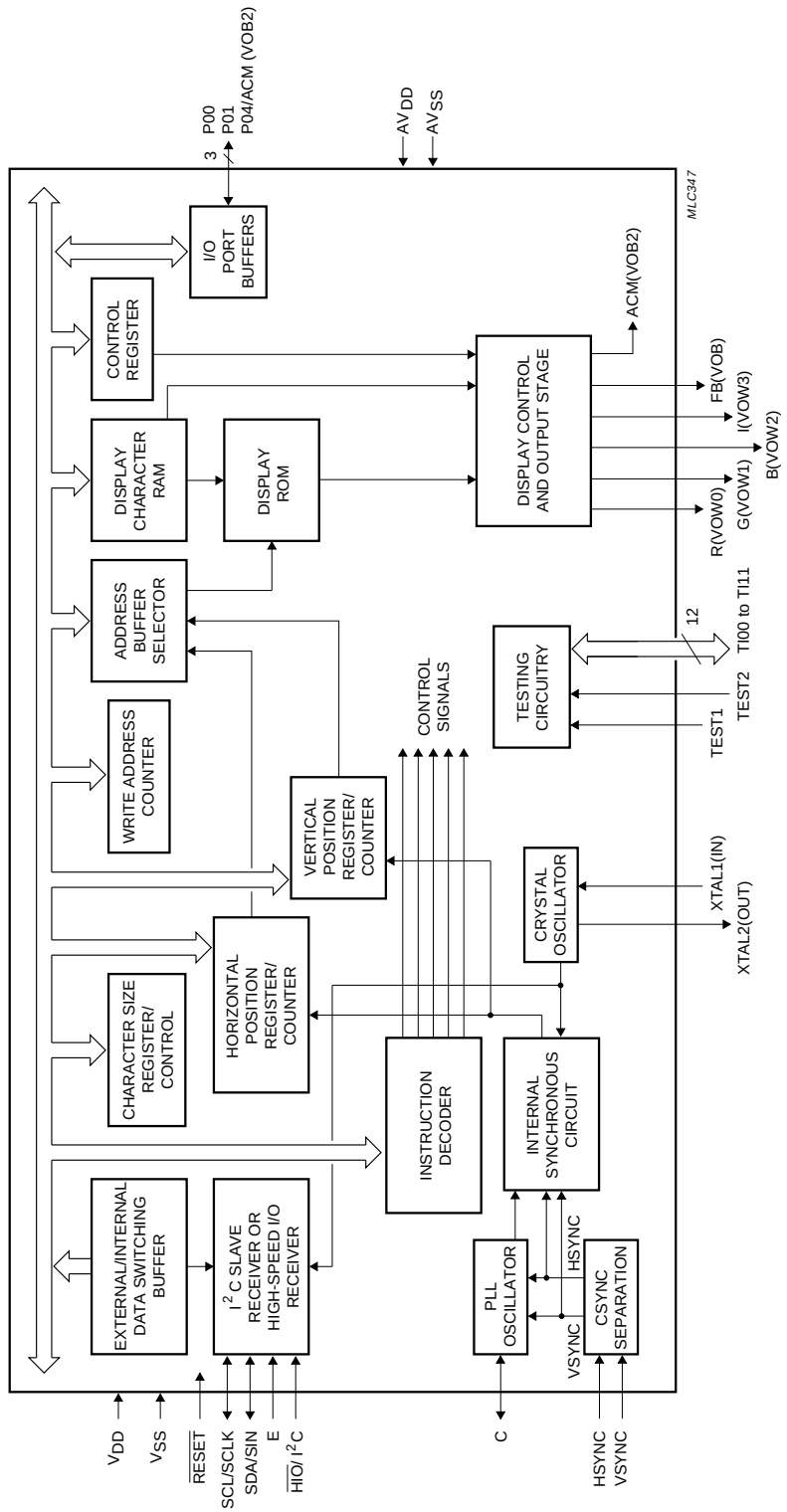


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

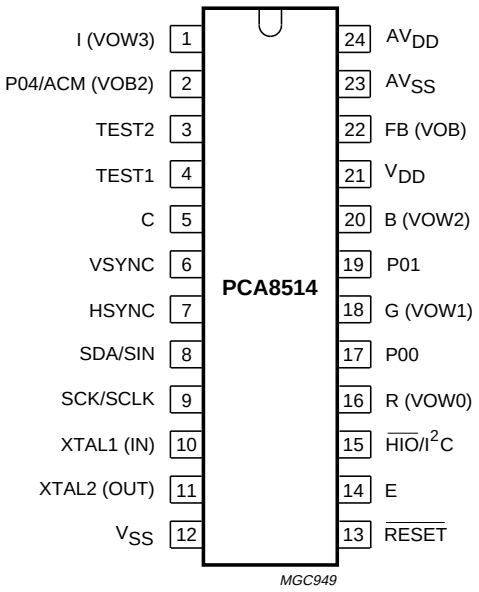


Fig.2 Pin configuration for SDIP24 and SO24.

5.2 Pin description

Table 1 SDIP24 and SO24 packages

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control.
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2).
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to $V_{SS.}$
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator.
VSYNC	6	I	Vertical synchronization input, active polarity programmable.
HSYNC	7	I	Horizontal synchronization input, active polarity programmable.
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface.
SCL/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface.
XTAL1 (IN)	10	I	System clock input.
XTAL2 (OUT)	11	O	System clock output.
V_{SS}	12	I	Ground, digital.
$\overline{\text{RESET}}$	13	I	Master reset input (active LOW).
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{\text{HIO}}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red.
P00	17	I/O	General purpose I/O Port 00.
G (VOW1)	18	O	Character output signal: VOW1 for Green.
P01	19	I/O	General purpose I/O Port 01.
B (VOW2)	20	O	Character output signal: VOW2 for Blue.
V_{DD}	21	I	Power supply, digital.
FB (VOB)	22	O	Fast Blanking output (VOB).
AV_{SS}	23	I	Ground, analog.
AV_{DD}	24	I	Power supply, analog.

6 SERIAL I/O

The PCA8514 has two means by which it can communicate with a microcontroller: a fast I²C-bus serial interface and a High-speed serial interface. Selection of either interface is achieved via pin 15, $\overline{HIO}$/I²C. When $\overline{HIO}$/I²C is LOW, the HIO serial interface is selected. When $\overline{HIO}$/I²C is HIGH, the I²C-bus serial interface is selected.

The PCA8514 is programmed by a series of commands sent via one of these interfaces. There are 16 commands; each command selecting different functions of the PCA8514. The 16 commands are described in detail in Chapter 9.

6.1 I²C-bus serial interface

The I²C-bus serial interface is selected by driving pin 15 ($\overline{HIO}$/I²C) HIGH. Data transmission conforms to the fast I²C-bus protocol; the maximum transmission rate being 400 kHz. The PCA8514 operates in the slave receiver mode and therefore in normal operation is 'write only' from the master device.

The format of the data streams sent via the I²C-bus interface is shown in Fig.3. The first data byte is the slave address 1011 101X_b. The last bit of the slave address is always a logic 0, except in the Test mode when it could be a logic 1. Subsequent data bytes contain the commands for control of the device. Upon the successful reception of a complete data byte by the shift register, an Acknowledge bit is sent. A STOP condition terminates the data transfer operation.

The I²C-bus interface is reset to its initial state (waiting for a slave address call) by the following conditions:

- After a master reset
- After a bus error has been detected on the I²C-bus interface.

Under both these conditions the data held in the shift register is abandoned.

6.1.1 MAXIMUM SPEED OF THE I²C-BUS

The maximum I²C-bus transmission rate that the PCA8514 can receive is 400 kHz. However, if the data byte being transmitted is for display RAM then internal synchronization of the write operation from the shift register to the display RAM location is necessary. This will reduce the maximum transmission speed.

The synchronization process is carried out by on-chip hardware and takes place during the HSYNC retrace period when VSYNC is inactive. The I²C-bus clock is pulled LOW if a complete display RAM data byte is received before HSYNC becomes active. The I²C-bus clock will be released when HSYNC becomes active and then the contents of the shift register will be written into the display RAM location.

6.2 High-speed serial interface (HIO)

The High-speed serial interface is selected when pin 15 ($\overline{HIO}$/I²C) is pulled LOW. The High-speed serial interface has a 3-wire communication protocol; the maximum transmission rate being 1 MHz. The interface protocol is illustrated in Fig.4 and described below.

1. Pin 14 (E) the chip enable pin is driven HIGH. This LOW-to-HIGH transition clears the shift register and resets the serial input circuit.
2. On the first HIGH-to-LOW transition of SCLK after the interface has been enabled, the first data bit (D0) must be present at the SIN pin.
3. On the following LOW-to-HIGH transition of SCLK, the first data bit (D0) will be latched into the shift register.
4. On the next HIGH-to-LOW transition of SCLK the second data bit (D1) must be present at the SIN pin. Data bit (D1) will be latched into the shift register on the following LOW-to-HIGH transition of SCLK.
5. The operation specified in step 4 above is repeated another 6 times, thus loading the shift register with a complete data byte. This data byte is then transferred to the command interpreter which takes the appropriate action.
6. Providing the chip enable signal remains HIGH, a 2nd data byte can be transferred. The 1st data bit of the next data transfer takes place on the falling edge of the SCLK signal.

The following points should be noted:

- If the chip enable signal is pulled LOW at any time the shift operation in progress is stopped and the HIO slave receiver is disabled
- The rising edge of the chip enable signal resets the HIO slave receiver.

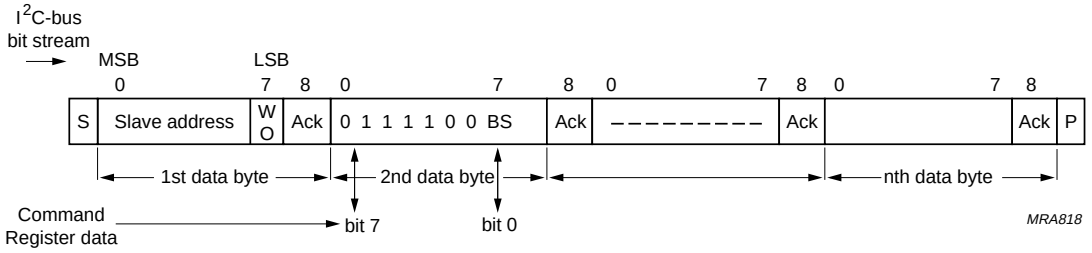
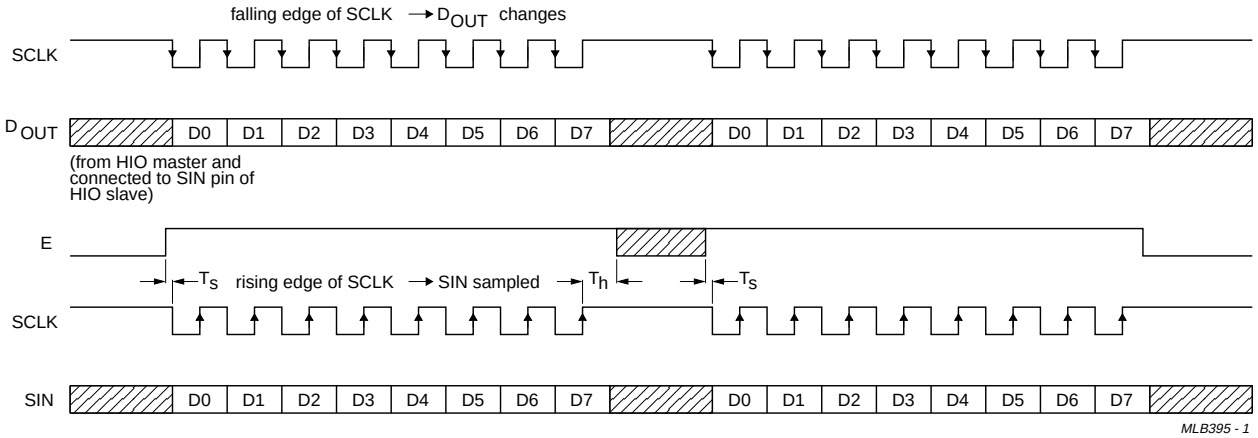


Fig.3 I^2C-bus write timing diagram - data stream.



(1) $T_s \geq 1\ \mu s$; $T_h \geq 1\ \mu s$.

Fig.4 High-speed I/O format.

7 CHARACTER FONTS

128 character fonts may be held in ROM; 125 customer selected fonts and three reserved character font codes. Customer selected fonts are mask programmable. Each character font is stored in a 12×19 dot matrix, as shown in Fig.5. Elements in Rows 1 to 18 can be selected as visible dots on the screen; Row 0 is used only for the combination of two characters in a vertical direction, when the North-West shadowing mode is selected (see Sections 9.9 and 10.2). Extremely high resolution can be achieved by having no spacing between characters on the same line and by programming the inter-line spacing to zero. The 12×18 dot matrix is suitable for the display of semigraphic patterns, Kanji, Hiragana, Katagana or even Chinese characters.

7.1 Character font address map

Figure 6 shows the character font address map in ROM and RAM. Addresses 7FH and 7EH hold the reserved codes for space and carriage return functions respectively; address 7DH is reserved for testing purposes and addresses (00H to 7CH) contain the character font codes.

7.2 Character font ROM

ROM is divided into two parts: ROM1 and ROM2. The organization of the bit patterns stored in ROM1 and ROM2 is shown in Fig.7.

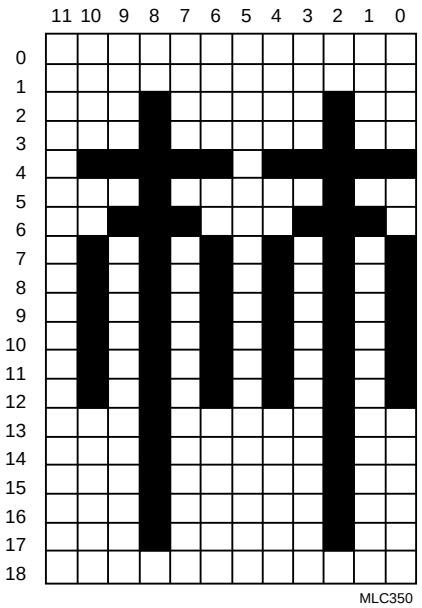


Fig.5 Character dot matrix organization.

The file format to submit to Philips for customized character sets is also shown in Fig.7. The following points should be noted:

1. Row 0 of each font is reserved for vertical combination of two fonts.
2. When two font cells are combined in a vertical direction Row 0 of the lower font must contain the same bit pattern as held in Row 18 of the character above it.
3. Binary 1 denotes visual dots; binary 0 denotes a blank space.
4. ROM1 and ROM2 data files are in INTEL hex format on a byte basis. Each byte is structured High nibble followed by Low nibble.
5. The remaining unused 16 bytes (one character font) in ROM1/ROM2 must be filled with FFH.
6. CS denotes Checksum.

A software package (OSDGEM) that assists in the design of character fonts on-screen and that also automatically generates the bit pattern HEX files, is available on request. The package is run under the MS-DOS environment for IBM compatible PCs.

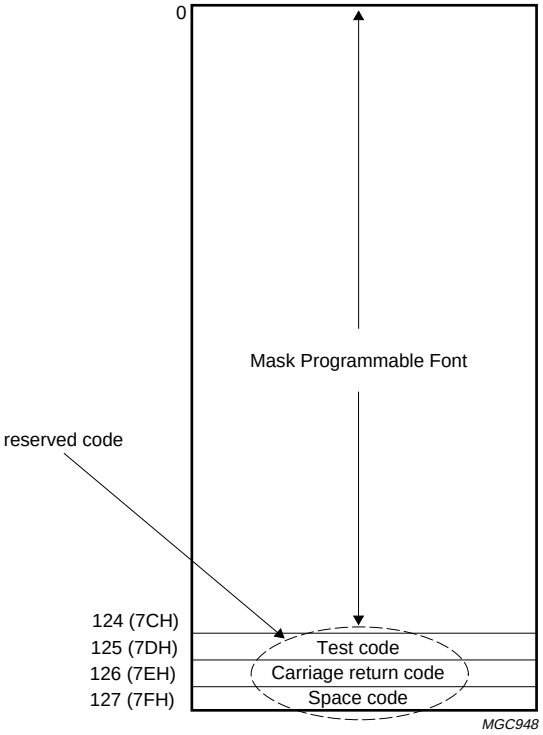


Fig.6 ROM address map.

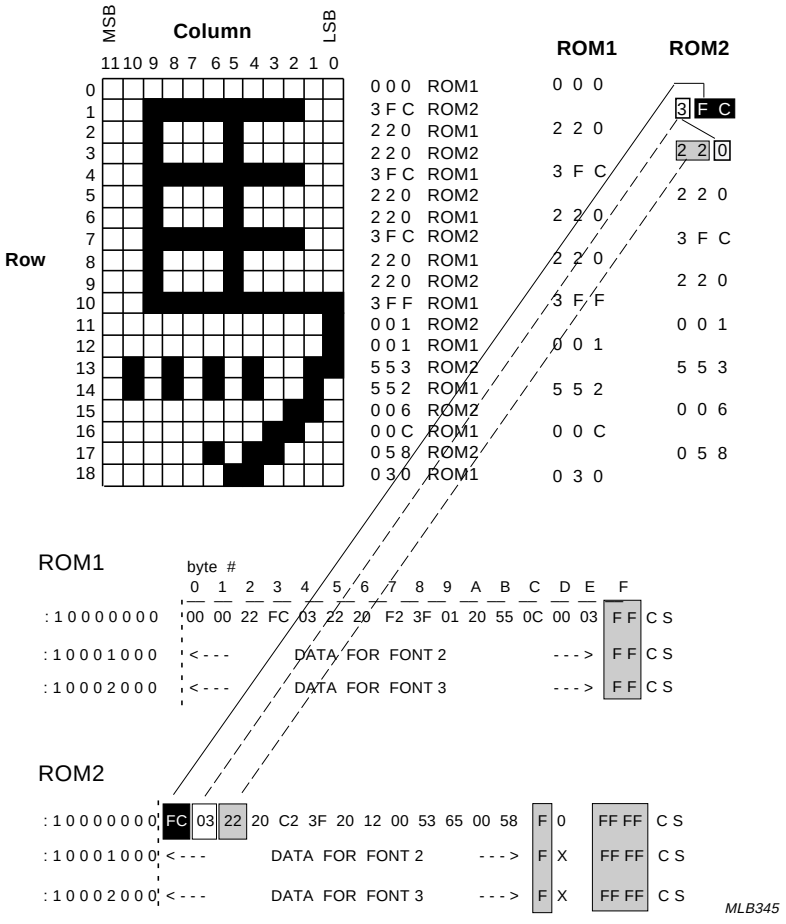


Fig.7 Character font pattern stored in ROM1 and ROM2.

8 DISPLAY RAM ORGANIZATION

The display RAM is organized as 256 × 12 bits. The general format of each RAM location is as follows. Bits <11-5> hold character data and allow a choice from 125 customer designed character fonts to be selected or one of three reserved codes. Bits <4-0> contain the attributes of the character font, for example colour, character size etc.

8.1 Description of display RAM codes

There are four data formats for display RAM code:

1. Character Font Code
2. Test Code
3. Carriage Return Code
4. Space Code.

The above data formats allow great flexibility in the creation of On Screen Displays; see Fig.8.

8.1.1 CHARACTER FONT CODE

If bits <11-5> are in the range (00H to 7CH), then this is a Character Font Code. 1 of 125 customer designed character fonts can be selected. Bits <4-1> determine the colour of the character, a choice of 16 colours being available. Bit <0> determines whether the character blinks or not. The format of the Character Font Code is shown in Table 2.

8.1.2 TEST CODE

If bits <11-5> hold 7DH, then this is a special code reserved for testing purposes only.

8.1.3 CARRIAGE RETURN CODE

If bits <11-5> hold 7EH, then this is the Carriage Return Code. A transparent pattern will be displayed on the screen and the next character will be displayed at the beginning of the next line. Bits <4-3> select the size of the characters to be displayed on the next line. Bits <2-1> determine the spacing between lines of displayed characters. Bit <0> is the End of Display bit and indicates the end of display of the current screen before exhaustion of display RAM (i.e. before the 256th RAM location). The format of the Carriage Return Code is shown in Table 3.

8.1.4 SPACE CODE

If bits <11-5> hold 7FH, then this is the Space Code. A transparent pattern, equal to one character width, will be displayed on the screen. A mask programmable option is available that allows the space character to be transparent or to have a programmable background colour; see Section 13.1. Bits <4-1> determine the background colour of the characters that follow the Space Code in both the Box shadowing and North-West shadowing modes. Bit <0> is the Active Character Monitor (ACM) enable/disable bit. The ACM signal is specifically for use in camrecorder applications where part of the display is to be recorded on tape and displayed on the screen, whilst the remaining part is for display only. Figure 9 shows a typical ACM application. During the back-tracing period R, G, B, I, FB and ACM are inactive. The format of the Space Code is shown in Table 4.

Table 2 Format of Character Font Code

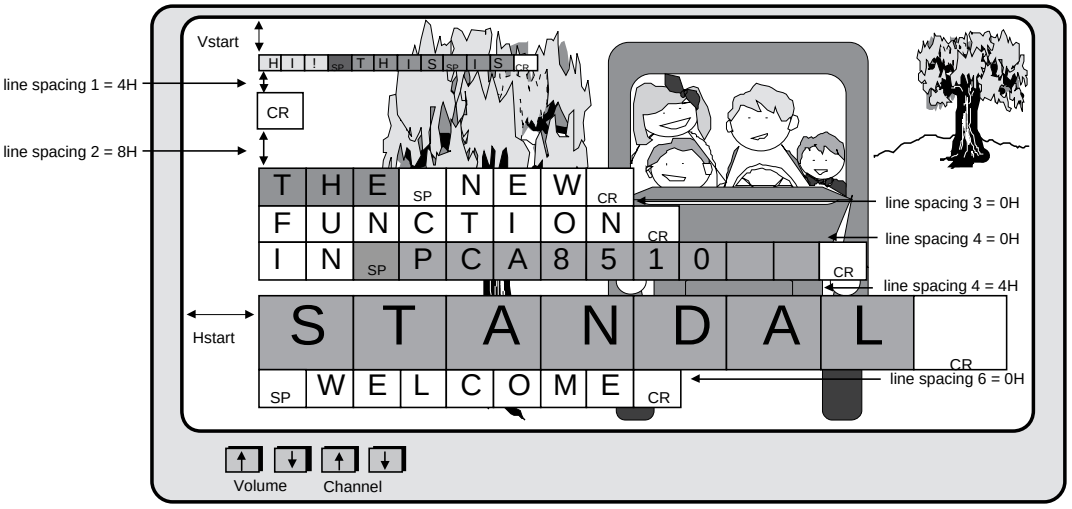
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Character Font Code (00H - 7CH)							Foreground colour				Blink

Table 3 Format of Carriage Return Code

11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T1
Carriage Return Code (7EH)							Character size		Line Spacing		End

Table 4 Format of Space Code

11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Space Code (7FH)							Background colour				ACM

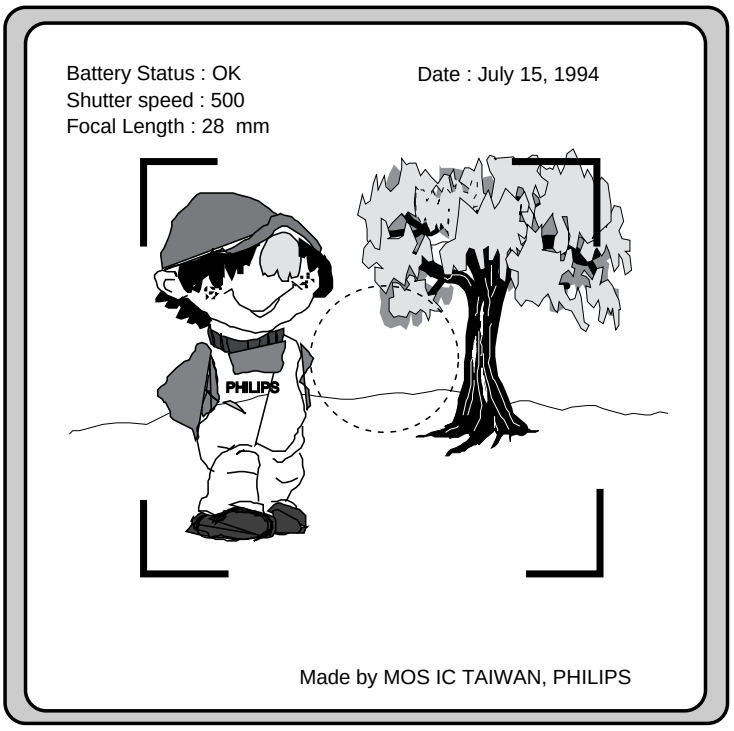


MRA832

Four different background colours (in box shadowing mode):

- BLACK
- RED
- GREEN
- BLUE

Fig.8 Example of On Screen Display.



In this example, all the characters are displayed on the viewfinder. As only the data 'Date : July 15, 1994' is to be recorded onto the tape, only these characters' ACM attribute bit is set to a logic 1.

Fig.9 Example of ACM signal for use in camrecorder applications.

8.2 Loading character data into display RAM

Three registers are used to address and load data into the display RAM. These registers are described below.

8.2.1 DCR ADDRESS REGISTER (DCRAR)

Table 5 DCR Address Register

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

This register holds the address of the location in display RAM into which data is to be written. Command 3 loads the High nibble of the address into this register; Command 4 loads the Low nibble of the address.

8.2.2 DCR ATTRIBUTE REGISTER (DCRTR)

Table 6 DCR Attribute Register

7	6	5	4	3	2	1	0
–	–	–	T4	T3	T2	T1	T0

The Attribute Register is loaded with character font attribute data using Command 2. The data will be loaded into bits <4-0> of the location in RAM addressed by the contents of DCRAR. Bits 7 to 5 are not used and are reserved.

8.2.3 DCR CHARACTER REGISTER (DCRCR)

Table 7 DCR Character Register

7	6	5	4	3	2	1	0
–	C6	C5	C4	C3	C2	C1	C0

This register holds the character font data loaded by Command 5. The data will be loaded into bits <12-5> of the location in RAM addressed by the contents of DCRAR.

8.3 Writing character data to display RAM

The procedure for writing character data to the display RAM is as follows:

1. Select the start address in display RAM. The start address can take any value between 0 and 255. Command 3 is used to load the High nibble of the start address. Command 4 is used to load the Low nibble of the start address. The start address is stored in DCRAR.
2. Load the character attributes into DCRTR using Command 2. The actual attribute selected is dependent upon whether the Character Font Code, Carriage Return Code or Space Code has been selected by Command 5 (see Section 8.1).

   If the attributes of a series of displayed characters are the same, the contents of this register need not be updated.
3. Load the Character Font data into DCTCR using Command 5. This command signals that a complete command byte is available and the data held in registers DCRTR and DCRCR is loaded into the RAM location pointed to by the address stored in DCRAR. The address held in DCRAR is then incremented by ‘1’ pointing to the next RAM location in anticipation of the next operation.

A description of all the Commands is given in Chapter 9.

9 COMMANDS

The PCA8514 is programmed by a series of commands sent by a microcontroller via the I^2C-bus interface or the High-speed serial interface. 16 commands (Commands 0 to G) are available for selecting the various functions of the PCA8514. A command overview is shown in Table 8; full descriptions of each command are given in Sections 9.1 to 9.15.

Table 8 Command overview (note 1)

COMMAND		BS1	BS0	7	6	5	4	3	2	1	0
0	Command Bank selection	X	X	0	1	1	1	1	0	BS1	BS0
1	Not used in the PCA8514	0	0	1	–	–	–	–	–	–	–
2	Character attributes	X	0	0	0	0	T4	T3	T2	T1	T0
3	Display Character Address High	0	0	0	0	1	0	A7	A6	A5	A4
4	Display Character Address Low	0	0	0	0	1	1	A3	A2	A1	A0
5	Character font selection - Bank 2	1	0	1	C6	C5	C4	C3	C2	C1	C0
6	OSD PLL oscillator divisor	0	1	0	0	D5	D4	D3	D2	D1	D0
7	Scan mode, polarity of FB, ACM, R, G, B and I; OSD enable/disable	0	1	0	1	0	0	M1	M0	Bp	EN
8	Polarity of HSYNC and VSYNC, Display mode	0	1	0	1	0	1	Hp	Vp	S1	S0
9	Blinking frequency, blinking frequency active ratio	0	1	0	1	1	0	BF1	BF0	BR1	BR0
A	I/O port selection	0	1	0	1	1	1	0	A/P	0	0
B	Vertical start position High	0	1	1	0	0	1	V5	V4	V3	V2
C	Vertical start position Low/ Horizontal start position High	0	1	1	0	1	0	V1	V0	H5	H4
D	Horizontal start position Low	0	1	1	0	1	1	H3	H2	H1	H0
E	Write to ports P00, P01 and P04	0	1	1	1	X	P04	X	X	P01	P00
F	Background colour in Frame shadowing mode	0	0	0	1	0	0	R	G	B	I
G	Enable/disable OSD horizontal stabilization circuit (Regen H), selection of Half-tone background mode and character size of first line	0	0	0	1	0	1	HM3	HT2	FS1	FS0

Note

1. ‘X’ denotes don’t care state.

9.1 Command 0

Table 9 Command 0 format

7	6	5	4	3	2	1	0
0	1	1	1	1	0	BS1	BS0

Command 0 is used to select the Command Bank. Bits BS1 and BS0 are the two flags that indicate the current Command Bank being executed. During a master reset these two bits are cleared (BS1 = 0, BS0 = 0). Each command has its own associated Command Bank, this is shown in Table 8.

9.2 Command 1

Command 1 is not used in the PCA8514.

9.3 Command 2

Table 10 Command 2 format

BS1	BS0	7	6	5	4	3	2	1	0
X	0	0	0	0	T4	T3	T2	T1	T0

This command writes character attribute data into the DCR Attribute Register. The actual character attribute is dependent upon the code selected by Command 5.

Sections 9.3.1 to 9.3.2 define the character attribute data loaded by Command 2 when Command 5 selects either a Character Font Code, a Carriage Return Code or a Space code. See Tables 2, 3 and 4 for the three code formats.

9.3.1 Character Font Code attributes

Command 2 when used in conjunction with a Character Font Code (00H to 7CH) will select 1 of 16 foreground colours and enables/disables the Blinking function.

Table 11 Selection of Foreground colour

T4	T3	T2	T1
R	G	B	I
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Table 12 Selection of Blinking function

T0	BLINKING
0	OFF
1	ON

9.3.2 Carriage Return Code attributes

Command 2 when used in conjunction with the Carriage Return Code (7EH) determines the size of characters to be displayed on the next line, sets the spacing between lines of characters and enables/disables the display.

The character size is also a function of the TV scanning standard being used and f_{OSD}; this is explained in Chapter 12.

Table 13 Selection of character size

T4	T3	CHARACTER DOT SIZE
0	0	1H/1V (the default size)
0	1	2H/2V
1	0	3H/3V
1	1	4H/4V

Table 14 Selection of line spacing

T2	T1	LINE SPACING (BETWEEN TWO ROWS)
0	0	0H line
0	1	4H line
1	0	8H line
1	1	12H line

Table 15 End of display control

T0	DISPLAY CONTROL
0	Continue to display next character. This is also the default setting.
1	End of display.

9.3.3 Space Code attributes

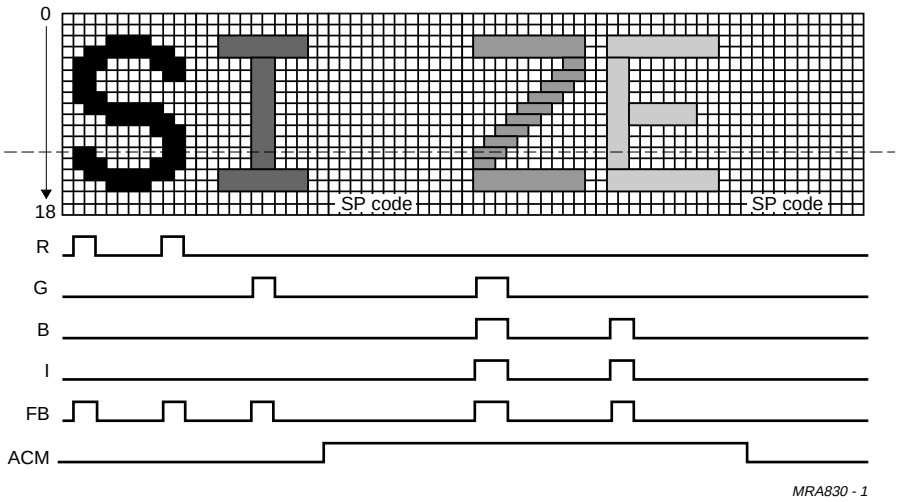
Command 2 when used in conjunction with the Space Code (7FH) selects the background colour of characters in Box shadowing or North-West shadowing modes and also controls the Active Character Monitor pin. The ACM pin will remain active until a Space Code is received that resets the ACM bit to logic 0. The ACM timing diagram is shown in Fig.10.

Table 16 Selection of Background colour

T4	T3	T2	T1
R	G	B	I
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Table 17 ACM control

T0	ACM PIN
0	The ACM pin is inactive; this is also the default setting.
1	The ACM function is active for all characters displayed following this Space Code.



'S' : Red
'I' : Green
'Z' : Green + Blue + Intensity
'E' : Blue + Intensity

1st SP code : ACM = on
2nd SP code: ACM = off

Fig.10 R, G, B, I - ACM timing.

9.4 Command 3

Table 18 Command 3 format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	A7	A6	A5	A4

Command 3 loads the DCR Address Register with the 4 MSBs of the RAM address to which data will be written.

9.5 Command 4

Table 19 Command 4 format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	A3	A2	A1	A0

Command 4 loads the DCR Address Register with the 4 LSBs of the RAM address to which data will be written.

9.6 Command 5

Table 20 Command 5 format

BS1	BS0	7	6	5	4	3	2	1	0
1	0	1	C6	C5	C4	C3	C2	C1	C0

Command 5 is used to load character data into the DCR Character Register. The data will specify either a Character Font Code, the Test Code, the Carriage Return Code or the Space Code. These codes are explained in detail in Section 8.1.

9.7 Command 6

Table 21 Command 6 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	0	D5	D4	D3	D2	D1	D0

Command 6 loads the programmable 6-bit counter of the OSD clock oscillator. The output frequency (f_{OSD}) is a function of the decimal value of the 6-bits loaded in by Command 6; see Chapter 11.

9.8 Command 7

Table 22 Command 7 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	0	0	M1	M0	Bp	EN

This command loads Control Register 1 with data that selects the scanning mode, the output polarity of signals FB, ACM, R, G, B and I, and also enables/disables the OSD clock.

With reference to the scanning modes: 1V/2V is the conventional NTSC or PAL scanning mode; 1V/2H is the Line Progress Scan used for the IDTV in NTSC and 2V/2H is for the PAL system and is known as 50 to 100 Hz scan conversion.

Table 23 Selection of Scanning Mode

M1	M0	SCAN MODE
0	0	1V/1H; NTSC 525LPF/60 Hz or PAL 625LPF/50 Hz; see Fig.11. This is the default setting.
0	1	reserved
1	0	1V/2H; NTSC 1050LPF/60 Hz; see Fig.11.
1	1	2V/2H; PAL 1250LPF/100 Hz; see Fig.12.

Table 24 Selection of output polarity (see Fig.13)

Bp	OUTPUT POLARITY (FB, ACM, R, G, B, I)
0	active LOW
1	active HIGH (the default setting)

Table 25 OSD clock control

EN	OSD CLOCK
0	disabled (the default setting)
1	enabled

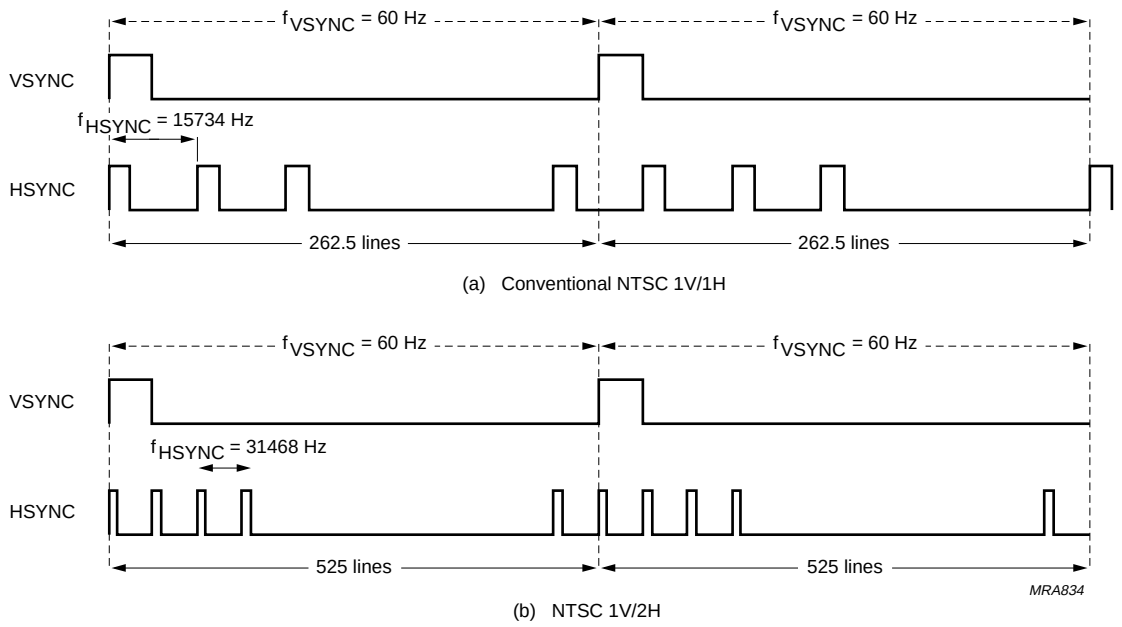


Fig.11 NTSC scan formats.

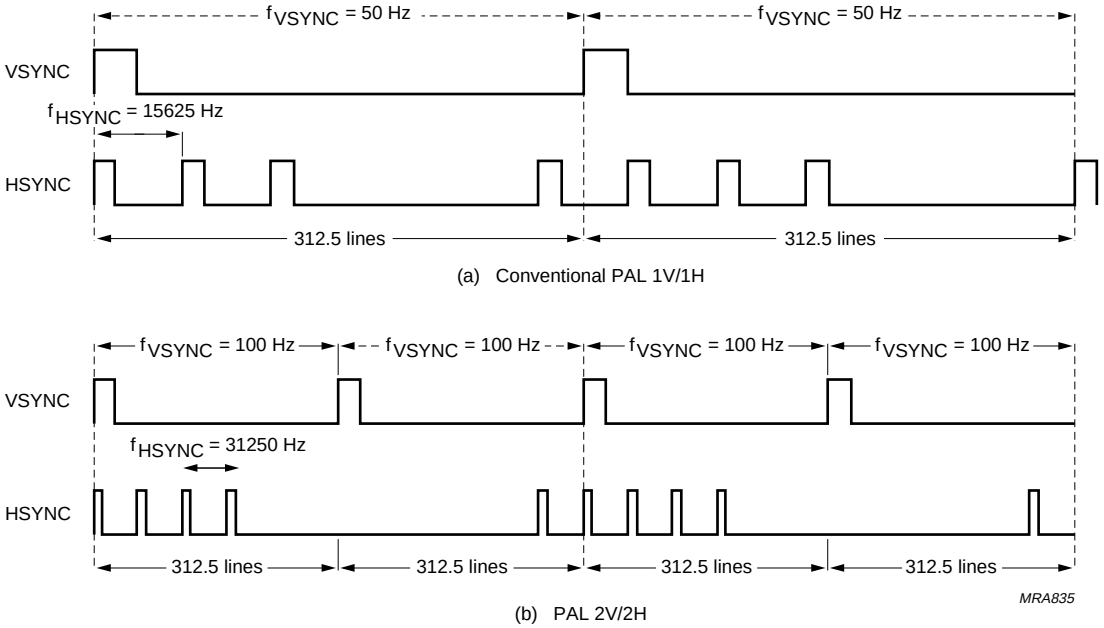


Fig.12 PAL scan formats.

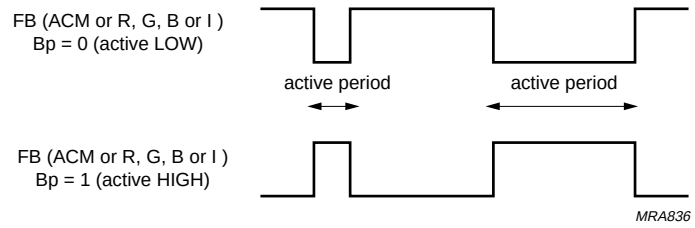


Fig.13 Active levels of FB, R, G, B, and I signals.

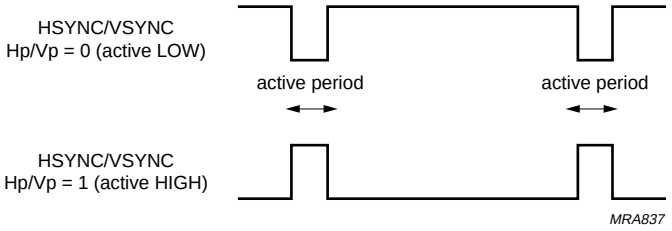


Fig.14 Active levels of HSYNC and VSYNC signals.

9.9 Command 8

Table 26 Command 8 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	0	1	Hp	Vp	S1	S0

Command 8 loads Control Register 2 with data that selects the input polarity of HSYNC and VSYNC (see Fig.14) and also selects the Display modes.

Table 27 Selection of input polarity of HSYNC/VSYNC

Hp/Vp	INPUT POLARITY
0	active LOW (the default setting)
1	active HIGH

Table 28 Selection of Display Mode

S1	S0	DISPLAY MODE
0	0	Mode 0: this is the No background mode. The OSD characters are superimposed on the TV video signals (see Fig.15).
0	1	Mode 1: this is the North-West shadowing mode; available only with character sizes 2V/2H or 4V/4H. The shadows are generated as if a light source was placed North-West of the character (see Figs 16 to 18). The shadows generated lie within 18 rows in a vertical direction but can be extended by one bit to the next characters first column, in a horizontal direction (see Figs 19 and 20).
1	0	Mode 2: this is the Box shadowing mode. A background dot matrix of 12×18 bits surrounds the character font; see Figs 21 and 22.
1	1	Mode 3: this is the Frame shadowing (raster blanking) mode. A background colour fills the whole screen when no bit patterns are being displayed (see Fig.23). 1 of 16 background colours can be selected using Command F; the default background colour is Blue.

9.10 Command 9

Table 29 Command 9 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	1	0	BF1	BF0	BR1	BR0

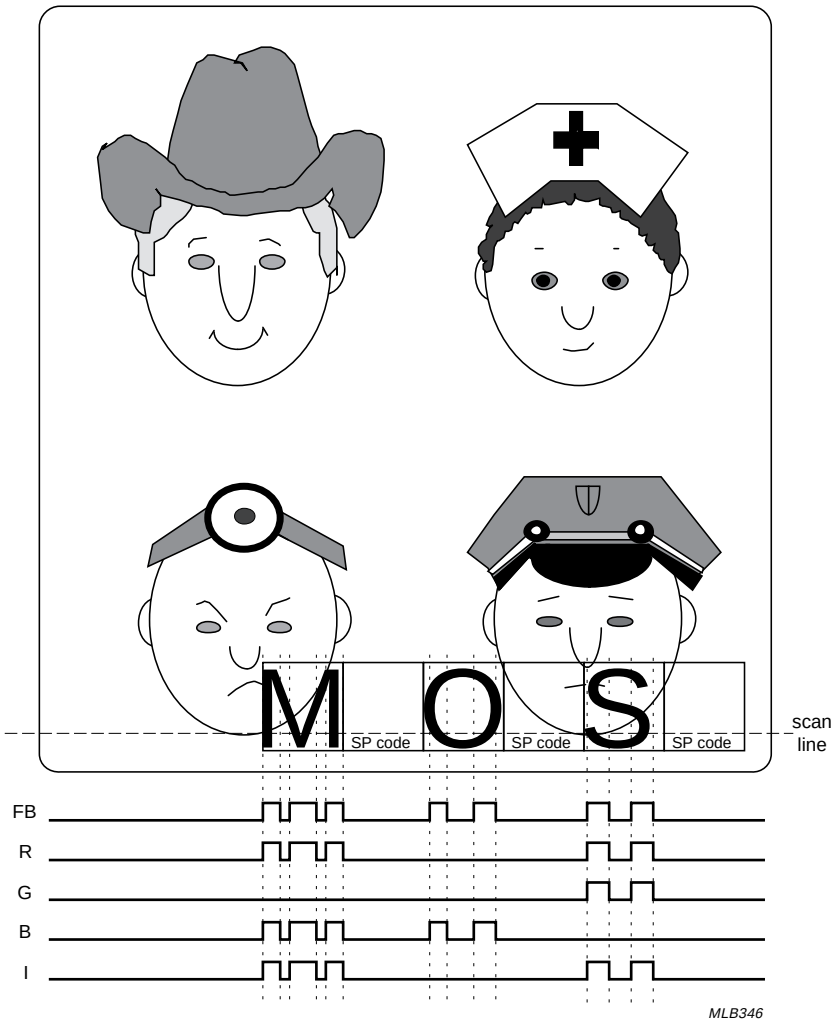
This command loads Control Register 3 with data that controls both the character blinking frequency and the active ratio of the character blinking frequency.
Figures 25 to 29 show how blinking influences the display in different display modes.

Table 30 Selection of Blinking frequency

BF1	BF0	BLINKING FREQUENCY (Hz)
0	0	$\frac{f_{VSYNC}}{16}$; this is the default setting
0	1	$\frac{f_{VSYNC}}{32}$
1	0	$\frac{f_{VSYNC}}{64}$
1	1	$\frac{f_{VSYNC}}{128}$

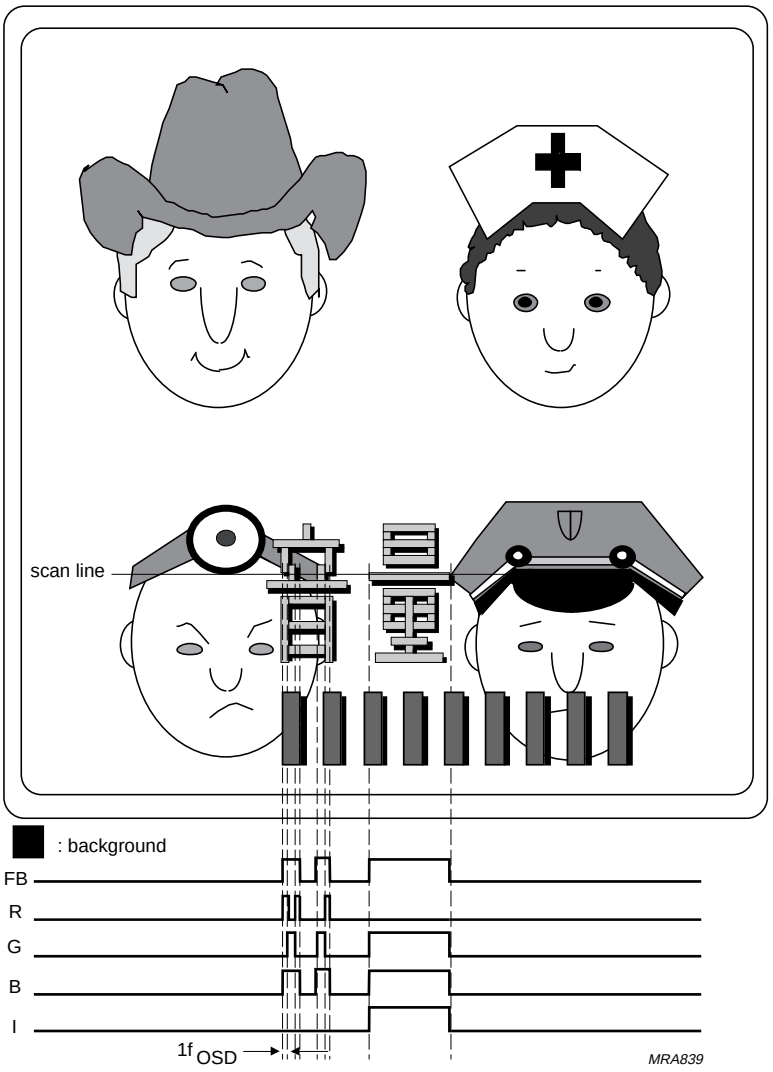
Table 31 Selection of active ratio of character blinking

BR1	BR0	ACTIVE RATIO
0	0	3 : 1 (the default setting)
0	1	1 : 1
1	0	1 : 3
1	1	reserved



'M' : Red + Blue + Intensity
'O' : Blue
'S' : Red + Green + Intensity
Bp = 1

Fig.15 Mode 0: No background mode.



1st character: GREEN
2nd character: GREEN + BLUE + INTENSITY
background: RED + BLUE
Bp = 1 (active HIGH)
Available only in character sizes 2V/2H or 4V/4H.

Fig.16 Mode 1: North-West shadowing mode.

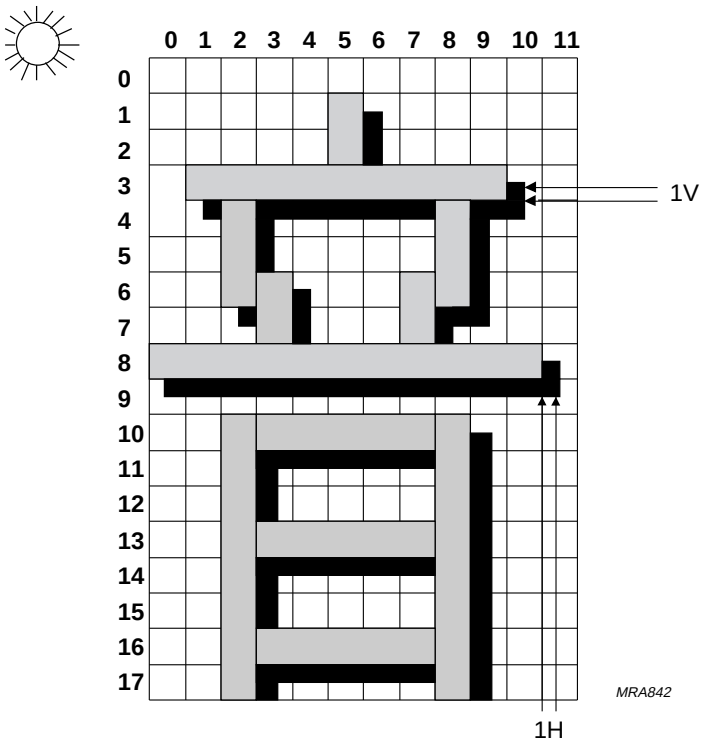


Fig.17 Example of North-West shadowing mode - size 2V/2H.

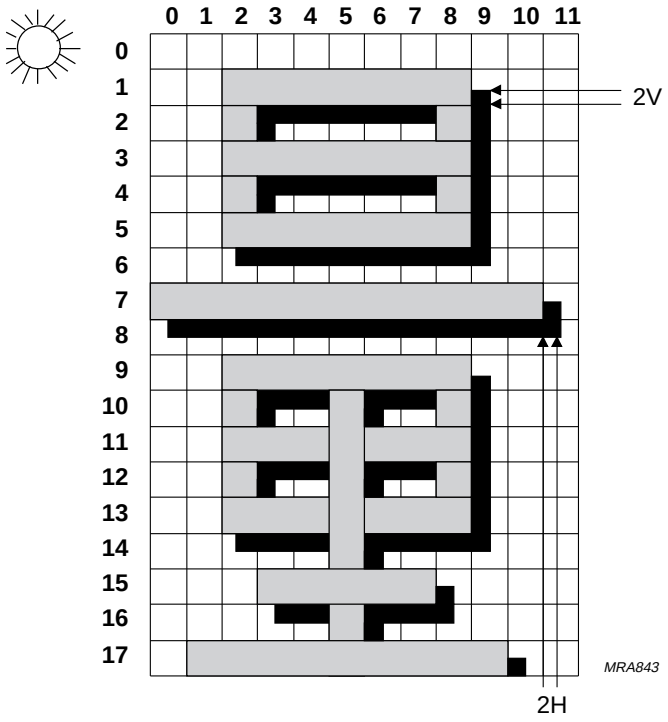


Fig.18 Example of North-West shadowing mode - size 4V/4H.

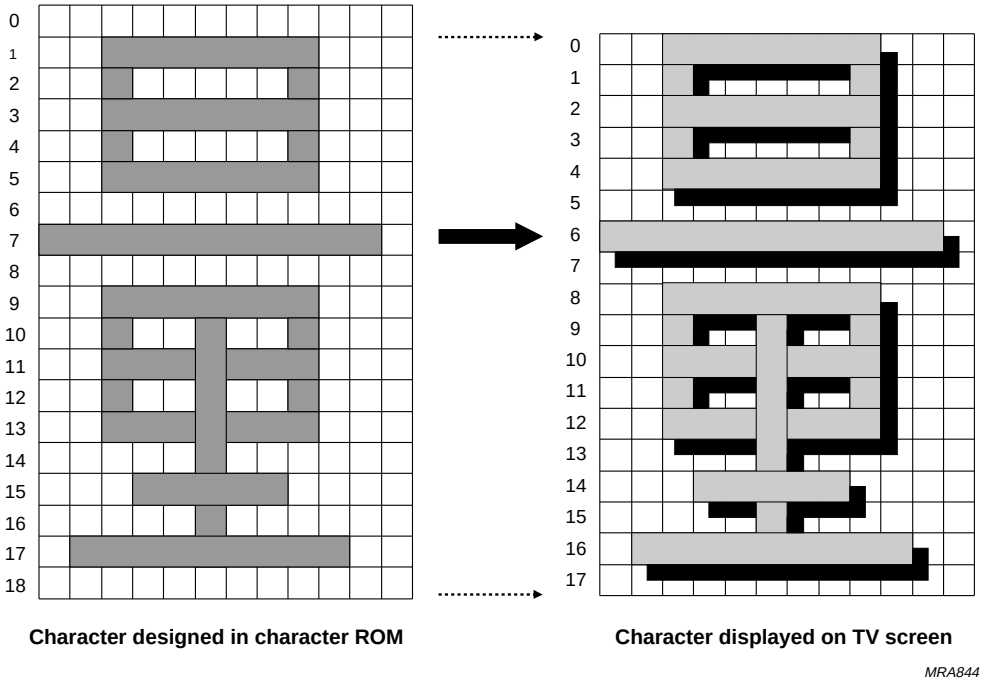


Fig.19 Example of North-West shadowing mode.

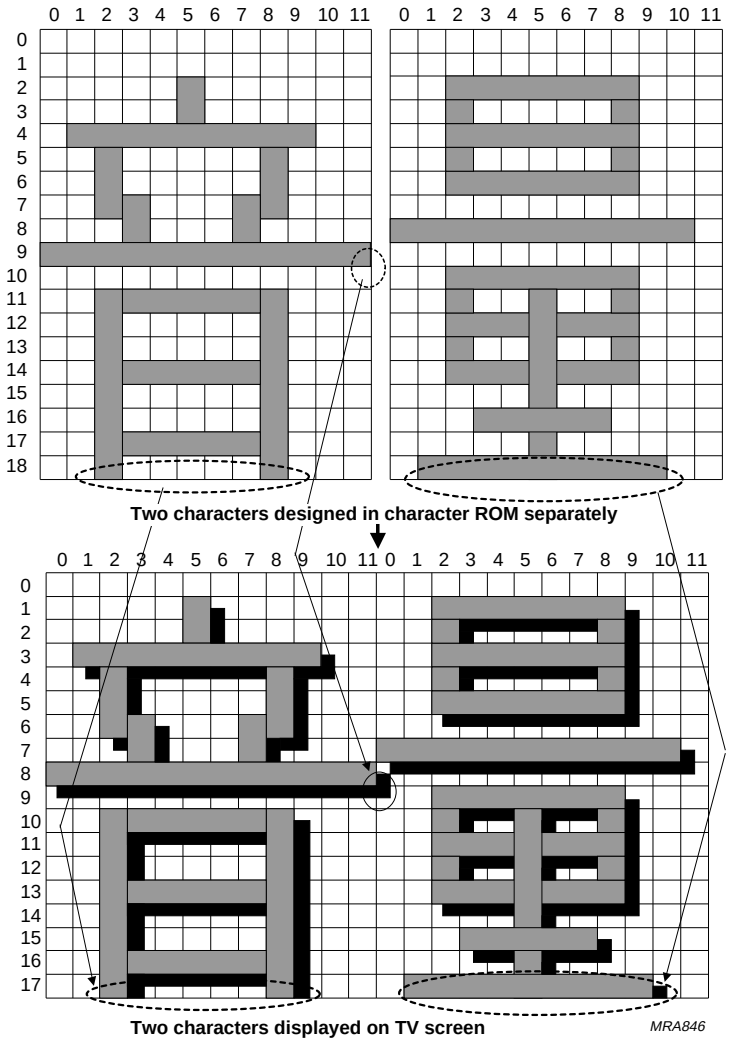


Fig.20 North-West shadowing.

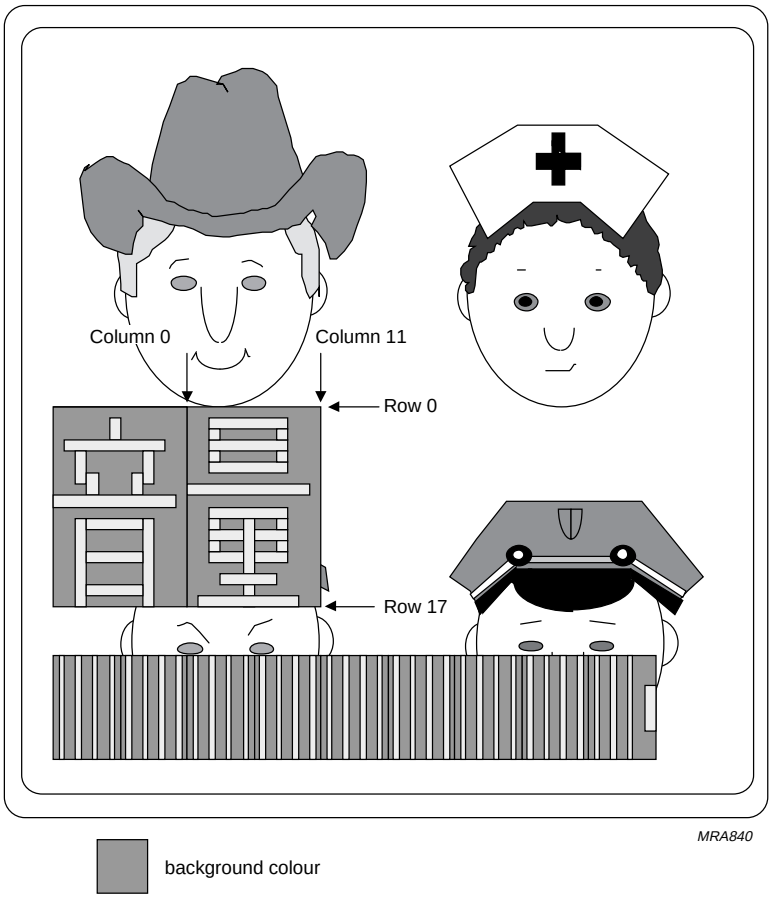


Fig.21 Mode 2: Box shadowing mode.

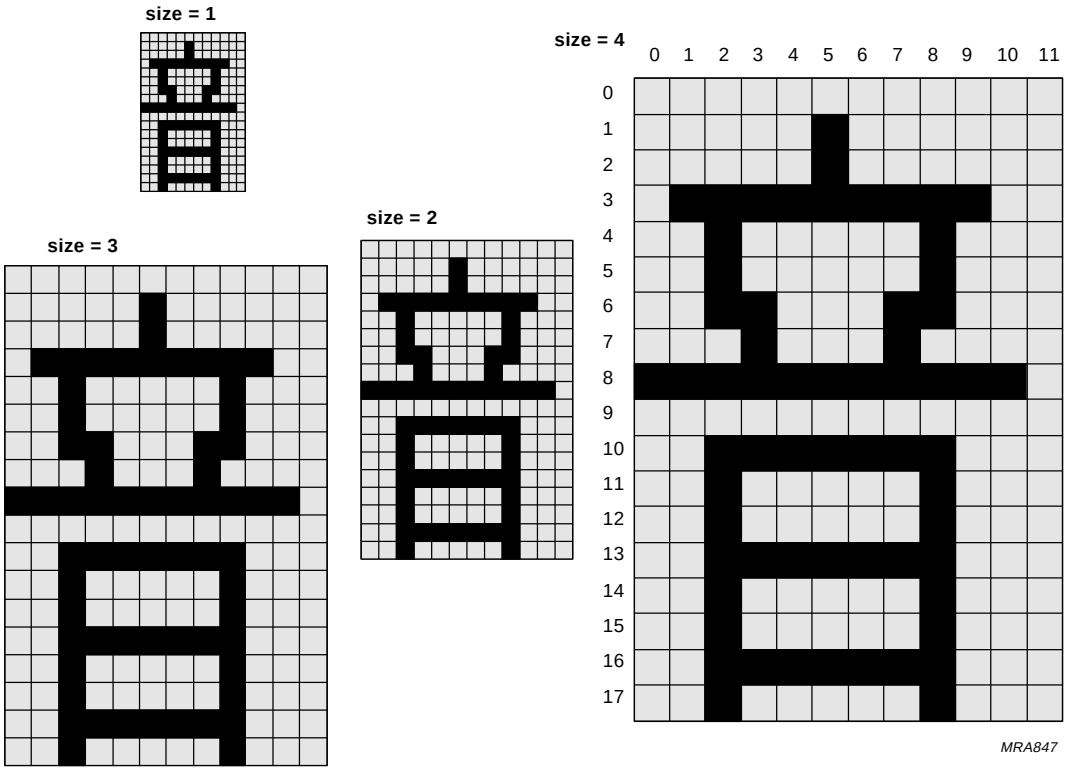


Fig.22 Example of Box shadowing mode.