# PBR 5111/2
# LPC Line Resistor Network

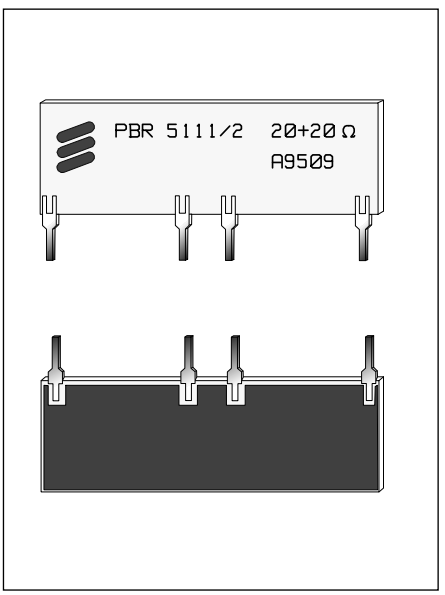
## Description

The Line Protection Resistor Network (LPC) PBR 5111/2 consists of a ratio matched pair of thickfilm resistors on a ceramic substrate. PBR 5111/2 is used in telephone line interface overvoltage protection networks, where the LPC resistors limit the current flow through voltage clamping devices such as diodes, tranzorbs, silicon thyristor diode transient suppressors etc.

The resistors will withstand multiple voltage/current surges of either polarity without failure and with only a negligible change inside specified values.If exposed to destructive power cross conditions, the LPC will act as a fuse depending on the applied condition. The PBR 5111/2 meets requirements set forth in ITU-T k17/k20 , UL 94-V0 and UL 1459.

## Key Features

- Two matched resistors in a single-in-line package
- Ratio match maintained after multiple surges
- Ratio match maintained after multiple non destructive power cross
- Fuse function for destructive power cross
- Non-flammable materials
- Auto insertable
- Low mechanical profile .




*Line Resistor Network PBR 5111/2.*

## Absolute Maximum Ratings

Tamb = +25 ± 2 °C unless otherwise stated.

| Parameter | Symbol | Min | Max. | Unit |
|---|---|---|---|---|
| **Temperature** | | | | |
| Storage temperature range | $T_{stg}$ | -55 | +125 | °C |
| Operating temperature range | $T_{amb}$ | -40 | +85 | °C |
| **Power Dissipation**, $T_{amb}$ = + 85 °C | | | | |
| Per resistor | $P_{diss}$ | | 1 | W |
| Per component | $P_{diss}$ | | 2 | W |
| **Surge Voltage 10/700 µs, 1500 V** (note 1, 2, 4) | | | | |
| Change in resistance after 10 surges CM - DM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 10 surges (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Surge Voltage 6/400 µs, 600 V** (note 1, 3, 4) | | | | |
| Change in resistance after 10 surges CM - DM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 10 surges (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Surge Voltage 10/1000 µs, 450 V** (note 1, 3) | | | | |
| Change in resistance after 100 surges CM - DM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 100 surges (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Surge Voltage 1/2 µs, 1500 V** (note 1, 3) | | | | |
| Change in resistance after 10 surges CM - DM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 10 surges (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Surge Voltage 2/10 µs, 665 V** (note 1, 3) | | | | |
| Change in resistance after 20 surges CM - DM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 20 surges (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Power Induction 600 VAC, 600 Ω** (note 1, 4) | | | | |
| Duration of Voltage | $t_{on}$ | | 1,0 | s |
| Change in resistance after 60 applications CM - DM (60 s pulse to pulse) | ΔR1, R2 | -2 | +2 | % |
| Change in ratio (matching) after 60 applications (CM - DM) | Δ(R1/R2) | -1 | +1 | % |
| **Power Induction 220 VAC, 600 Ω** (note 1, 4) | | | | |
| Duration of Voltage | $t_{on}$ | | 15 | min |
| Change in resistance after 1 application CM | ΔR1, ΔR2 | -2 | +2 | % |
| Change in ratio (matching) after 1 application (CM) | Δ(R1/R2) | -1 | +1 | % |
| **Power Contact 220 VAC Destructive, ≤10 Ω** (note 1, 5) | | | | |
| Duration of Voltage | $t_{on}$ | | 15 | min |
| **Power Contact Destructive, ≤3 Ω** (note 1, 5) | | | | |
| Duration of Voltage | $t_{on}$ | | 15 | min |
| Voltage | U | 100 | 600 | VAC |

## Electrical Characteristics

Tamb = +25 ± 2 °C unless otherwise stated.

| Parameter | Condition | Min | Typical | Max. | Unit |
|---|---|---|---|---|---|
| **Resistance/Ratio** | | | | | |
| Resistor R1, R2 | | 19,8 | 20 | 20,2 | Ω |
| Ratio R1/R2 | | 0,995 | 1,0 | 1,005 | - |
| R1, R2: Resistance Vs Temperature | $T_{amb}$ = -40 to + 85 °C | 19,7 | 20,0 | 20,3 | Ω |
| Tracking R1 - R2 | $T_{amb}$ = -40 to + 85 °C | 0,995 | 1,00 | 1,005 | - |
| Insulation | | | | | |
| Insulation R1 - R2 | U = 500 VDC | 1000 | | | MΩ |

### Notes

*Note 1*: Common Mode (CM) and Differential Mode (DM) are applied if stated. DM equals R1 or R2 tested, CM R1 and R2 simultaneously

*Note 2:* Surge voltage shape measured according to IEC 60-2, section 4. Surge voltage, peak voltage, shape and schematics according to ITU-T rec. k17. The surge peak voltage over the resistors: 500 V.

*Note 3:* Surge voltage shape measured according to IEC 60-2, section 4. Surge voltage pulse shape over the resistor.

*Note 4:* Reference: ITU-T k20

*Note 5:* For the test, the requirements are:

* The line resistor is not to start to burn with open flame
* No induction of fire of the surroundings

## Pin Description

Figure 1: Circuit diagram Pin 1 is the leftmost pin on the side with marking. Pin 7 and 9 are named a and b and equal the outgoing line). All other combinations of placing of a and b are less severe than above stated due to the design of the line resistor.

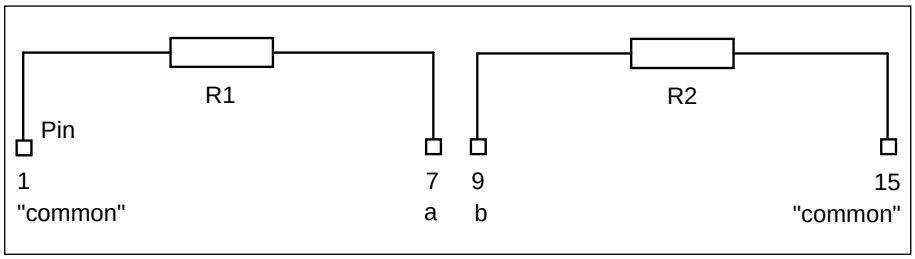



*Figure 1. Circuit diagram.*

## Functional Description

### General

The Line Protection Resistor Network consists of two thickfilm resistors screenprinted onto a ceramic substrate. The LPC is designed to break open when exposed to power cross conditions; i.e. to act as a fuse. It is also designed to fulfil surge voltage requirements set forth in ITU-T k17/k20 and Bellcore.

### High voltage characteristics

For high voltages, i.e. surge voltage and power cross test, the resistance of the LPC is not lower than 19,5 ohms and not higher than 20,5 ohms.

### Break open characteristics

The LPC has the following break open-characteristics: Common Mode (CM) and Differential Mode (DM) are applied if stated. DM equals R1 or R2 tested, CM R1 and R2 simultaneously For currents up to 0,5 A in DM and 1,0 A in CM the LPC will not break open. Max. temperature is 200 °C depending on design of PCB. Peak temperature is reached after three minutes. For currents 0,5 - 2,0 A in DM and 1,0 - 3,0 A in CM the LPC will not break open. High temperature, i.e. above 200 °C, is reached within 30 s. If the break open time is more than 1 s, high temperatures might be reached. Note: In DM, the LPC will not break both the ”a”- and ”b” branch open; i.e. if the voltage is applied to ”a”, only R1 will break open within stated time. See also diagram 1.

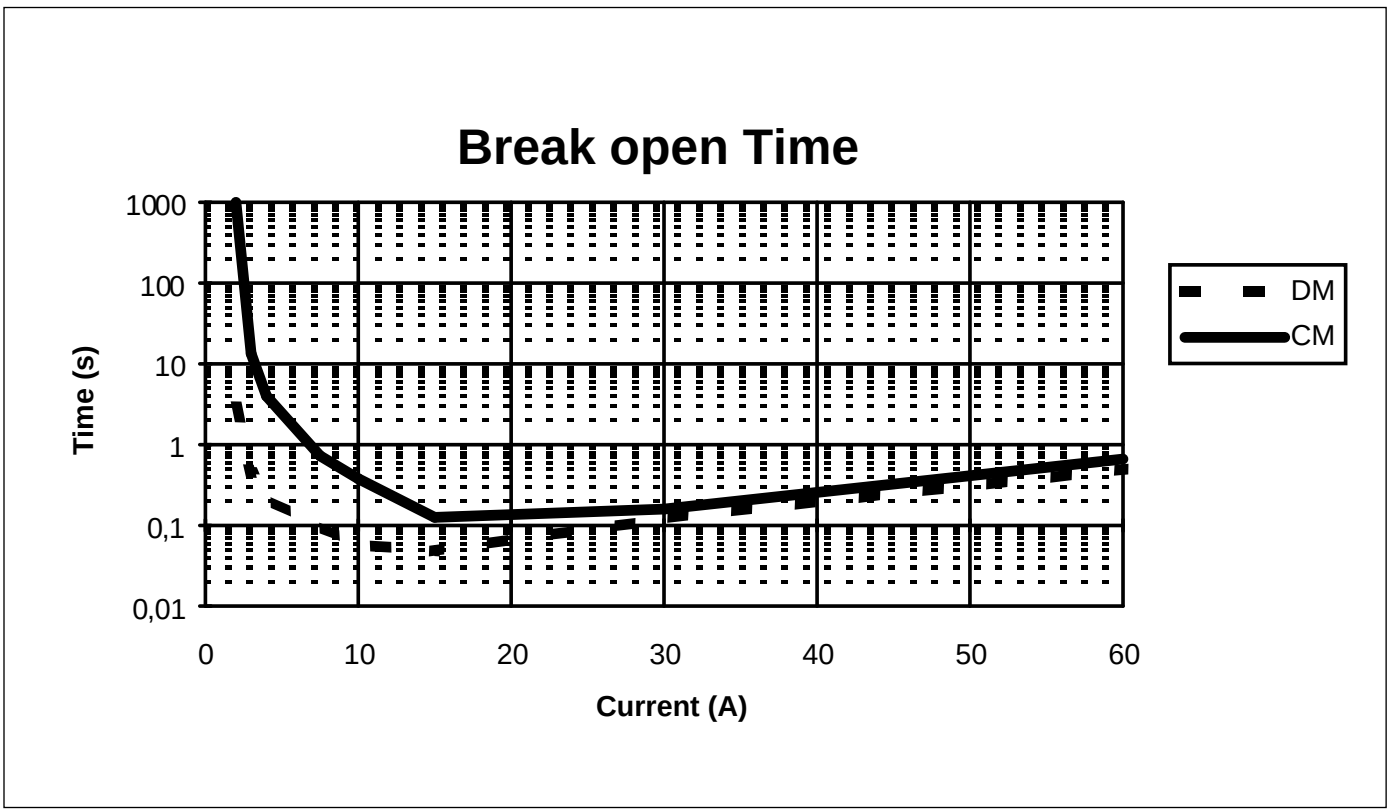



*Figure 2. Diagram 1 Break open Time.*

## Mechanical Outline

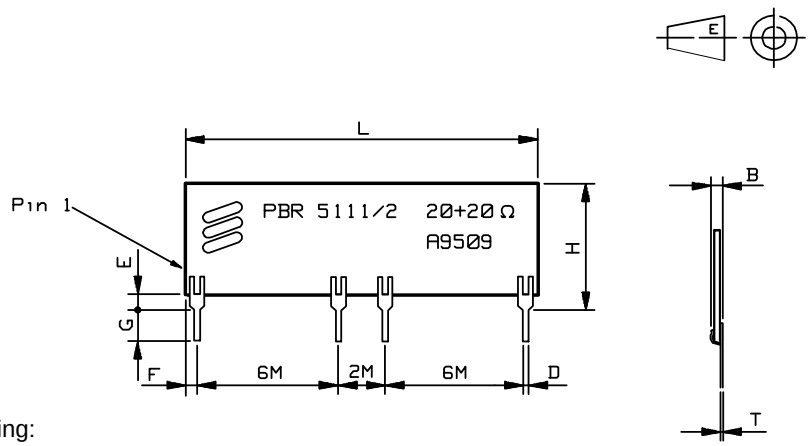
**Quality Specifications**

The LPC is delivered at the following AQL: Resistance, Ratio:
AQL 0,4, Level II
Surge Voltage, Power Cross:
AQL 1,0, Level S-3
according to:
IEC 410, MIL STD 105.

**Pin types and Package**

Three different pins are available:
*Type A:* Non-preformed lead for 0,8-1,0 mm through-hole-mounting.
*Type B:* Pre-formed lead for 1,0 mm through-hole-mounting.
*Type C:* (On Request) Pre-formed lead for 0,8 mm through-hole-mounting.

Two types of packages are available:
*Bulk:* with the LPC's individually fixed in a carrier.
*Taped:* (On Request) with the LPC's placed on a tape as described in IEC 286-2




All dimensions in mm.

| | | |
|---|---|---|
| B: | 1,5 | ± 0,3 |
| D: | 0,5 | ± 0,1 |
| E: | 1,0 | + 0,25 |
| | | - 0,15 |
| F: | 1,27 | ± 0,25 |
| G: | 3,2 | + 0,2 |
| | | - 0,3 |
| H: | 12,2 | + 0,4 |
| | | - 0,1 |
| L: | 38,1 | ± 0,3 |
| M: | 2,54 | ± 0,1 n-a. |
| T: | 0,25 | ± 0,04 |

*Note:* Dimensions for Lead type A

Marking:
The LPC is marked shown in the mechanical outline; i.e.
The Ericsson Logotype, Product Number "PBR 5111/2" and code of manufacture: Year and week

*Figure. 3 Mechanical outline.*

## Ordering Information

The LPC may be ordered as:

PBR 5111/2 AK, PBR 5111/2 BK and PBR 5111/2 CK for Bulk

PBR 5111/2 AT, PBR 5111/2 BT and PBR 5111/2 CT for Taped

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