National Semiconductor

PAL20RA10
Programmable Array Logic (PAL®)

General Description

The PAL20RA10 is a new member of National's broad PAL family. It provides several new features which will dramatically benefit PAL users. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the RA (Registered Asynchronous) devices.

Programmable logic devices provide convenient solutions for a wide variety fo application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

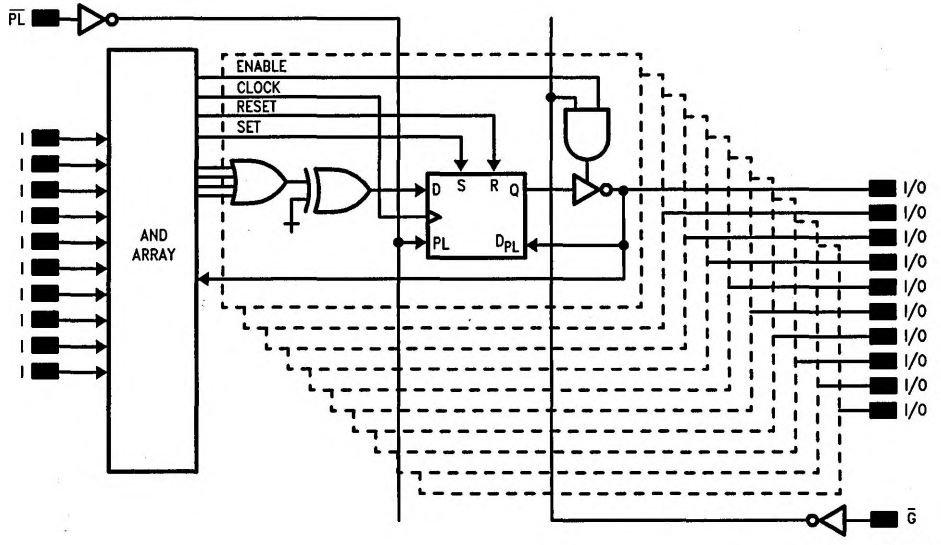
The PAL20RA10 is made up of ten Output Logic Macro Cells (OLMC). Four AND array outputs feed into the fixed OR-gate for each OLMC to generate the device's output functions. Four other AND array outputs are used for control functions in the OLMC. With a robust mixture of logic derived controlled functions and selectable output data paths, the PAL20RA10 provides an ideal solution for registered random logic applications.

This device is housed in a 24-pin 300 mil DIP. A 28-pin PCC package is also available. It can be programmed by most PAL programmers.

Features

- Programmable asynchronous set and reset
- Individually programmable clocks
- Programmable and hard-wired TRI-STATE® outputs
- Programmable output polarity
- Registers can be bypassed individually
- Register preload guarantees testability
- Outputs can be reconfigured as inputs
- Power-up reset for registered outputs
- Fully supported by National PLAN™ development software
- A variety of JEDEC-compatible programming equipment and design development software available
- Security fuse prevents direct copying of logic patterns

Block Diagram—PAL20RA10



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	Operating	Programming
Supply Voltage V_{CC}	7.0V	12.0V
Input Voltage	5.5V	22.0V
Off-State Output Voltage	5.5V	12.0V
Storage Temperature		−65°C to +150°C
ESD Tolerance (Note 2)		1000V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55			0		75	°C
T_C	Operating Case Temperature				125				°C
t_W	Pulse Width of Clocking Input (High/Low)		25	13		20	13		ns
t_{WP}	Pulse Width of Preload ($\overline{PL}$) Input (Low)		45	15		35	15		ns
t_{SU}	Setup Time from Input or Feedback to Clocking Input		25	10		20	10		ns
t_{SUP}	Setup Time from Input to $\overline{PL}$ High		30	5		25	5		ns
t_H	Hold Time of Input after Clocking Input	Polarity Fuse Intact	10	−2		10	−2		ns
		Polarity Fuse Blown	0	−6		0	−6		
t_{HP}	Hold Time of Input after $\overline{PL}$ High		30	5		25	5		ns
f_{CLK}	Clock Frequency (Note 3)	With Feedback			16.6			20	MHz
		Without Feedback			20			25	MHz

Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage	(Note 4)				0.8	V
V_{IH}	High-Level Input Voltage	(Note 4)		2.0			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min	I_I = −18 mA		−0.8	−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max	V_I = 0.4V		−0.02	−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = Max	V_I = 2.4V			25	μA
I_I	Maximum Input Current	V_{CC} = Max	V_I = 5.5V			100	μA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA		0.3	0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min	I_{OH}: Mil-2 mA Com-3.2 mA	2.4	2.8		V
I_{OZ}	Off-State Output Current	V_{CC} = Max	(Note 5) V_O = 0.4V or 2.4V	−100		100	μA
I_{OS}	Output Short-Circuit Current	V_{CC} = 5V	(Note 6) V_O = 0V	−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max			155	200	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 are connected directly to the security fuses, and, although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 3: f_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
f_{CLK} without feedback is derived as $(2t_W)^{-1}$.

Note 4: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

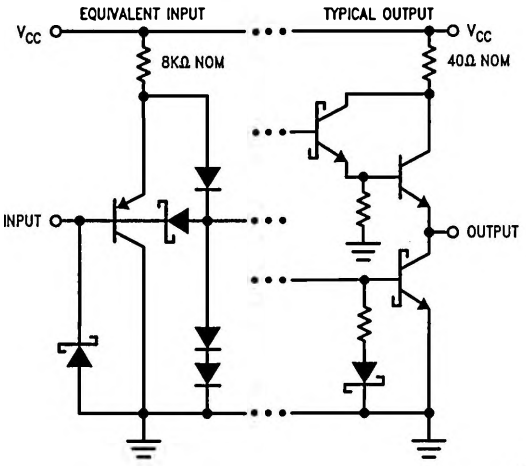
Note 5: I/O leakage as the worst case of I_{OZX} or I_{IX}, e.g. I_{IL} and I_{OZL}.

Note 6: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage otherwise may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	Polarity Fuse Intact	C_L = 50 pF, S1 Closed		20	35		20	30	ns
		Polarity Fuse Blown			25	40		25	35	
t_{CLK}	Clock Input to Registered Output or Feedback		C_L = 50 pF, S1 Closed	10	17	35	10	17	30	ns
t_S	Asynchronous Set Input to Registered Output Low				22	40		22	35	ns
t_R	Asynchronous Reset Input to Registered Output High				27	45		27	40	ns
t_{PZXG}	$\overline{G}$ Pin to Output Enabled		C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		10	25		10	20	ns
t_{PXZG}	$\overline{G}$ Pin to Output Disabled		C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed		10	25		10	20	ns
t_{PZXI}	Input to Output Enabled via Product Term		C_L = 50 pF, Active High: S1 Open, Active Low: S1 Closed		18	35		18	30	ns
t_{PXZI}	Input to Output Disabled via Product Term		C_L = 5 pF, From V_{OH}: S1 Open, From V_{OL}: S1 Closed		15	35		15	30	ns
t_{RESET}	Power-Up to Registered Output High				600	1000		600	1000	ns

Schematic of Inputs and Outputs



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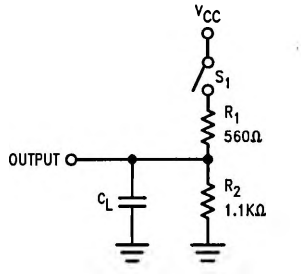
Test Load



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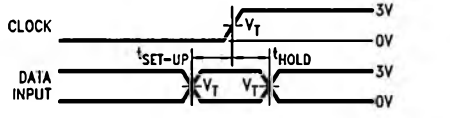
Test Waveforms

Set-Up and Hold



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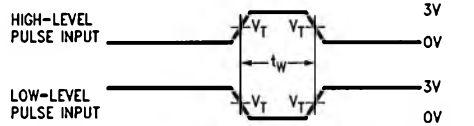
Pulse Width



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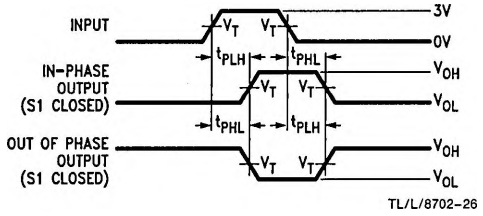
Propagation Delay



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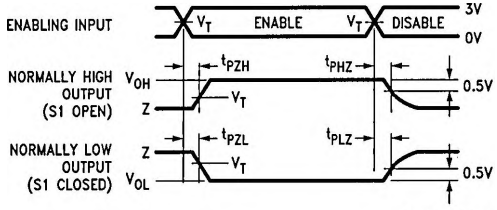
Enable and Disable



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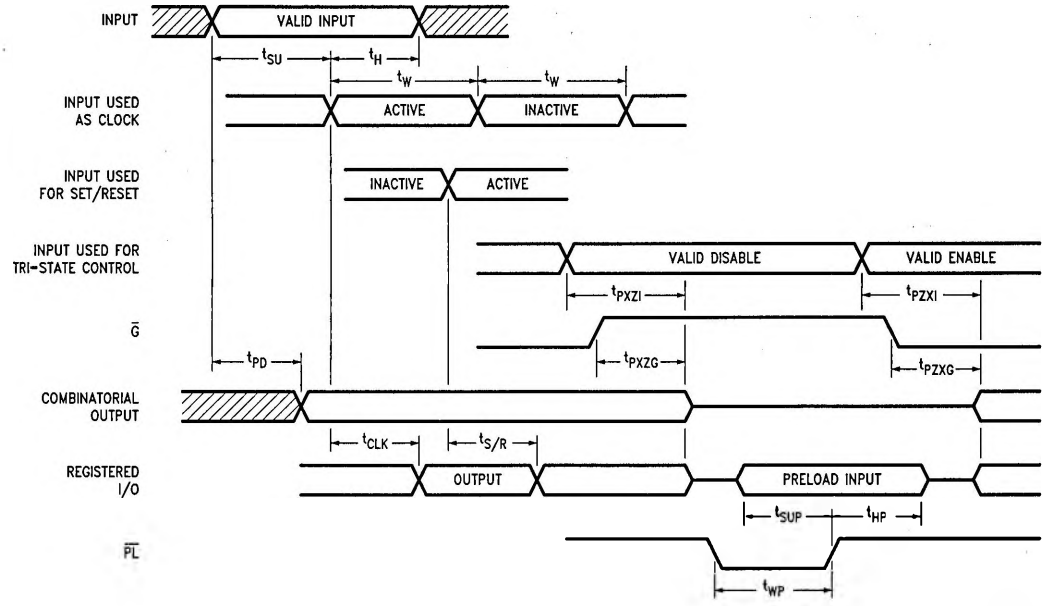
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



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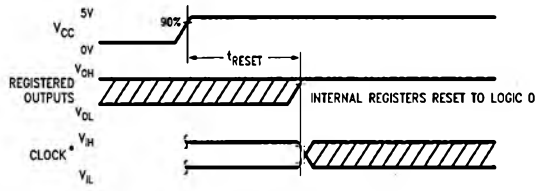
Power-Up Reset Waveform



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*The clock input should not be switched from low to high until after time t_{RESET}.

Functional Description

The PAL20RA10 logic array consists of 20 complementary input lines and 80 product-term lines with a programmable fuse link at each intersection (3200 fuses). The product terms are organized into ten groups of eight each. Four of the eight product terms in each group connect into an OR-gate to produce the sum-of-products logic function. The remaining four product terms in each group are used for control functions in the Output Logic Macro Cell (OLMC) as shown in *Figure 1.*

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

PROGRAMMABLE SET AND RESET

In each cell, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1, the output pin becomes a 0. If the reset product line is high, the register output becomes a logic 0, the output pin becomes a 1. The operation of the programmable set and reset overrides the clock.

INDIVIDUALLY PROGRAMMABLE REGISTER BYPASS

If both the set and reset product lines are high, the sum-of-products bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

PROGRAMMABLE CLOCK

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Functional Description (Continued)

PROGRAMMABLE AND HARD-WIRED TRI-STATE OUTPUTS

The PAL20RA10 provides a product term dedicated to output control. There is also an output control pin (Pin 13). The output is enabled if both the output control pin is low and the output control product term is HIGH. If the output control pin is high all outputs will be disabled or if an output control product term is low, then that output will be disabled.

OUTPUT CONTROL ALTERNATIVES

Output Always Enabled

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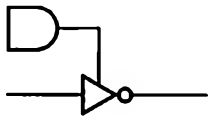
Programmable



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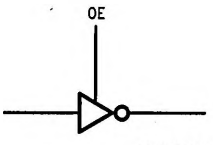
Hard-Wired



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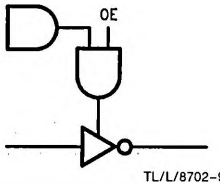
Combination of Programmable and Hard-Wired



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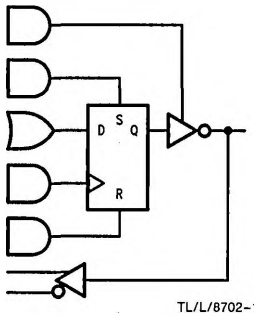
PROGRAMMABLE OUTPUT POLARITY

The outputs can be programmed either active-low or active-high. This is represented by the exclusive-or gates shown in the PAL20RA10 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high. Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity features allows the user a higher degree of flexibility when writing equations.

POWER-UP RESET

The PAL20RA10 device resets all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

Registered/Active Low



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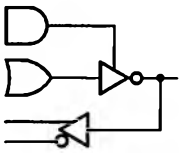
Combinatorial/Active Low



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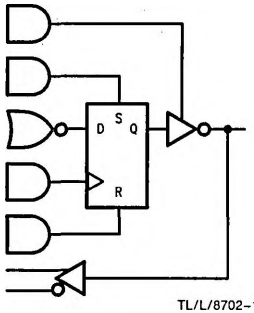
Registered/Active High



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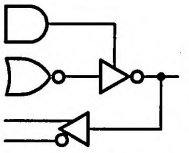
Combinatorial/Active High



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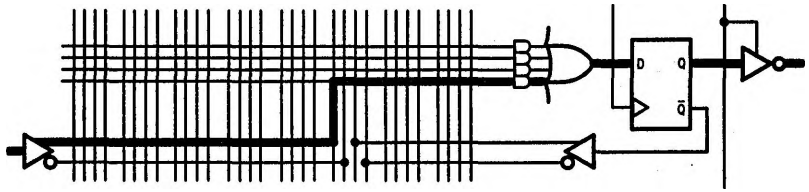
As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period (t_W high + t_W low) and the minimum "data window" period (t_{SU} + t_H). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as t_{CLK} + t_{SU}. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Functional Description (Continued)

Typical Registered Logic Function Without Feedback



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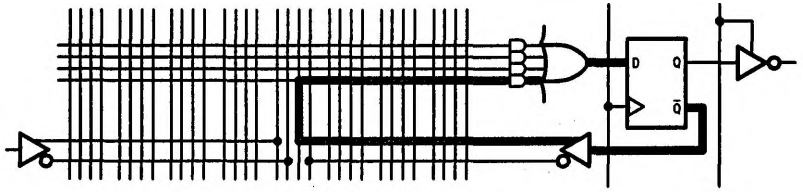
Typical Registered Logic Function With Feedback



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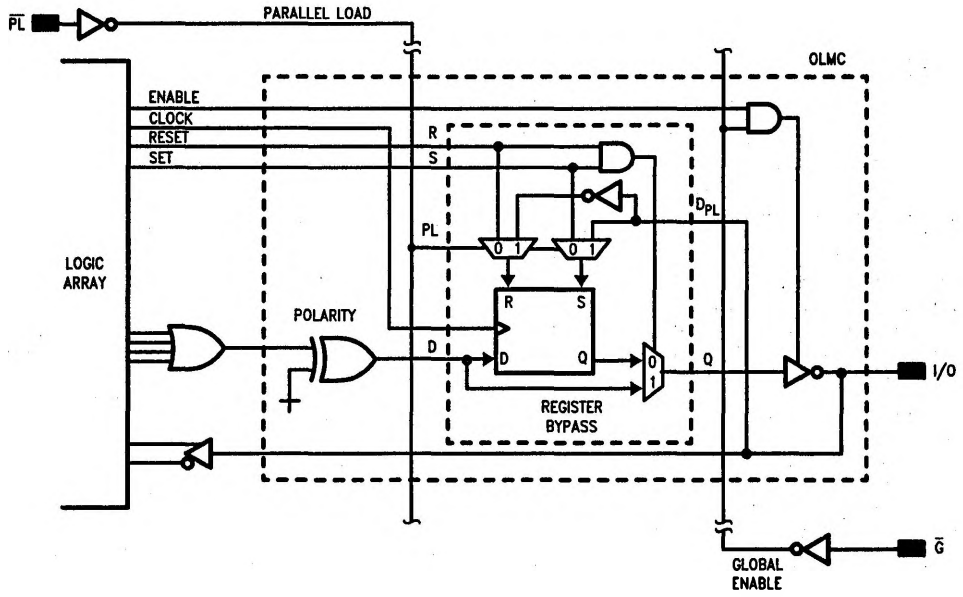

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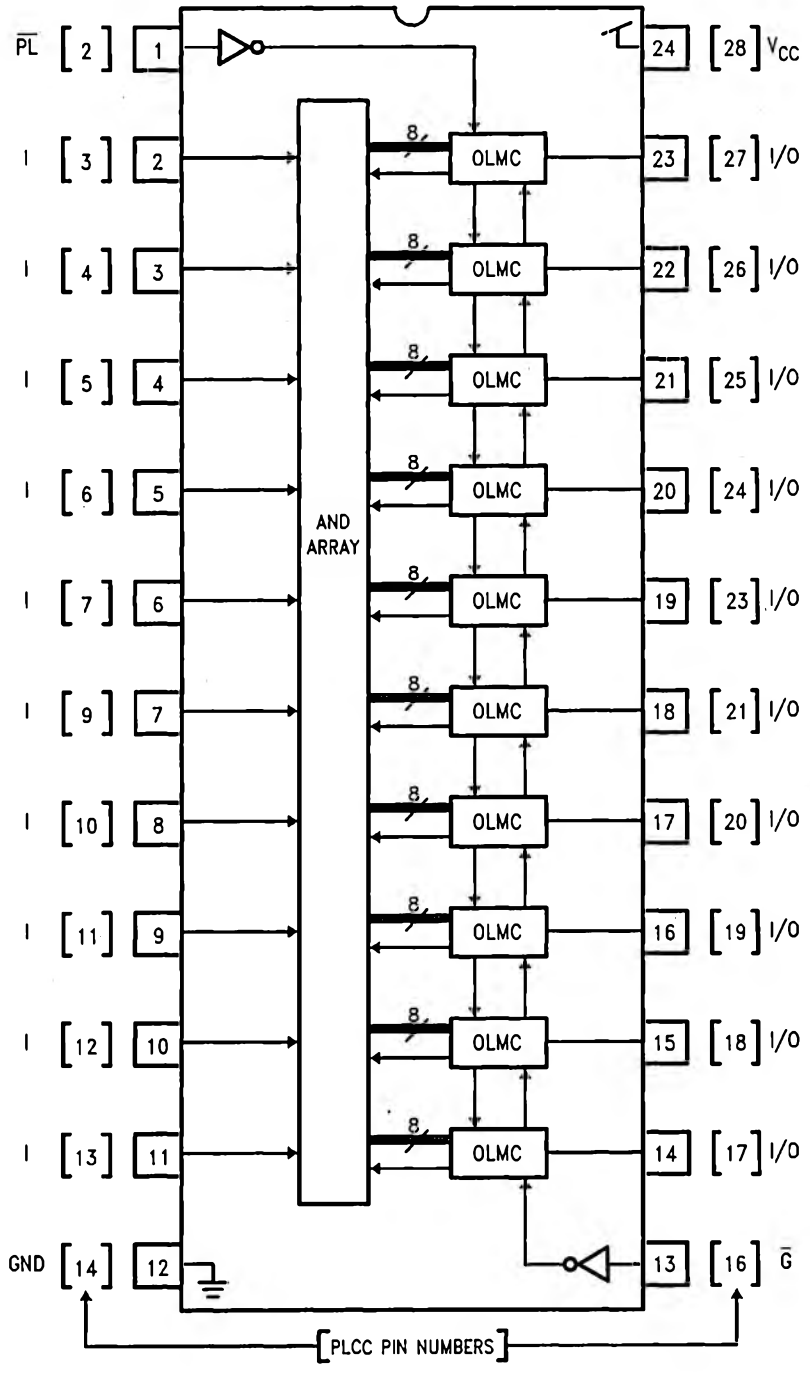
FIGURE 1. "RA" Output Logic Macrocell Logic Diagram

24-Pin PAL20RA10 Block Diagram—DIP Connections



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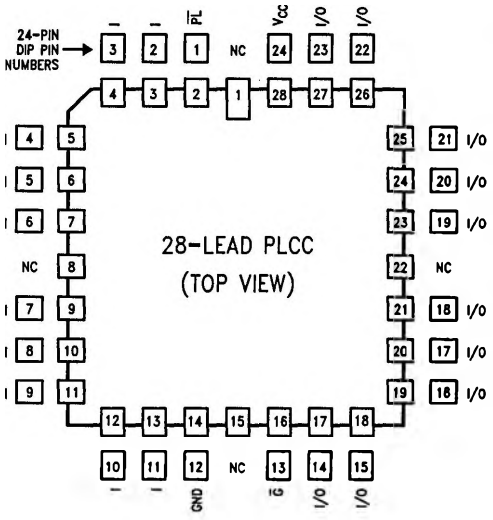
28-Lead PLCC Connection Diagram



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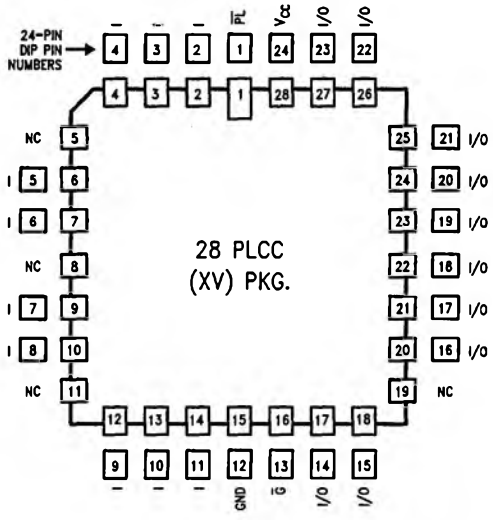
Non-JEDEC PLCC Diagram



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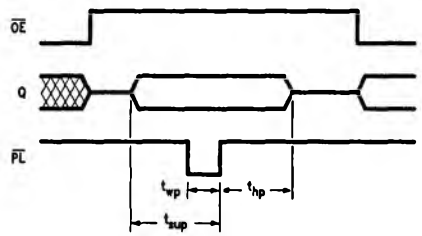
Note: For availability of old (Non-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor.

Output Register Preload

Register preload allows any arbitrary state to be loaded into the PAL output registers. This allows complete logic verification, including states that are impossible or impractical to reach. To use the preload feature, first disable the outputs by bringing $\overline{OE}$ high, and present the data at the output pins. A low-level on the preload pin ($\overline{PL}$) will then load the data into the registers.



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Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format en-

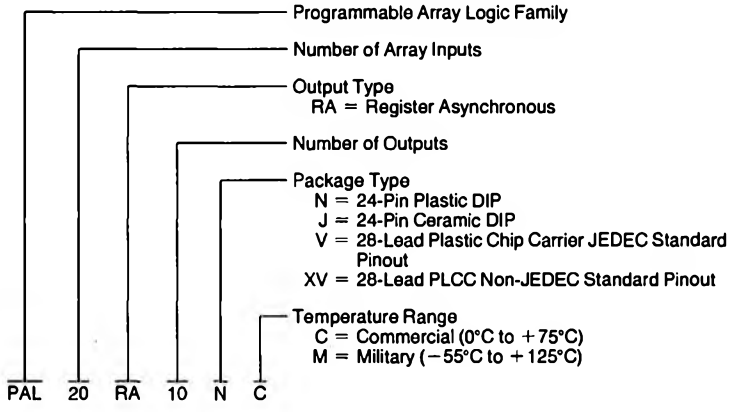
Design Development Support (Continued)

sures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

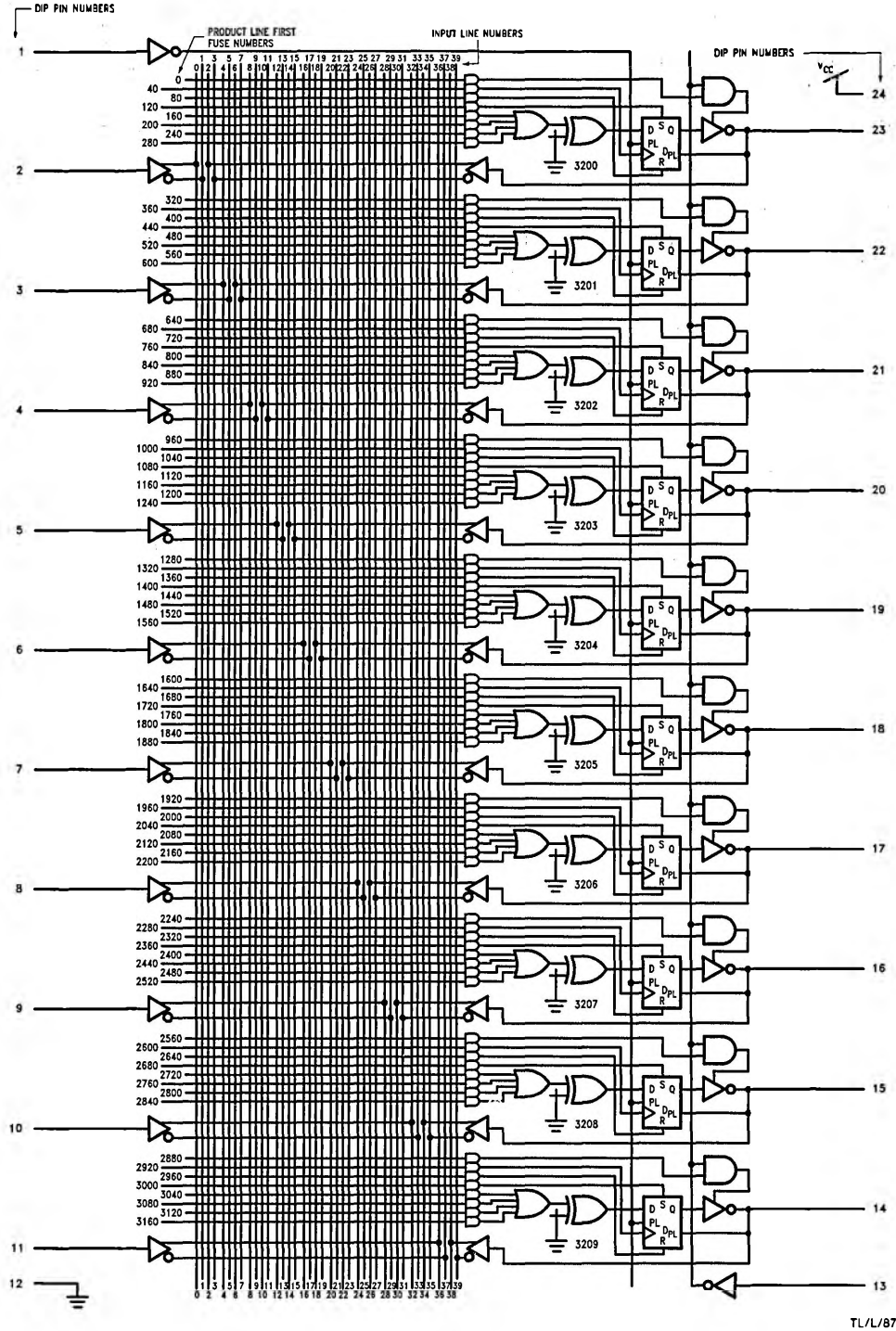
A detailed logic diagram showing all JEDEC fuse-map addresses for the PAL20RA10 is provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Logic Diagram—PAL20RA10



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JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.