

Programmable Array Logic (PAL®) 24-Pin Medium PAL Family

General Description

The 24-pin Medium PAL family contains four of the most popular PAL architectures with speeds as fast as 10 ns maximum propagation delay. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the Series A and Series B devices. Series D devices are manufactured using National Semiconductor's isoplanar "FAST-Z" TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration ("AIM") technology offering very high programming yields and is an extension of National's FAST® logic family. The 24-pin Medium PAL family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy. The PAL logic array has a total of 20 complementary input pairs and 8 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions

(combinatorial) or passed through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixtures, as shown in the Device Types table below.

On power-up, Series-D devices reset all registers to simplify sequential circuit design and testing and for Series B devices, the registers are set on power-up. For Series D and Series B devices, direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- As fast as 10 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- High programming yield and reliability of vertical-fuse technology for Series D products. (Programming equipment with certified vertical-fuse algorithm required)
- Extension of FAST product line (Series-D).
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ software
- Power-up set/reset for registered outputs (Series-B, D)
- Register preload facilitates device testing (Series-B, D)
- Security fuse prevents direct copying of logic patterns

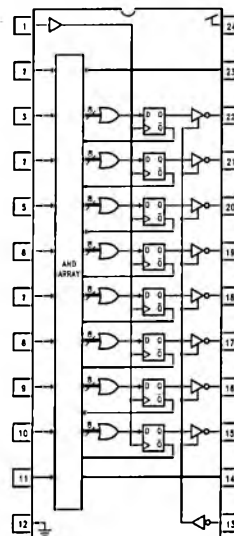
Device Types

Device Type	Dedicated Inputs	Registered Outputs (With Feedback)	Combinatorial	
			I/Os	Outputs
PAL20L8	14	—	6	2
PAL20R4	12	4	4	—
PAL20R6	12	6	2	—
PAL20R8	12	8	—	—

Speed/Power Versions

Series	Example	Commercial		Military	
		t _{PD}	I _{CC}	t _{PD}	I _{CC}
A	PAL 20L8A	25 ns	210 mA	30 ns	210 mA
B	PAL 20L8B	15 ns	210 mA	20 ns	210 mA
D	PAL20L8D	10 ns	210 mA		

Block Diagram—PAL20R8



TL/L/9394-1

Series A (PAL20L8A, PAL20R4A, PAL20R6A, PAL20R8A)**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5V to +7.0V
Input Voltage (Note 2)	−1.5V to +5.5V
Off-State Output Voltage (Note 2)	−1.5V to +5.5V
Input Current (Note 2)	−30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
ESD Tolerance (Note 3)	400V
$C_{ZAP} = 100$ pF	
$R_{ZAP} = 1500\Omega$	
Test Method: Human Body Model	
Test Specification: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55			0		75	°C
T_C	Operating Case Temperature			125				°C
t_W	Clock Pulse Width	Low	20	7	15	7		ns
		High	20	7	15	7		ns
t_{SU}	Setup Time from Input or Feedback to Clock	30	18		25	18		ns
t_H	Hold Time of Input after Clock	0	−10		0	−10		ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		20			28.5	MHz
		Without Feedback		25			33.3	MHz

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V _{IL}	Low Level Input Voltage (Note 6)						0.8	V
V _{IH}	High Level Input Voltage (Note 6)				2			V
V _{IC}	Input Clamp Voltage	V _{CC} = Min, I = −18 mA				−0.8	−1.5	V
I _{IL}	Low Level Input Current (Note 7)	V _{CC} = Max, V _I = 0.4V				−0.02	−0.25	mA
I _{IH}	High Level Input Current (Note 7)	V _{CC} = Max, V _I = 2.4V					25	μA
I _I	Maximum Input Current	V _{CC} = Max, V _I = 5.5V					100	μA
V _{OL}	Low Level Output Voltage	V _{CC} = Min	I _{OL} = 12 mA	MIL		0.3	0.5	V
			I _{OL} = 24 mA	COM				
V _{OH}	High Level Output Voltage	V _{CC} = Min	I _{OH} = −2 mA	MIL	2.4	3.4		V
			I _{OH} = −3.2 mA	COM				
I _{OZL}	Low Level Off-State Output Current (Note 7)	V _{CC} = Max	V _O = 0.4V				−100	μA
I _{OZH}	High Level Off-State Output Current (Note 7)	V _{CC} = Max	V _O = 2.4V				100	μA
I _{OS}	Output Short-Circuit Current (Note 8)	V _{CC} = 5V, V _O = 0V			−30	−70	−130	mA
I _{CC}	Supply Current	V _{CC} = Max, Outputs Open				160	210	mA

Series A (PAL20L8A, PAL20R4A, PAL20R6A, PAL20R8A) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: t_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.

t_{CLK} without feedback is derived as $(2t_w)^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

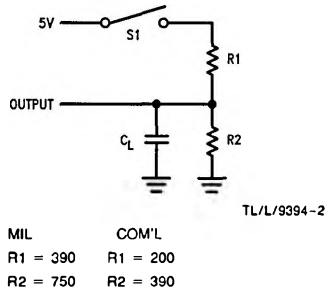
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OL} or between I_{IH} and I_{OH} .

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the t_{OG} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

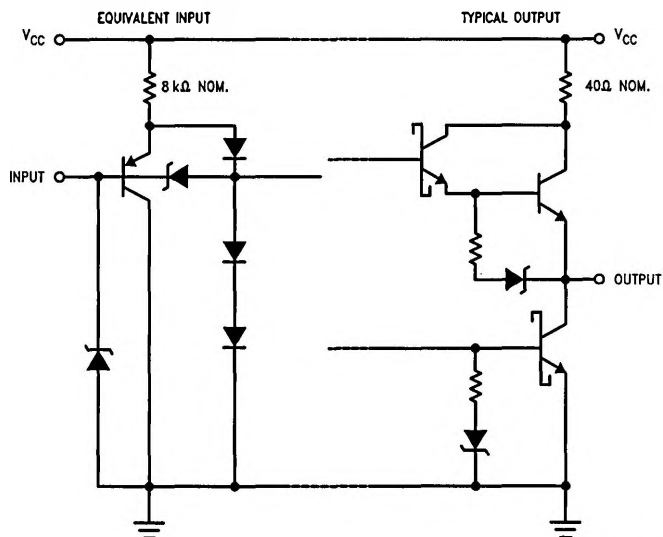
Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commerical			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	$C_L = 50$ pF, S1 Closed		18	30		18	25	ns
t_{CLK}	Clock to Registered Output or Feedback	$C_L = 50$ pF, S1 Closed		12	20		12	15	ns
t_{PZG}	$\bar{G}$ Pin to Registered Output Enabled	$C_L = 50$ pF, Active High: S1 Open, Active Low: S1 Closed		10	25		10	20	ns
t_{PXG}	$\bar{G}$ Pin to Registered Output Disabled	$C_L = 5$ pF, From V_{OH} : S1 Open, From V_{OL} : S1 Closed		11	25		11	20	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	$C_L = 50$ pF, Active High: S1 Open, Active Low: S1 Closed		10	30		10	25	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	$C_L = 5$ pF, From V_{OH} : S1 Open, From V_{OL} : S1 Closed		13	30		13	25	ns

Test Load



Schematic of Inputs and Outputs



TL/L/9394-28

Series B (PAL20L8B, PAL20R4B, PAL20R6B, PAL20R8B)**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	–0.5V to +7.0V
Input Voltage (Note 2)	–1.5V to +5.5V
Off-State Output Voltage (Note 2)	–1.5V to +5.5V
Input Current (Note 2)	–30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
Junction Temperature	–65°C to +150°C
ESD Tolerance (Note 3)	1500V
C_{ZAP}	100 pF
R_{ZAP}	1500Ω
Test Method: Human Body Model	
Test Specification: NSC SOP-5-028	

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	–55			0		75	°C
T_C	Operating Case Temperature			125				°C
t_W	Clock Pulse Width							
	Low	12	8		10	5		ns
	High	12	8		10	5		ns
t_{SU}	Setup Time from Input or Feedback to Clock	20	10		15	10		ns
t_H	Hold Time of Input after Clock	0	–5		0	–5		ns
f_{CLK}	Clock Frequency (Note 4)			28.5			37	MHz
	Without Feedback			41.7			50	MHz

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V _{IL}	Low Level Input Voltage (Note 6)						0.8	V
V _{IH}	High Level Input Voltage (Note 6)				2			V
V _{IC}	Input Clamp Voltage	V _{CC} = Min, I = −18 mA				−0.8	−1.5	V
I _{IL}	Low Level Input Current (Note 7)	V _{CC} = Max, V _I = 0.4V				−0.02	−0.25	mA
I _{IH}	High Level Input Current (Note 7)	V _{CC} = Max, V _I = 2.4V					25	μA
I _I	Maximum Input Current	V _{CC} = Max, V _I = 5.5V					100	μA
V _{OL}	Low Level Output Voltage	V _{CC} = Min	I _{OL} = 12 mA	MIL		0.3	0.5	V
			I _{OL} = 24 mA	COM				
V _{OH}	High Level Output Voltage	V _{CC} = Min	I _{OH} = −2 mA	MIL	2.4	3.4		V
			I _{OH} = −3.2 mA	COM				
I _{OZL}	Low Level Off-State Output Current (Note 7)	V _{CC} = Max	V _O = 0.4V				−100	μA
I _{OZH}	High Level Off-State Output Current (Note 7)	V _{CC} = Max	V _O = 2.4V				100	μA
I _{OS}	Output Short-Circuit Current (Note 8)	V _{CC} = 5V, V _O = 0V			−30	−70	−130	mA
I _{CC}	Supply Current	V _{CC} = Max, Outputs Open				160	210	mA

Series B (PAL20L8B, PAL20R4B, PAL20R6B, PAL20R8B) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: t_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.

t_{CLK} without feedback is derived as $(2t_w)^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

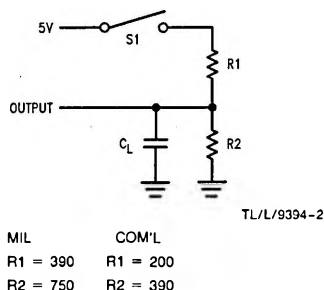
Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OL} or between I_{IH} and I_{OH} .

Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

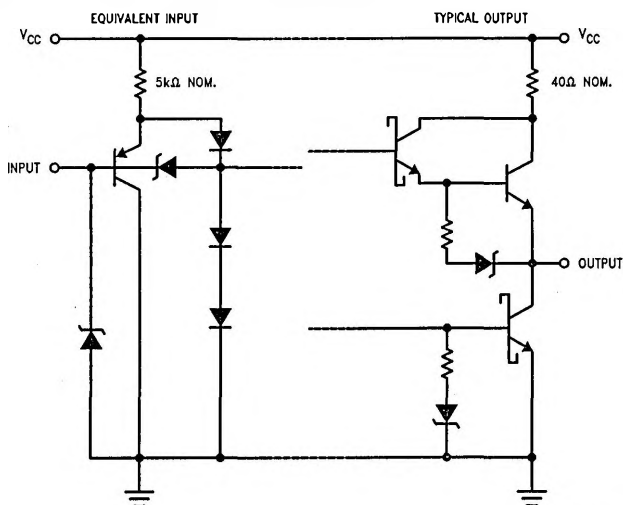
Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commerical			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	$C_L = 50 \text{ pF}$, S1 Closed		11	20		11	15	ns
t_{CLK}	Clock to Registered Output or Feedback	$C_L = 50 \text{ pF}$, S1 Closed		8	15		8	12	ns
t_{PZG}	$\bar{G}$ Pin to Registered Output Enabled	$C_L = 50 \text{ pF}$, Active High: S1 Open, Active Low: S1 Closed		10	20		10	15	ns
t_{PXG}	$\bar{G}$ Pin to Registered Output Disabled	$C_L = 5 \text{ pF}$, From V_{OH} : S1 Open, From V_{OL} : S1 Closed		8	20		8	12	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	$C_L = 50 \text{ pF}$, Active High: S1 Open, Active Low: S1 Closed		11	20		11	15	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	$C_L = 5 \text{ pF}$, From V_{OH} : S1 Open, From V_{OL} : S1 Closed		11	20		11	15	ns
t_{SET}	Power-Up to Registered Output Low			600	1000		600	1000	ns

Test Load



Schematic of Inputs and Outputs



Series D (PAL20L8D, PAL20R4D, PAL20R6D, PAL20R8D)**PRELIMINARY****Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	–0.5V to +7.0V
Input Voltage (Note 2)	–1.5V to +7.0V
Off-State Output Voltage (V_O) (Notes 2 & 3)	–1.5V to +5.5V
Input Current (Note 2)	–30 mA to +5.0 mA
Output Current (I_{OL})	+100 mA

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
Junction Temperature	–65°C to +150°C
ESD Tolerance	2000V
C_{ZAP}	100 pF
R_{ZAP}	1500Ω
Test Method:	Human Body Model
Test Specification:	NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Commercial			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	0	25	75	°C
t_W	Clock Pulse Width	Low			ns
		High			ns
t_{SU}	Setup Time from Input or Feedback to Clock	10			ns
t_H	Hold Time of Input after Clock	0			ns
f_{CLK}	Clock Frequency (Note 4)	With Feedback		55.5	MHz
		Without Feedback		71.4	MHz
V_Z	Register Preload Control Voltage	9.5	9.75	10.0	V

Electrical Characteristics Over Recommended Operating Conditions (Note 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 6)				0.8	V
V_{IH}	High Level Input Voltage (Note 6)		2			V
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min}, I = -18 \text{ mA}$			–1.2	V
I_{IL}	Low Level Input Current (Note 7)	$V_{CC} = \text{Max}, V_I = 0.4 \text{ V}$			–250	μA
I_{IH}	High Level Input Current (Note 7)	$V_{CC} = \text{Max}, V_I = 2.4 \text{ V}$			25	μA
I_I	Maximum Input Current	$V_{CC} = \text{Max}, V_I = 5.5 \text{ V}$			100	μA
V_{OL}	Low Level Output Voltage	$V_{CC} = \text{Min}$ $I_{OL} = 24 \text{ mA}$			0.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = \text{Min}$ $I_{OH} = -3.2 \text{ mA}$	2.7			V
I_{OZL}	Low Level Off-State Output Current (Note 7)	$V_{CC} = \text{Max}, V_O = 0.4 \text{ V}$			–50	μA
I_{OZH}	High Level Off-State Output Current (Note 7)	$V_{CC} = \text{Max}, V_O = 2.4 \text{ V}$			50	μA
I_{OS}	Output Short-Circuit Current (Note 8)	$V_{CC} = 5 \text{ V}, V_O = 0 \text{ V}$	–50		–130	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}, \text{Outputs Open}$		125	210	mA
C_I	Input Capacitance	$V_{CC} = 5.0 \text{ V}, V_I = 2.0 \text{ V}$		8		pF
C_O	Output Capacitance	$V_{CC} = 5.0 \text{ V}, V_O = 2.0 \text{ V}$		8		pF
$C_{I/O}$	I/O Capacitance	$V_{CC} = 5.0 \text{ V}, V_{I/O} = 2.0 \text{ V}$		8		pF

Series D (PAL20L8D, PAL20R4D, PAL20R6D, PAL20R8D) (Continued)

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

Note 3: V_O must not exceed $V_{CC} + 1V$

Note 4: t_{CLK} with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.

t_{CLK} without feedback is derived as $(2t_w)^{-1}$.

Note 5: All typical values are for $V_{CC} = 5.0V$ and $T_A = 25^\circ C$.

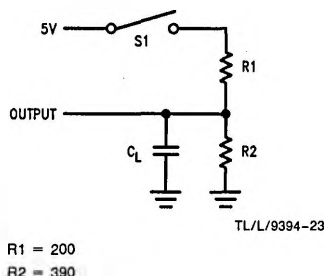
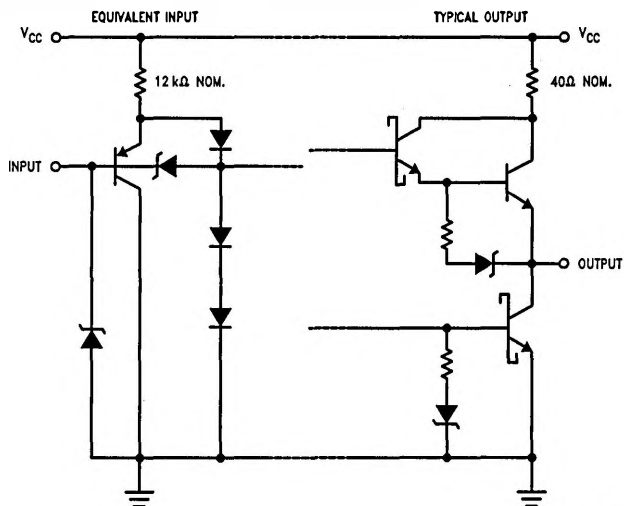
Note 6: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

Note 7: Leakage current for bidirectional I/O pins is the worst case between I_{IL} and I_{OZL} or between I_{IH} and I_{OZH} .

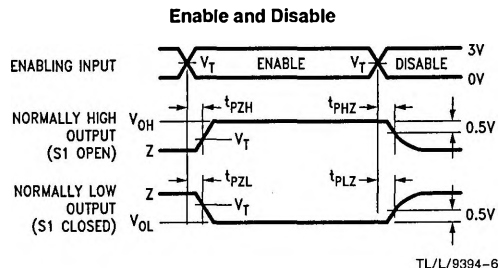
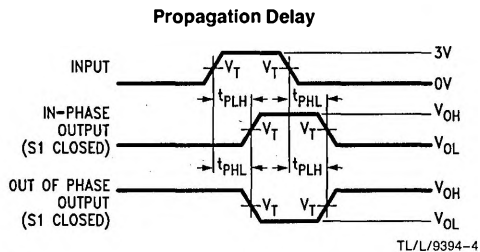
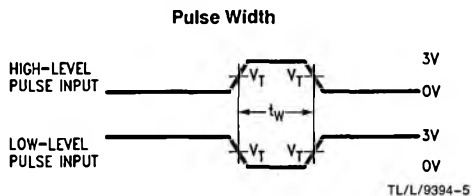
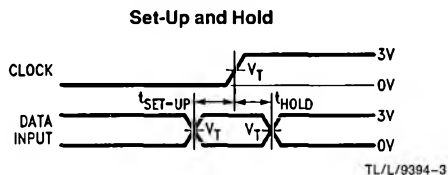
Note 8: To avoid invalid readings in other parameter tests it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Commercial			Units
			Min	Typ	Max	
t_{PD}	Input or Feedback to Combinatorial Output	$C_L = 50 \text{ pF}$, S1 Closed			10	ns
t_{CLK}	Clock to Registered Output or Feedback	$C_L = 50 \text{ pF}$, S1 Closed			8	ns
t_{PZXG}	$\overline{G}$ Pin to Registered Output Enabled	$C_L = 50 \text{ pF}$, Active High: S1 Open, Active Low: S1 Closed			10	ns
t_{PXZG}	$\overline{G}$ Pin to Registered Output Disabled	$C_L = 5 \text{ pF}$, From V_{OH} : S1 Open, From V_{OL} : S1 Closed			10	ns
t_{PZXI}	Input to Combinatorial Output Enabled via Product Term	$C_L = 50 \text{ pF}$, Active High: S1 Open, Active Low: S1 Closed			10	ns
t_{PXZI}	Input to Combinatorial Output Disabled via Product Term	$C_L = 5 \text{ pF}$, From V_{OH} : S1 Open, From V_{OL} : S1 Closed			10	ns
t_{RESET}	Power-Up to Registered Output High				1000	ns

Test Load**Schematic of Inputs and Outputs**

Test Waveforms



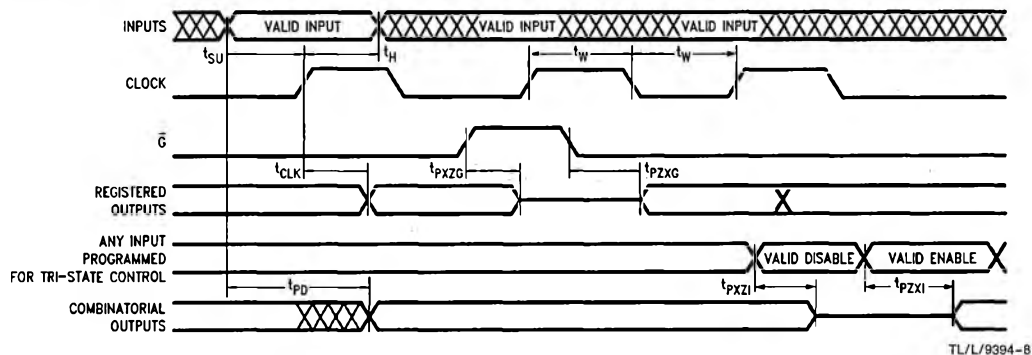
Notes:

$V_T = 1.5V$

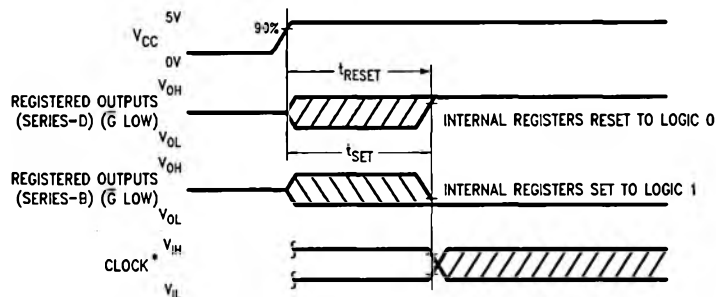
C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Switching Waveforms



Power-Up Set/Reset Waveform



*The clock input should not be switched from low to high until after time t_{RESET} or t_{SET} .

TL/L/9394-9

Functional Description

All of the 24-pin Medium PAL logic arrays consist of 20 complementary input lines and 64 product-term lines with a programmable cell at each intersection (2560 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

For the fuse-link PAL devices (all PAL devices prior to National Series D), an unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. In the National Series D vertical fuse PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed National Series-D PAL device).

The medium PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 20L8, 20R4, 20R6 and 20R8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

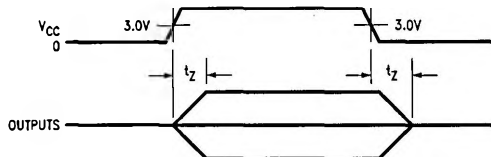
Each combinatorial output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 20L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisfied (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable

($\bar{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series-B Medium PAL devices set all the registers high on power-up (active low outputs assume low logic levels if enabled). Series-D Medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up set or reset, V_{CC} must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the set or reset operation. The clock input should also remain stable until after the power-up set or reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

For the National Series D PAL device, during power-up, all outputs are held in the high-impedance state until DC power supply conditions are met (V_{CC} approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinatorial outputs) or the $\bar{G}$ pin (registered outputs). Whenever V_{CC} goes below 3V (at 25°C), the outputs are disabled as shown in Figure 1 below.



TL/L/9394-25

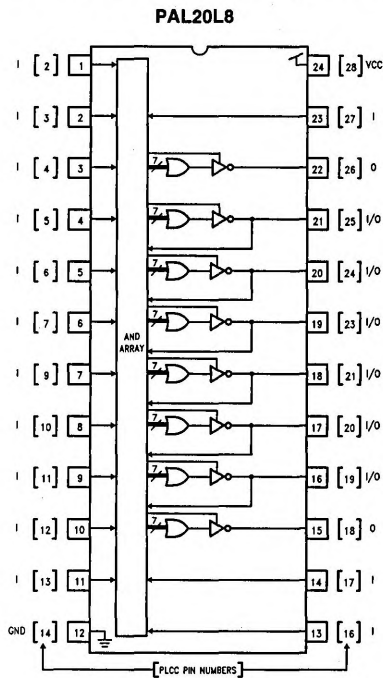
Note: t_z is less than 100 ns.

FIGURE 1. Series-D Power-Up TRI-STATE Waveform

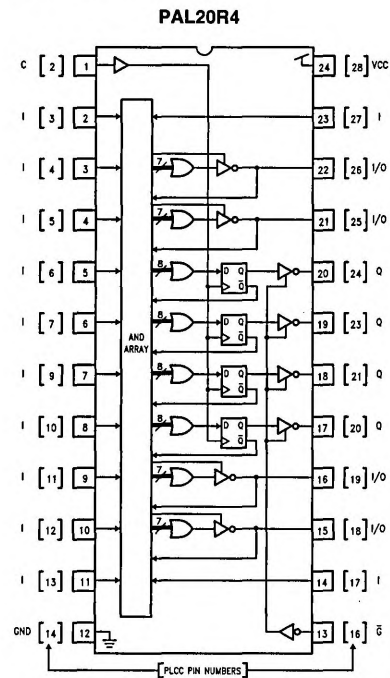
In an unprogrammed National Series D PAL device, no array inputs are connected to any product-term lines. Therefore, all combinatorial outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL} , V_{OH} , or resistively to V_{CC} . However, switching any input not connected to a product term or logic function has no effect on its output logic state.

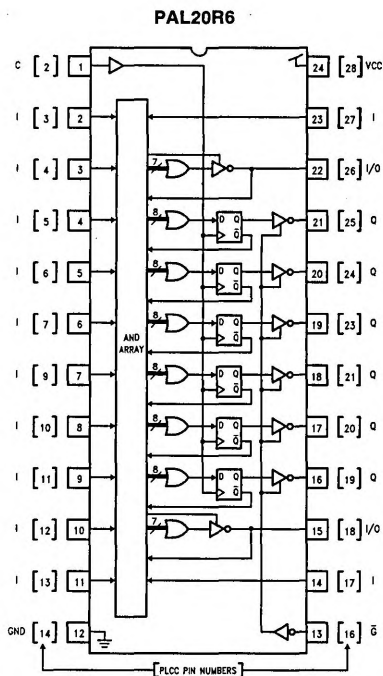
24-Pin Medium PAL Family Block Diagrams—DIP Connections



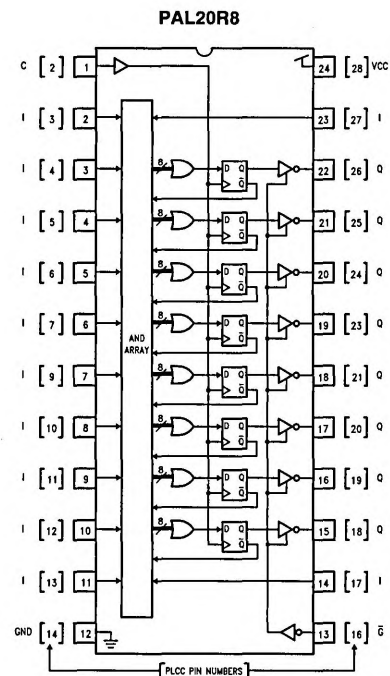
TL/L/9394-10



TL/L/9394-11

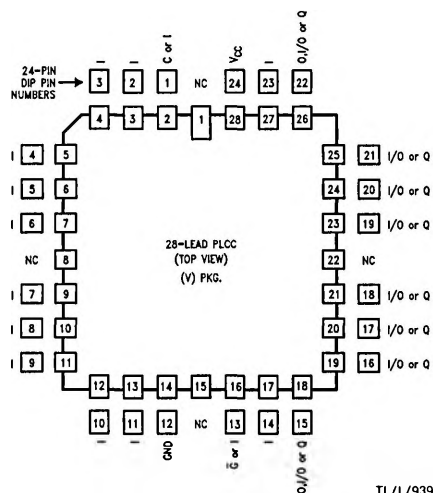


TL/L/9394-12



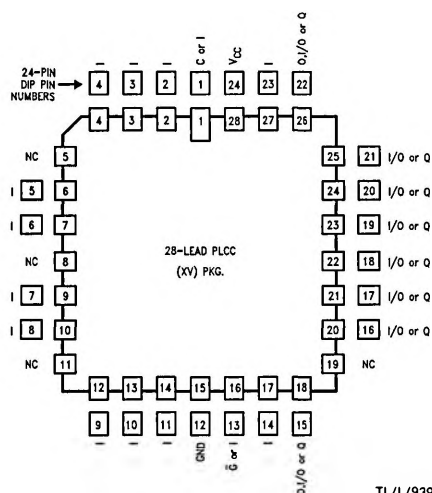
TL/L/9394-13

28-Lead PLCC Connection Conversion Diagram*



TL/L/9394-14

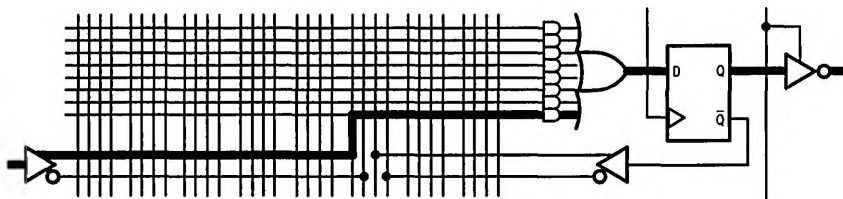
Non-JEDEC PLCC Diagram



TL/L/9394-18

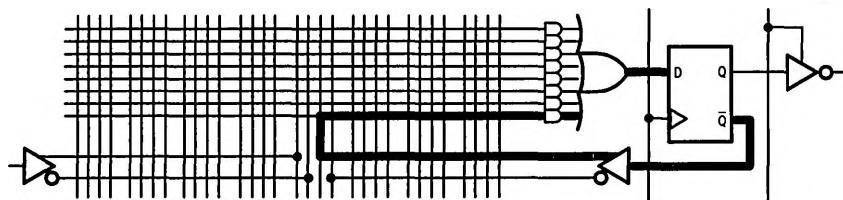
*For availability of old (non-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor.

Typical Registered Logic Function Without Feedback



TL/L/9394-15

Typical Registered Logic Function With Feedback



TL/L/9394-16

Functional Description (Continued)

CLOCK FREQUENCY SPECIFICATION

The clock frequency (f_{CLK}) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e., based only on external inputs), the minimum required cycle period (f_{CLK}^{-1} without feedback) is defined as the greater of the minimum clock period ($t_{W\text{ high}} + t_{W\text{ low}}$) and the minimum "data window" period ($t_{SU} + t_{H}$). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period (f_{CLK}^{-1} with feedback) is defined as $t_{CLK} + t_{SU}$. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

Output Register Preload

This feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility. This feature is available on the Series-B and Series-D devices only.

SERIES-D

For the National Series D PAL devices, the preload function allows the registers to be loaded directly and asynchronously with any desired pattern. These vertical-fuse devices provide two register preload operations:

1. All registers can be reset to the low state (high-level outputs) by applying the elevated control voltage (V_Z) to input pin 2* for time t_D (Figure 2a).
2. Selected registers can be set to the high state (low-level outputs) as follows (Figure 2b):
 - a. All registered outputs are disabled by raising the $\bar{G}$ input pin 1* to V_{IH}
 - b. After time t_D , the selected registered output pins are raised to the elevated control voltage (V_Z) for time t_D to set the corresponding registers.

*Refers to DIP packages only. For equivalent PCC package refer to the 28-pin PCC connection conversion diagram.

SERIES-B

For Series-B devices in the 24-pin Medium PAL family, the preload function allows the registers to be loaded asynchronously from data placed on the output pins. The register preload procedure is as follows and the waveform is shown in Figure 3:

1. Apply V_{CC}
2. Disable the registered outputs by raising pin 13 to V_{IH} .
3. Apply V_{IL} to inputs corresponding to all non-registered outputs.
4. Apply the desired V_{IL}/V_{IH} to the inputs corresponding to registered outputs. (A high input will force the register high and the output low.)
5. Raise the Preload pins (pin 18 and pin 14) to V_{IH} . ($V_{IH} = 11.75V \pm 0.25V$)

6. Apply a clock pulse.

7. Remove V_{IH} from the Preload pins. (The data inputs will return to normal inputs.)

8. Lower pin 13 to V_{IL} to enable the outputs.

Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

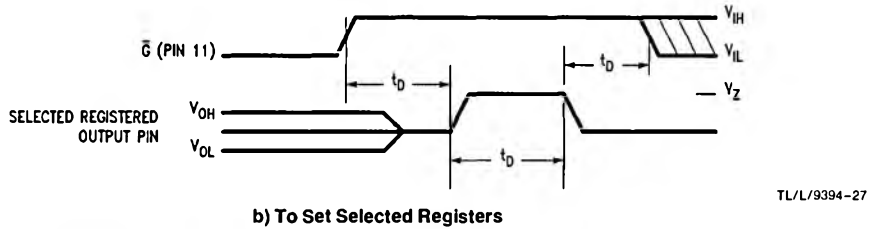
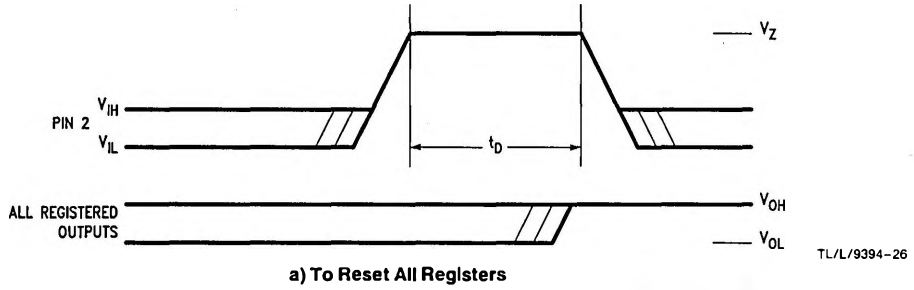
Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLANTM software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

In National Series D PAL devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposite to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the user's design development process looks the same. (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices). The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where ones are located in the map to remove corresponding connections, whereas the algorithm for National Series D PAL products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the same JEDEC map representing the user's desired logic equations produces the same functional results when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National Series D vertical-fuse PAL programming algorithm can be used to program these vertical-fuse devices.

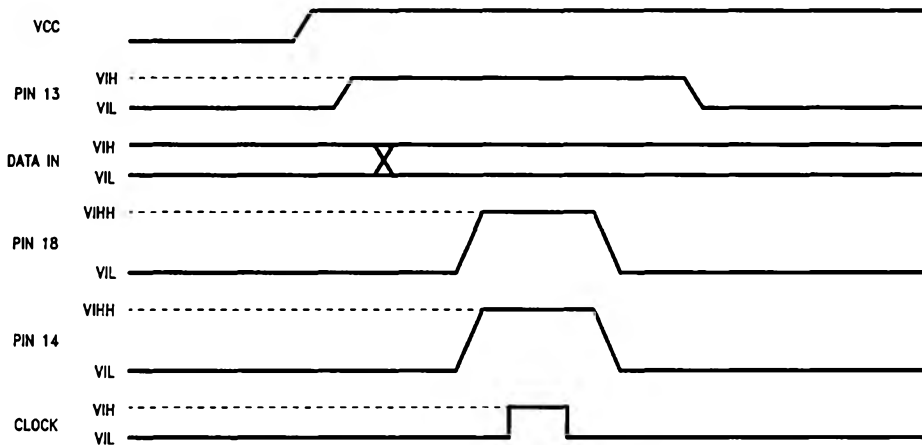
Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Medium PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

Functional Description (Continued)

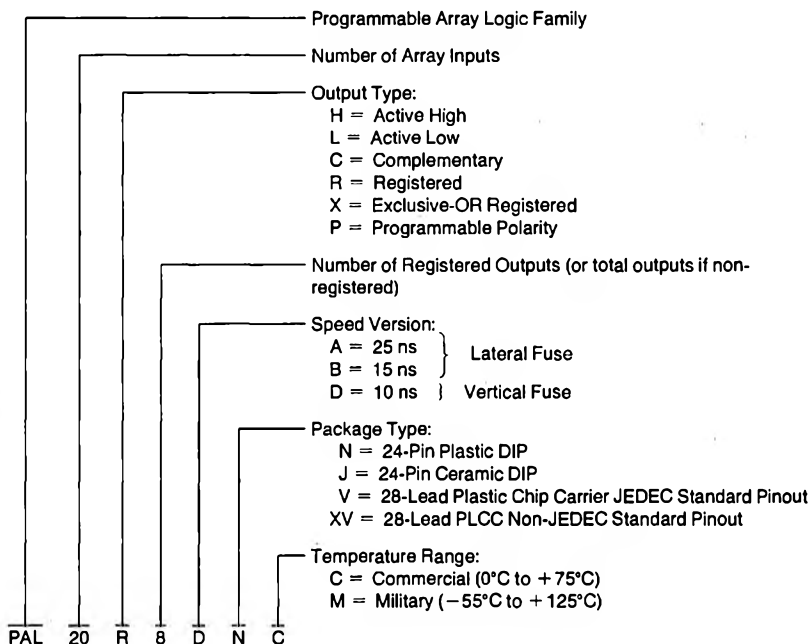


Note: $V_Z = 9.5V$ to $10.0V$, $t_D \text{ min.} = 500 \text{ ns}$

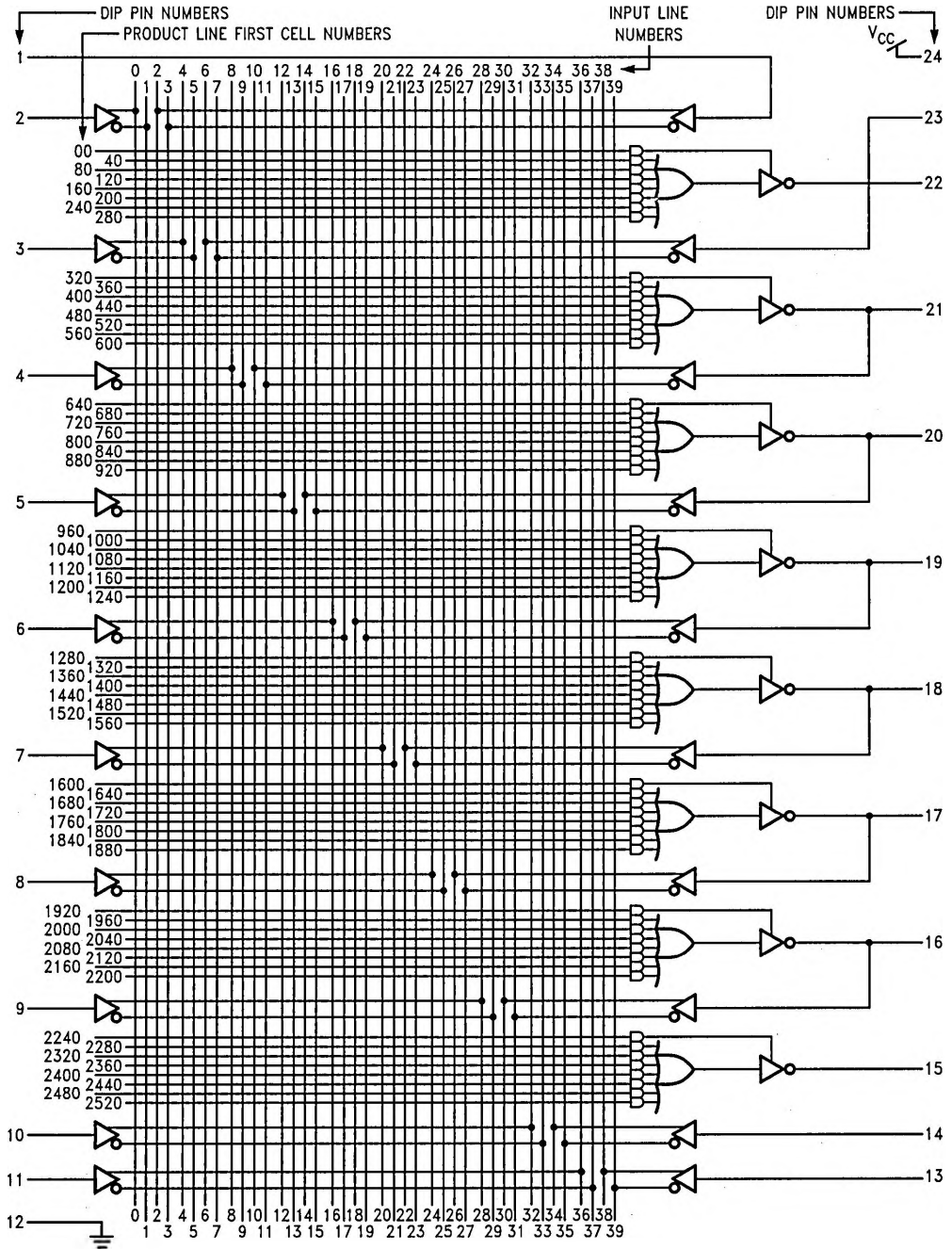
FIGURE 2. Series-D Register Preload Waveforms (Vertical-Fuse Devices)



Ordering Information



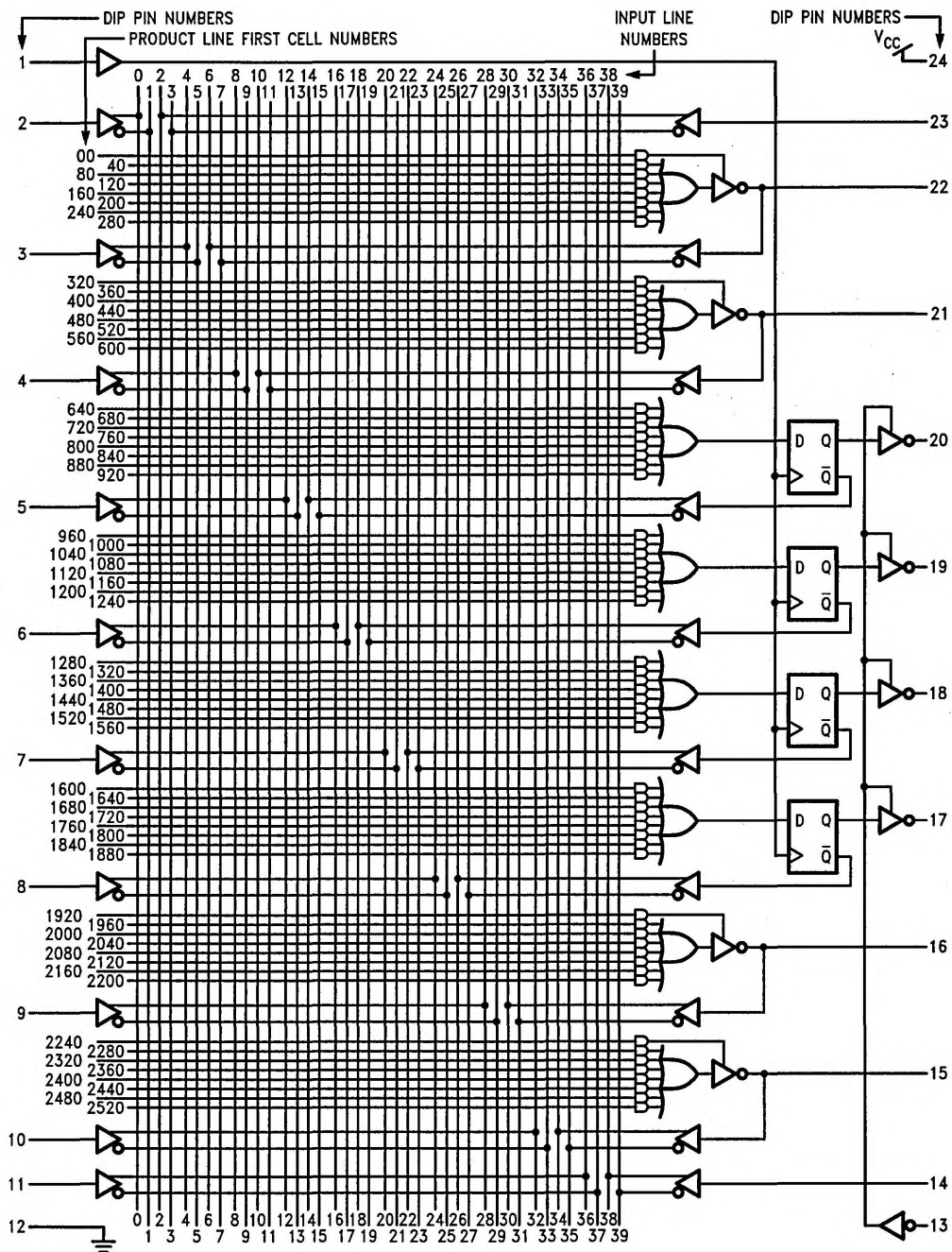
Logic Diagram—PAL20L8



JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

TL/L/9394-19

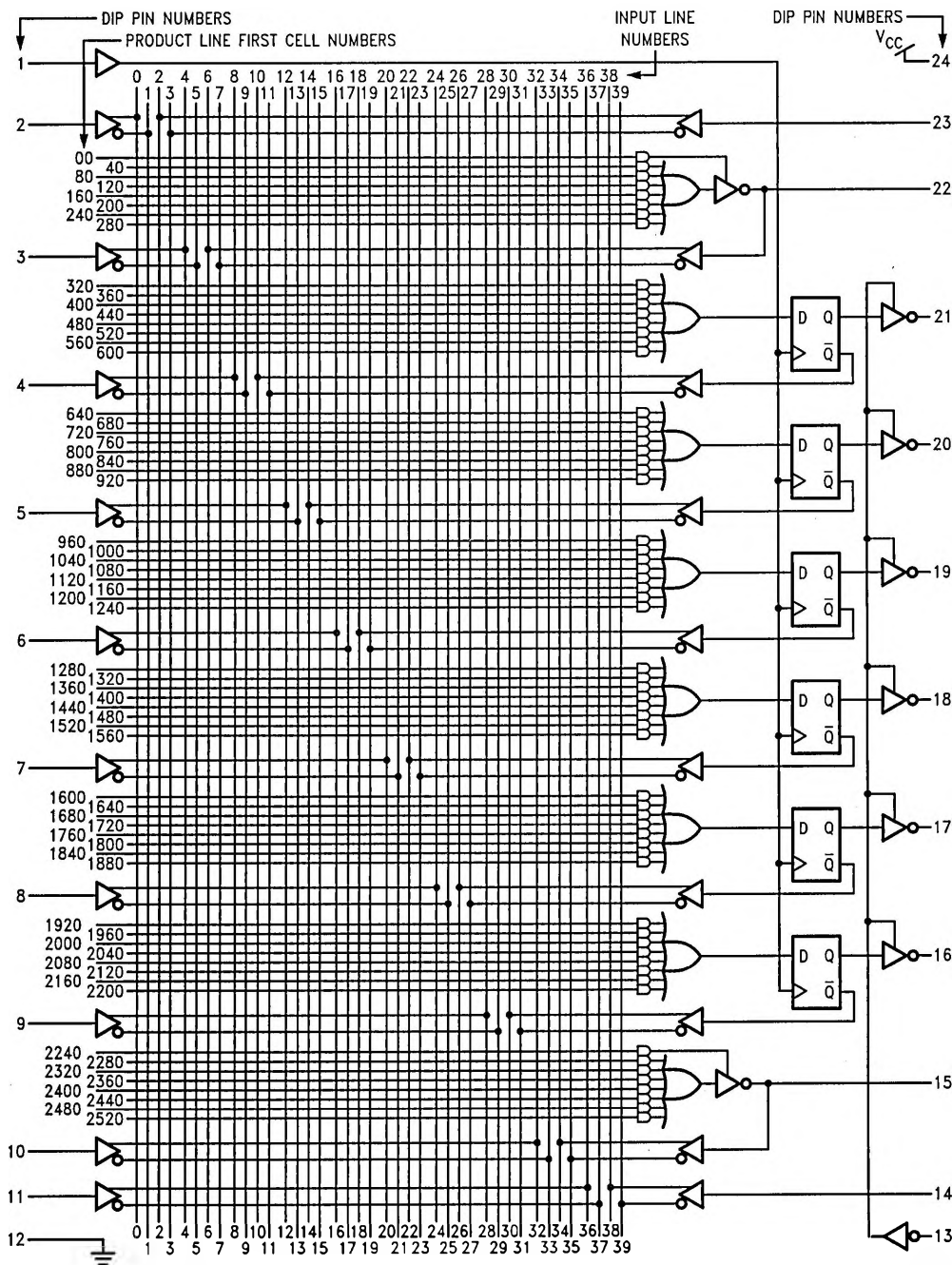
Logic Diagram—PAL20R4



JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

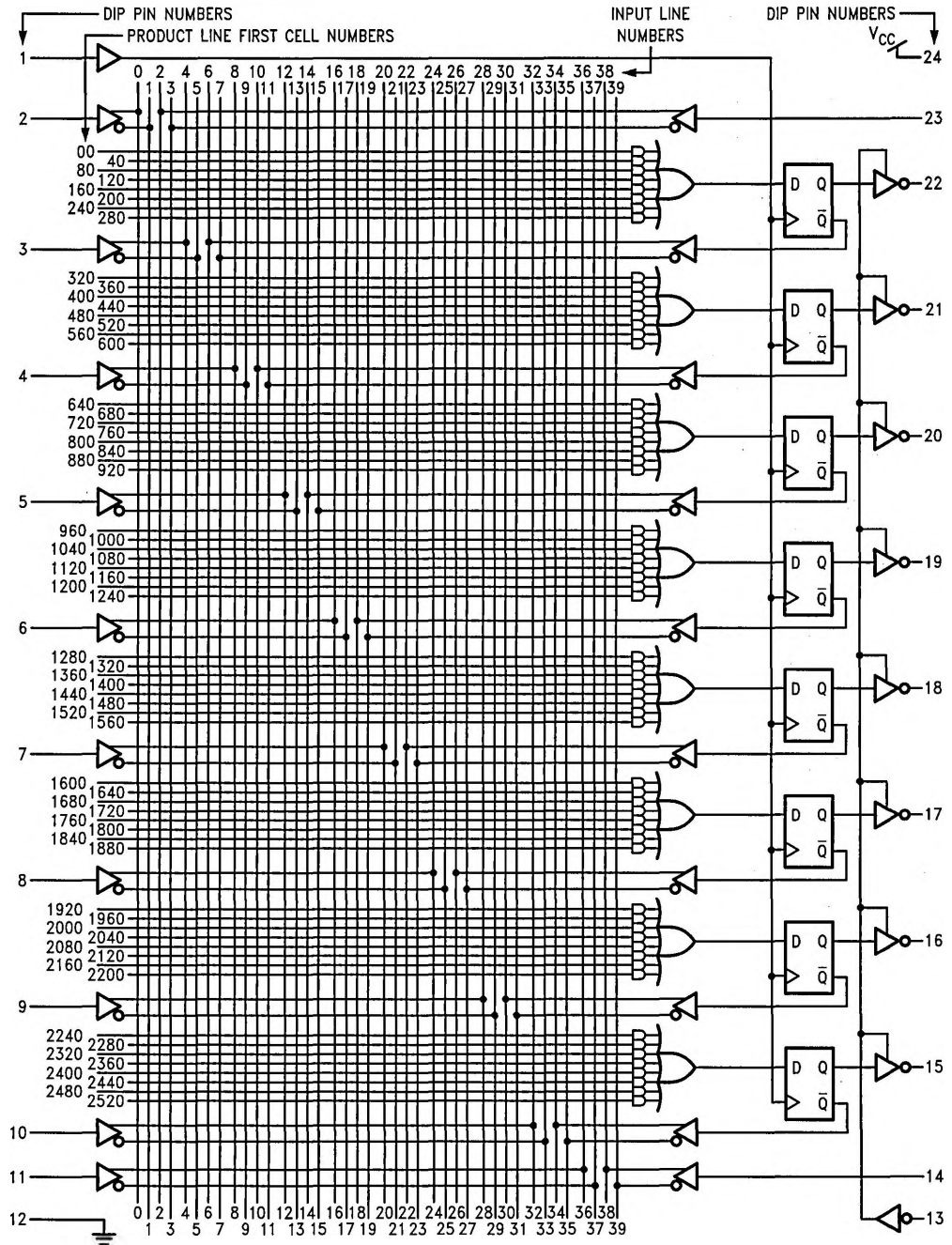
TL/L/9394-20

Logic Diagram—PAL20R6



JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

Logic Diagram—PAL20R8



JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

TL/L/9394-22