National Semiconductor

Programmable Array Logic (PAL®) 24-Pin Small PAL Family

General Description

The 24-pin Small PAL family contains six popular PAL architectures. The devices in the Small PAL family draw only 100 mA maximum supply current as compared to 210 mA in the 24-pin Medium PAL devices. These devices offer speeds as fast as 25 ns maximum propagation delay. National Semiconductor's Schottky TTL process with titanium tungsten fusible links provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fusible links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The Small PAL logic array has between 12 and 20 complementary inputs and up to 10 combinatorial outputs generated by a single programmable AND-gate array with fixed OR-gate connections. The Small PAL family offers a variety of input/output combinations as shown in the Device Types table below. Security fuses can be programmed to prevent direct copying of proprietary logic patterns.

Features

- As fast as 25 ns maximum propagation delay
- User-programmable replacement for TTL logic
- Large variety of JEDEC-compatible programming equipment available
- Fully supported by National PLAN™ development software
- Security fuse prevents direct copying of logic patterns

Device Types

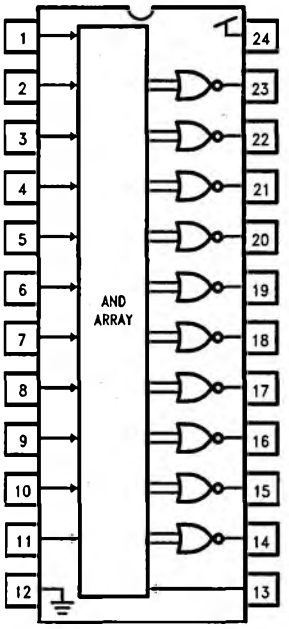
Device Type	Dedicated Inputs	Combinatorial Outputs
PAL12L10	12	10
PAL14L8	14	8
PAL16L6	16	6
PAL18L4	18	4
PAL20L2	20	2
PAL20C1	20	1 Pair

Speed/Power Versions

Series	Example	Commercial		Military	
		t_{PD}	I_{CC}	t_{PD}	I_{CC}
Standard	PAL12L10	40 ns	100 mA	45 ns	100 mA
A	PAL12L10A	25 ns*	100 mA	30 ns*	100 mA

*Except PAL20C1A t_{PD} = 30 ns Commercial, 35 ns Military.

Block Diagram—PAL12L10



TL/L/9997–1

Standard Series (PAL12L10, PAL14L8, PAL16L6, PAL18L4, PAL20L2, PAL20C1)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5 to +7.0V
Input Voltage (Notes 2 and 3)	−1.5 to +5.5V
Off-State Output Voltage (Note 2)	−1.5 to +5.5V
Input Current (Note 2)	−30.0 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55			0		75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Over Recommended Operating Conditions (Note 4)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 5)						0.8	V
V_{IH}	High Level Input Voltage (Note 5)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−0.8	−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.02	−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA			0.3	0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4	3.0		V
			I_{OH} = −3.2 mA	COM				
I_{OS}	Output Short-Circuit Current (Note 6)	V_{CC} = 5V, V_O = 0V			−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

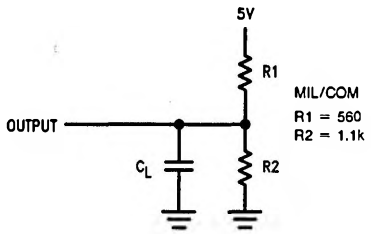
Note 6: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Standard Series (PAL12L10, PAL14L8, PAL16L6, PAL18L4, PAL20L2, PAL20C1) (Continued)

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input to Output	C_L = 50 pF		25	45		25	40	ns

Test Load



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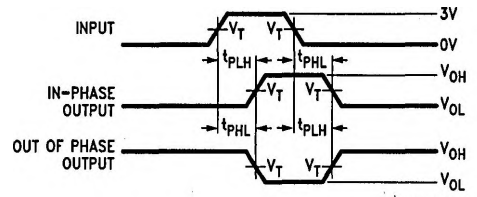
Test Waveform

Propagation Delay



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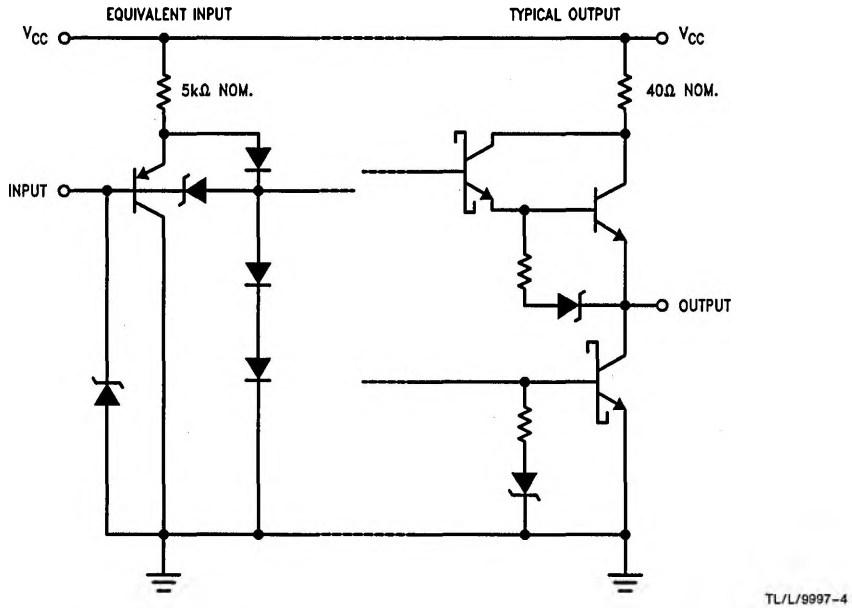
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs



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Series A (PAL12L10A, PAL14L8A, PAL16L6A, PAL18L4A, PAL20L2A, PAL20C1A)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 2)	−0.5 to +7.0V
Input Voltage (Note 2)	−1.5 to +5.5V
Off-State Output Voltage (Note 2)	−1.5 to +5.5V
Input Current (Note 2)	−30.0 mA to +5.0 mA
Output Current (I_{OL})	+100 mA
Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−65°C to +125°C
Junction Temperature	−65°C to +150°C
ESD Tolerance (Note 3)	1500V

C_{ZAP} = 100 pF
R_{ZAP} = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature	−55			0		75	°C
T_C	Operating Case Temperature			125				°C

Electrical Characteristics Over Recommended Operating Conditions (Note 4)

Symbol	Parameter	Test Conditions			Min	Typ	Max	Units
V_{IL}	Low Level Input Voltage (Note 5)						0.8	V
V_{IH}	High Level Input Voltage (Note 5)				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−0.8	−1.5	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.02	−0.25	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					25	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V					100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA			0.3	0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2 mA	MIL	2.4	3.0		V
			I_{OH} = −3.2 mA	COM				
I_{OS}	Output Short-Circuit Current (Note 6)	V_{CC} = 5V, V_O = 0V			−30	−70	−130	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open				60	100	mA

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

Note 2: Some device pins may be raised above these limits during programming operations according to the applicable specification.

Note 3: It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 13 (DIP) are connected directly to the security fuses, and although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged preventing subsequent programming and verification operations.

Note 4: All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 5: These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

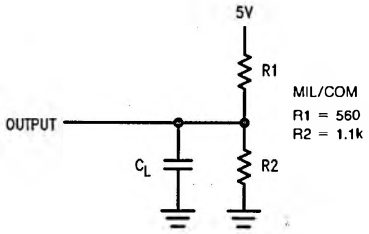
Note 6: To avoid invalid readings in other parameter tests, it is preferable to conduct the I_{OS} test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a high output may raise the chip temperature above normal and permanent damage may result.

Series A (PAL12L10A, PAL14L8A, PAL16L6A, PAL18L4A, PAL20L2A, PAL20C1A) (Continued)

Switching Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions		Military			Commercial			Units
				Min	Typ	Max	Min	Typ	Max	
t_{PD}	Input to Output	C_L = 50 pF	12L10A, 14L8A, 16L6A, 18L4A, 20L2A		15	30		15	25	ns
			20C1A			35			30	ns

Test Load



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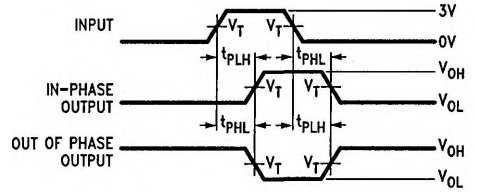
Test Waveform

Propagation Delay



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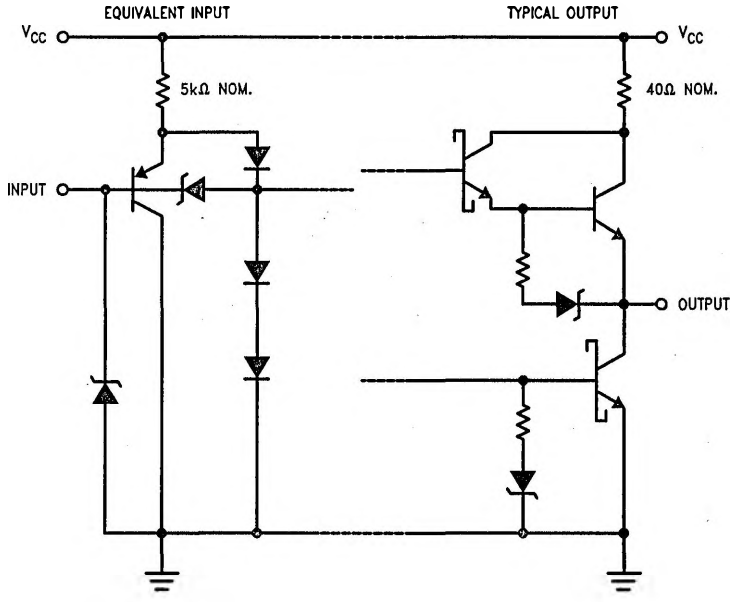
Notes:

V_T = 1.5V

C_L includes probe and jig capacitance.

In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Schematic of Inputs and Outputs



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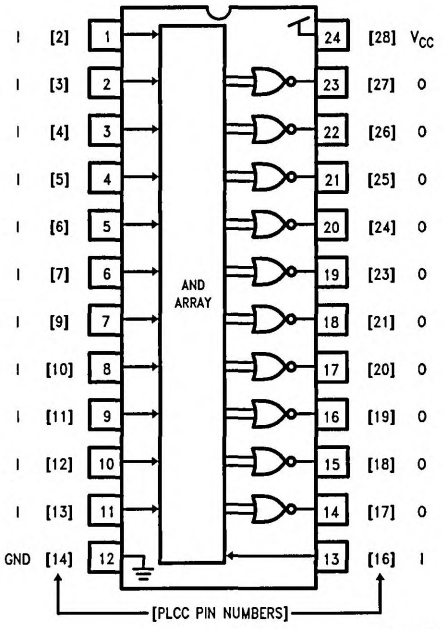
24-Pin Small PAL Family Block Diagrams—DIP Connections

PAL12L10



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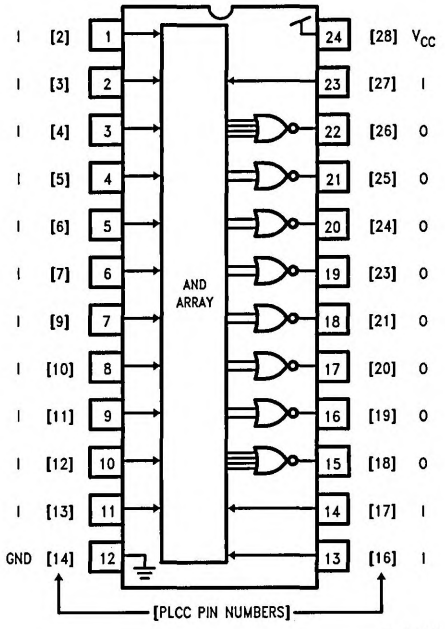
PAL14L8



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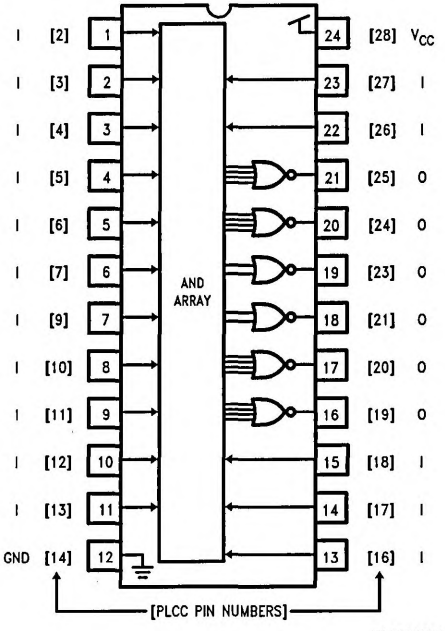
PAL16L6



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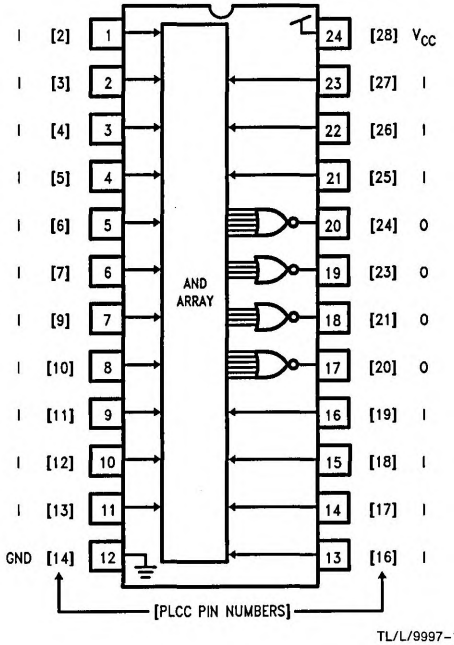
PAL18L4



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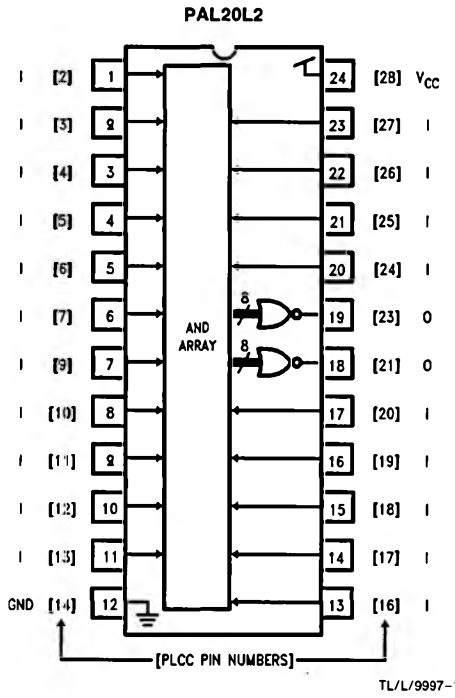
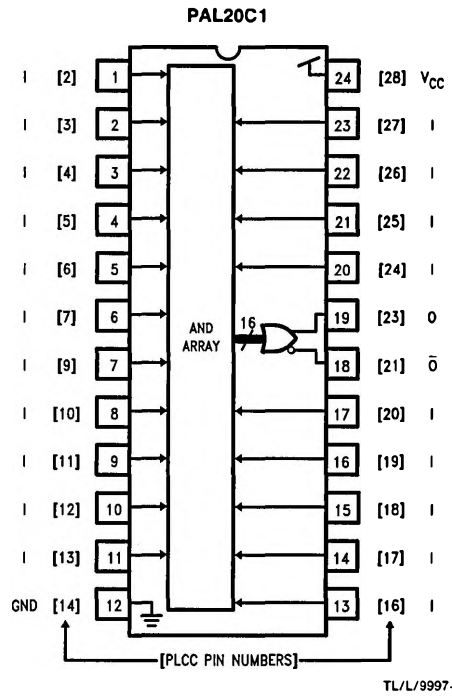
24-Pin Small PAL Family Block Diagrams—DIP Connections (Continued)



TL/L/9997-12



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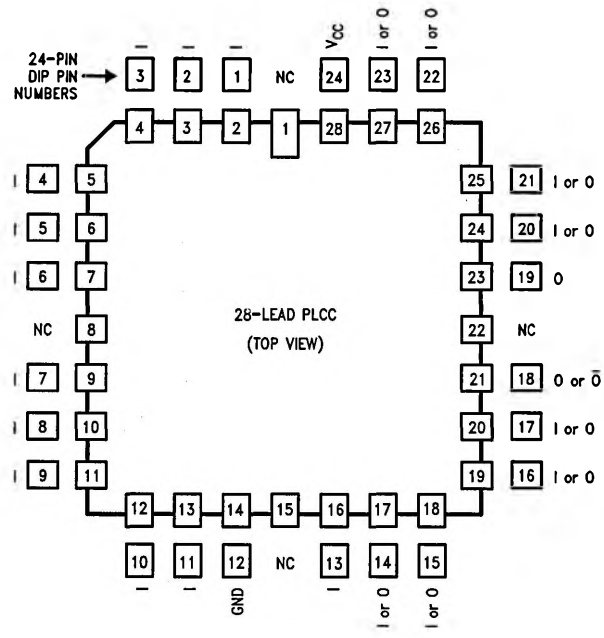
28-Lead PLCC Connection Conversion Diagram



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Note: For availability of old (NON-JEDEC) pinout, please contact your local National Semiconductor sales representative or distributor.

Functional Description

The 24-pin Small PAL logic arrays consist of between 12 and 20 complementary input lines and either 16 or 20 product-term lines with a programmable fuse link at each intersection (up to 720 fuses). The family consists of six device types with different numbers of combinatorial outputs. The 24-pin Small PAL Family Block Diagrams show the number of product terms allocated to each output for each device. All product terms allocated to each output connect into an OR-gate to produce the sum-of-products output logic function.

An unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses) are in the high logic state. Therefore, if both the true and complement of at least one array input is left connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed device). Conversely, if all fuses on a product term were programmed, the product term and the resulting logic function would be held in the high state.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, V_{OL}, V_{OH}, or resistively to V_{CC}. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

Security Fuse

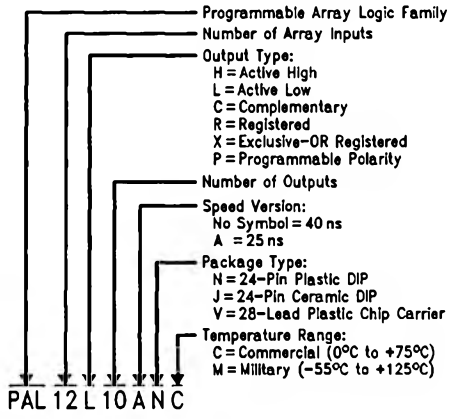
Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses.

Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 24-pin Small PAL family are provided for direct map editing and diagnostic purposes. Contact your local National Semiconductor sales representative or distributor for a list of current software and programming support tools available for these devices. Contact the National Semiconductor Programmable Device Support Department if detailed specifications of PAL programming algorithms are needed.

Ordering Information



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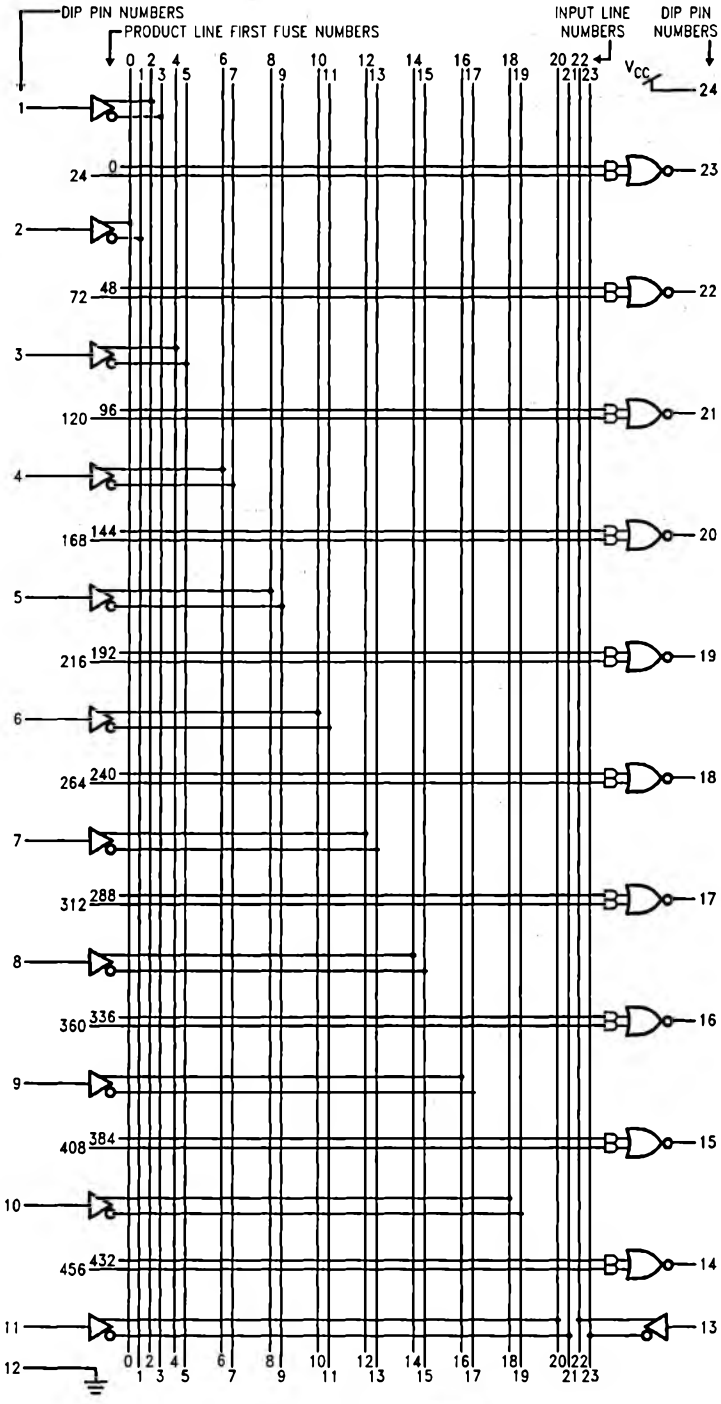
Logic Diagram PAL12L10



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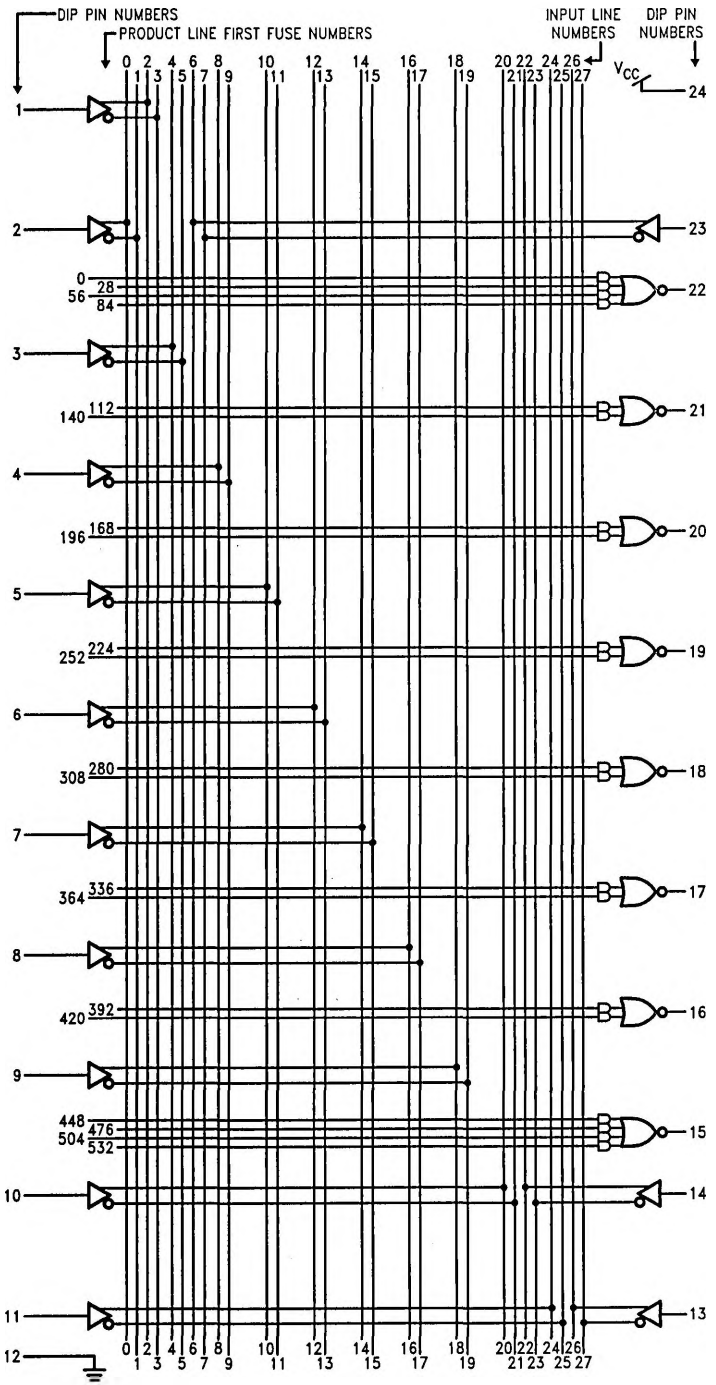
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL14L8



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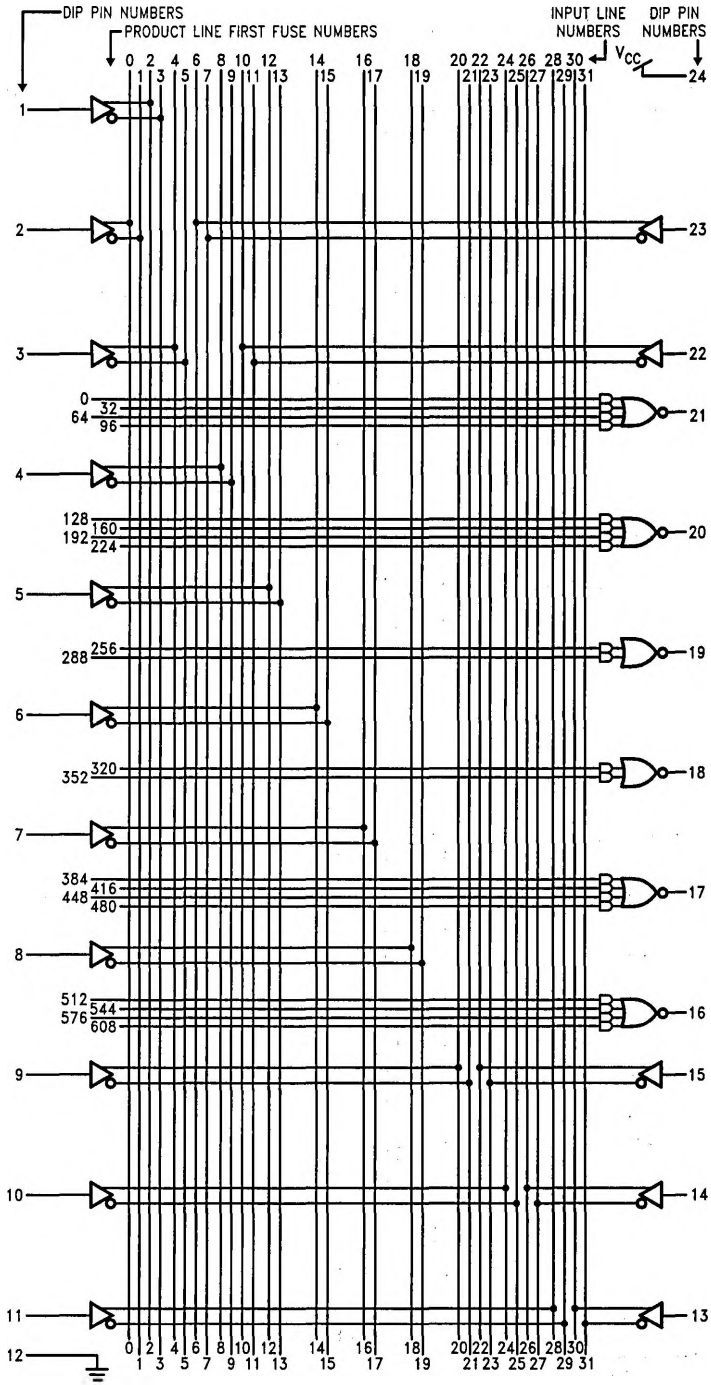
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL16L6



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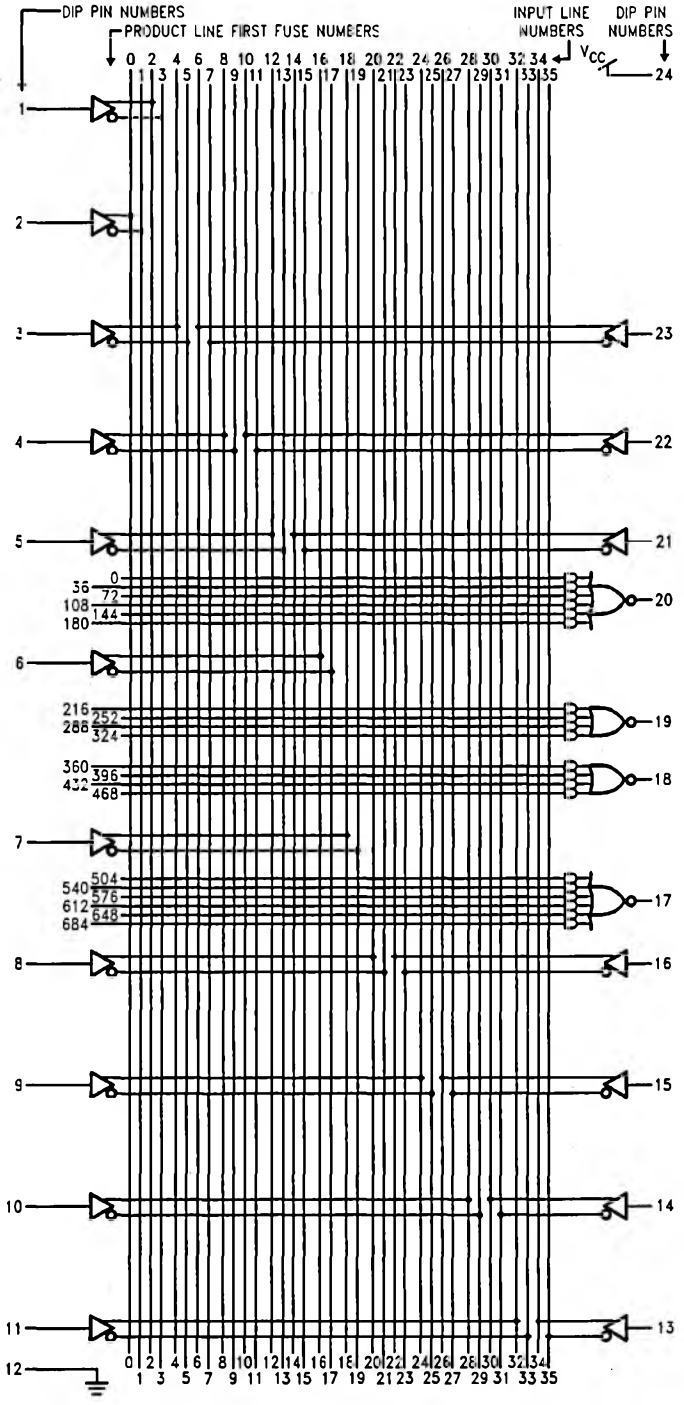
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL18L4



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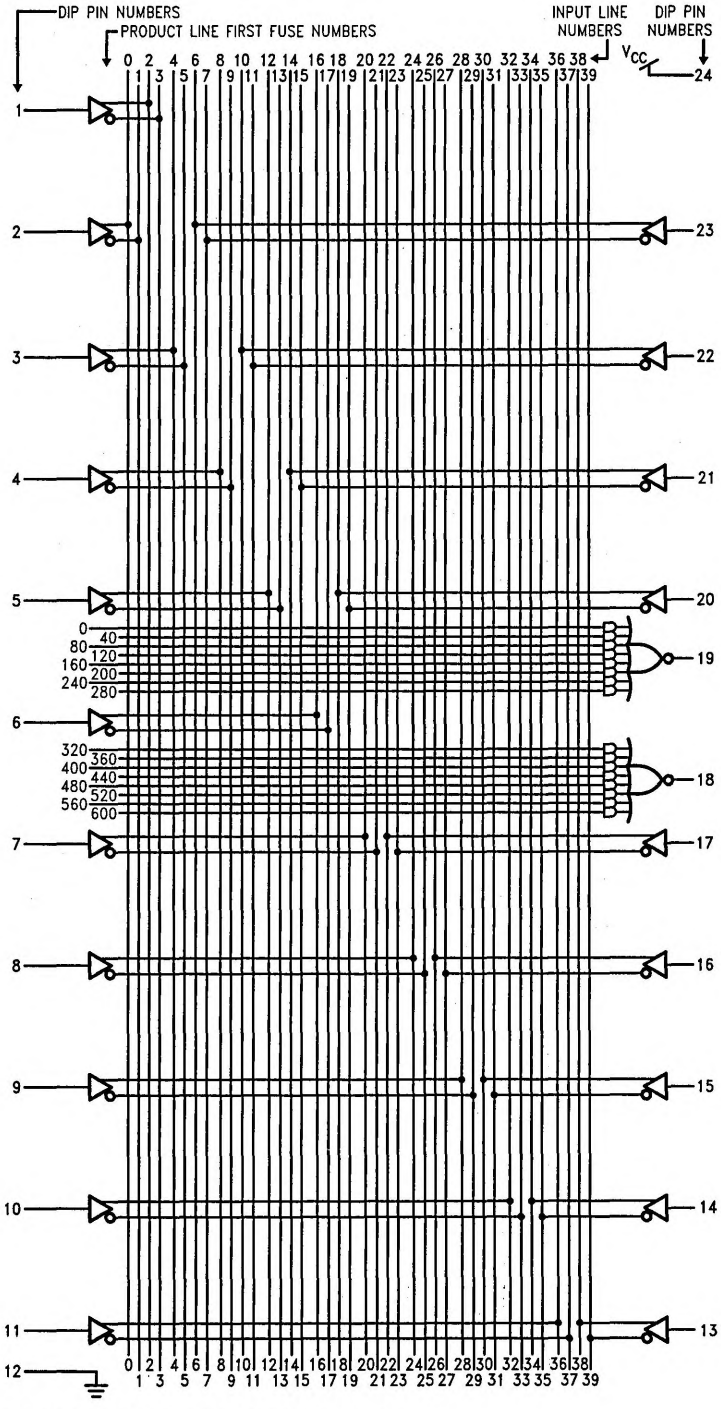
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL20L2



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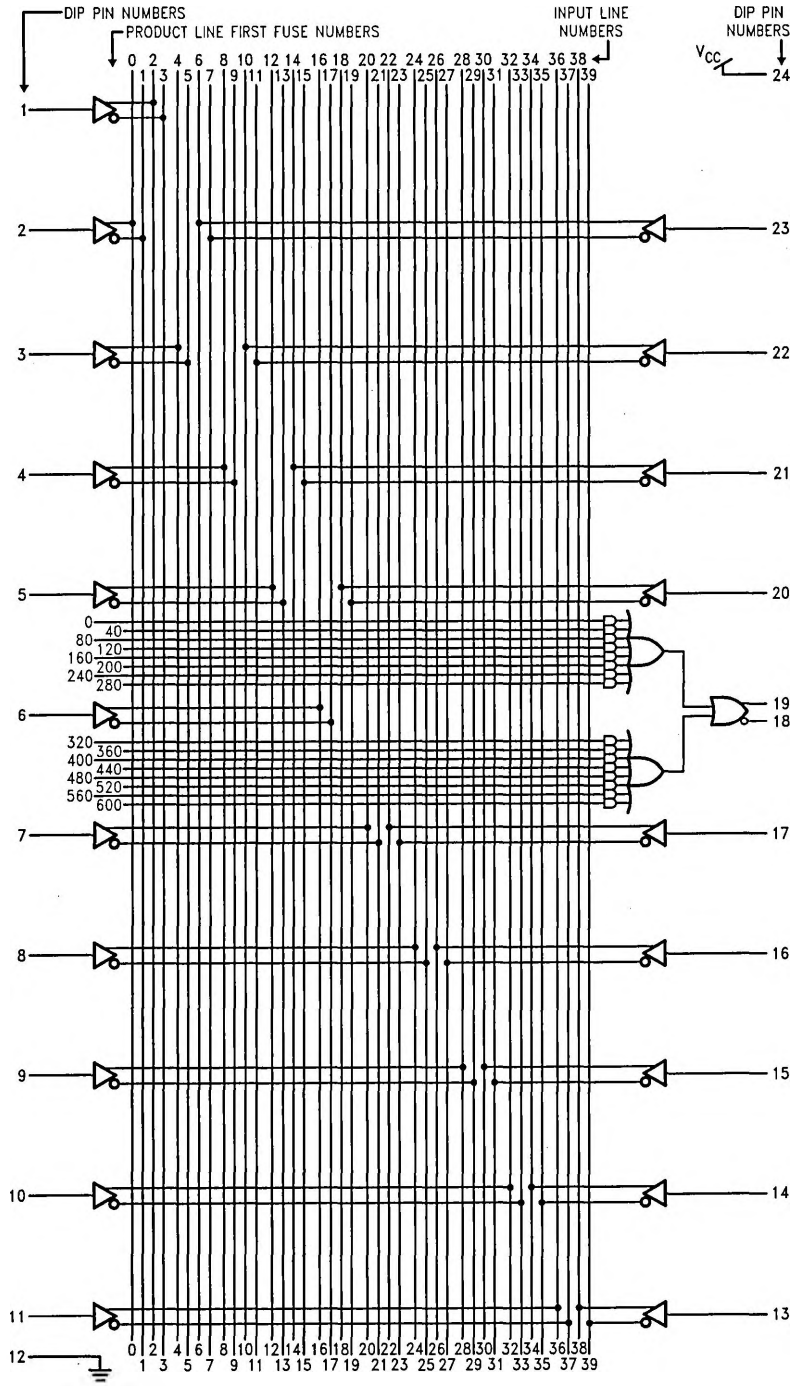
Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL20C1



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Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.