National Semiconductor

# Programmable Array Logic (PAL®) 20-Pin Medium PAL Family

## General Description

The 20-pin Medium PAL family contains four of the most popular PAL architectures used in industry. National Semiconductor's advanced Schottky TTL process with titanium tungsten fusible links is used in manufacturing the standard, Series-A, Series-A2, Series-B and Series-B2 devices. Series-D devices are manufactured using National Semiconductor's isoplanar "FAST-Z" TTL process with highly reliable "vertical-fuse" programmable cells. Vertical fuses are implemented using avalanche-induced migration ("AIM") technology offering very high programming yields and is an extension of National's FAST logic family. The 20-pin Medium PAL Family provides high-speed user-programmable replacements for conventional SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming the programmable cells to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products. A large variety of programming units and software makes design development and functional testing of PAL devices quick and easy.

The PAL logic array has a total of 16 complementary input pairs and 8 outputs generated by a single programmable AND-gate array with fixed OR-gate connections. Device outputs are either taken directly from the AND-OR functions (combinatorial) or passed through D-type flip-flops (registered). Registers allow the PAL device to implement sequential logic circuits. TRI-STATE® outputs facilitate busing and provide bidirectional I/O capability. The medium PAL family offers a variety of combinatorial and registered output mixtures, as shown in the Device Types table below.

On power-up, Series-D devices reset all registers to simplify sequential circuit design and testing. For these devices, direct register preload is also provided to facilitate device testing. Security fuses can be programmed to prevent direct copying of proprietery logic patterns in all the family devices.

## Features

- As fast as 7 ns maximum propagation delay (combinatorial)
- User-programmable replacement for TTL logic
- High programming yield and reliability of vertical-fuse technology for Series-D/-7 products. (Programming equipment with certified vertical-fuse algorithm required.)
- Extension of FAST product line
- Large variety of JEDEC-compatible programming equipment and design development software available
- Fully supported by National PLAN™ development software
- Power-up reset for registered outputs
- Register preload facilitates device testing
- Security fuse prevents direct copying of logic patterns

## Device Types

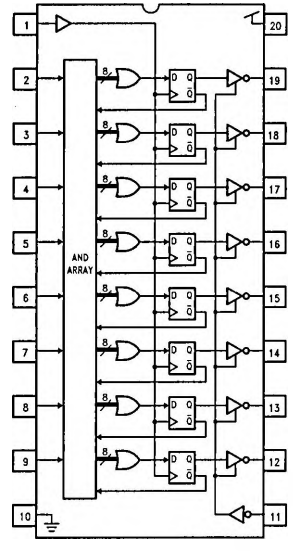
| Device Type | Dedicated Inputs | Registered Outputs (with Feedback) | Combinatorial | |
|---|---|---|---|---|
| | | | I/Os | Outputs |
| PAL16L8 | 10 | — | 6 | 2 |
| PAL16R4 | 8 | 4 | 4 | — |
| PAL16R6 | 8 | 6 | 2 | — |
| PAL16R8 | 8 | 8 | — | — |

## Speed/Power Versions

| Series | Example | Commercial | | Military | |
|---|---|---|---|---|---|
| | | $t_{PD}$ | $I_{CC}$ | $t_{PD}$ | $I_{CC}$ |
| Standard | PAL16L8 | 35 ns | 180 mA | 45 ns | 180 mA |
| A | PAL16L8A | 25 ns | 180 mA | 30 ns | 180 mA |
| A2 | PAL16L8A2 | 35 ns | 90 mA | 50 ns | 90 mA |
| B | PAL16L8B | 15 ns | 180 mA | 20 ns | 180 mA |
| B2 | PAL16L8B2 | 25 ns | 90 mA* | 30 ns | 90 mA* |
| D | PAL16L8D | 10 ns | 180 mA | | |
| -7 | PAL16L8-7 | 7 ns | 180 mA | | |

*For the registered devices $I_{CC}$ = 100 mA.

## Block Diagram—PAL16R8




TL/L/9391-1

## Standard Series (PAL16L8, PAL16R4, PAL16R6, PAL16R8)

### Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Notes 2 and 3) | −1.5V to +5.5V |
| Off-State Output Voltage (Note 2) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | 100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD | 1500V |

### Recommended Operating Conditions

| Symbol | Parameter | | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | −55 | | | 0 | | 75 | °C |
| $T_C$ | Operating Case Temperature | | | | 125 | | | | °C |
| $t_W$ | Clock Pulse Width | Low | 25 | | | 25 | | | ns |
| | | High | 25 | | | 25 | | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 45 | | | 35 | | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −15 | | 0 | −15 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 12.2 | | | 16.6 | MHz |
| | | Without Feedback | | | 20 | | | 20 | MHz |

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | | −0.8 | −1.5 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.02 | −0.25 | mA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 12 mA | MIL | | 0.3 | 0.5 | V |
| | | | $I_{OL}$ = 24 mA | COM | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = −2 mA | MIL | 2.4 | 2.9 | | V |
| | | | $I_{OH}$ = −3.2 mA | COM | | | | |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 0.4V | | | | −100 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 2.4V | | | | 100 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | | | 120 | 180 | mA |

## Standard Series (PAL16L8, PAL16R4, PAL16R6, PAL16R8) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(2t_W)^{-1}$.

**Note 5:** All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

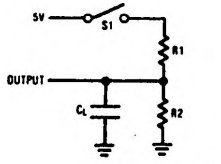
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 25 | 45 | | 25 | 35 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 25 | 45 | | 25 | 35 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 25 | 45 | | 25 | 35 | ns |

## Test Load

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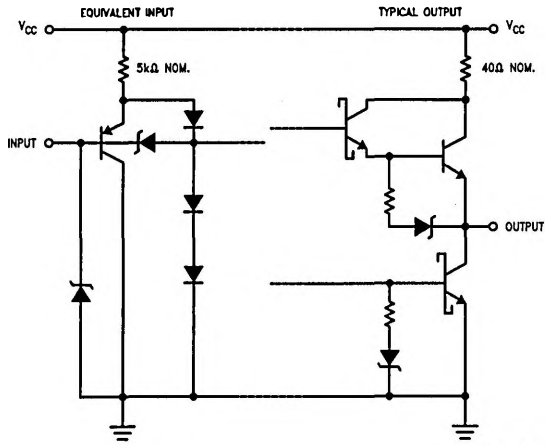
| MIL | COM'L |
|---|---|
| R1 = 390 | R1 = 200 |
| R2 = 750 | R2 = 390 |

## Schematic of Inputs and Outputs

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## Series-A (PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A)

### Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Notes 2 and 3) | −1.5V to +5.5V |
| Off-State Output Voltage (Note 2) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | 100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD | 1500V |

### Recommended Operating Conditions

| Symbol | Parameter | | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | −55 | | | 0 | | 75 | °C |
| $T_C$ | Operating Case Temperature | | | | 125 | | | | °C |
| $t_W$ | Clock Pulse Width | Low | 20 | 10 | | 15 | 10 | | ns |
| | | High | 20 | 10 | | 15 | 10 | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 30 | 16 | | 25 | 16 | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −10 | | 0 | −10 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 20 | | | 25 | MHz |
| | | Without Feedback | | | 25 | | | 33.3 | MHz |

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | | −0.8 | −1.5 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.02 | −0.25 | mA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 12 mA | MIL | | 0.3 | 0.5 | V |
| | | | $I_{OL}$ = 24 mA | COM | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = −2 mA | MIL | 2.4 | 2.9 | | V |
| | | | $I_{OH}$ = −3.2 mA | COM | | | | |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 0.4V | | | | −100 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 2.4V | | | | 100 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | | | 120 | 180 | mA |

## Series-A (PAL16L8A, PAL16R4A, PAL16R6A, PAL16R8A) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(2t_W)^{-1}$.

**Note 5:** All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

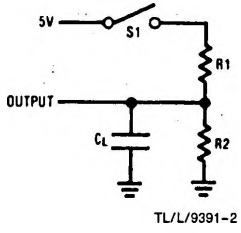
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 15 | 30 | | 15 | 25 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 10 | 20 | | 10 | 15 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 10 | 25 | | 10 | 20 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 11 | 25 | | 11 | 20 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 10 | 30 | | 10 | 25 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 13 | 30 | | 13 | 25 | ns |

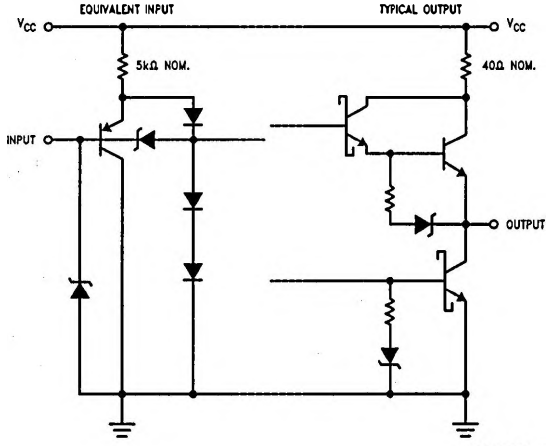
## Test Load




TL/L/9391-2

| MIL | COM'L |
|---|---|
| R1 = 390 | R1 = 200 |
| R2 = 750 | R2 = 390 |

## Schematic of Inputs and Outputs

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## Series-A2 (PAL16L8A2, PAL16R4A2, PAL16R6A2, PAL16R8A2)

### Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Notes 2 and 3) | −1.5V to +5.5V |
| Off-State Output Voltage (Note 2) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | 100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD | 1500V |

### Recommended Operating Conditions

| Symbol | Parameter | | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | −55 | | 125 | 0 | | 75 | °C |
| $t_W$ | Clock Pulse Width | Low | 25 | 10 | | 25 | 10 | | ns |
| | | High | 25 | 10 | | 25 | 10 | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 50 | 25 | | 35 | 25 | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −15 | | 0 | −15 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 13.3 | | | 16.7 | MHz |
| | | Without Feedback | | | 20 | | | 20 | MHz |

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | | −0.8 | −1.5 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.02 | −0.25 | mA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 12 mA | MIL | | 0.3 | 0.5 | V |
| | | | $I_{OL}$ = 24 mA | COM | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = −2 mA | MIL | 2.4 | 2.9 | | V |
| | | | $I_{OH}$ = −3.2 mA | COM | | | | |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 0.4V | | | | −100 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 2.4V | | | | 100 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | | | 70 | 90 | mA |

## Series-A2 (PAL16L8A2, PAL16R4A2, PAL16R6A2, PAL16R8A2) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(2t_W)^{-1}$.

**Note 5:** All typical values are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

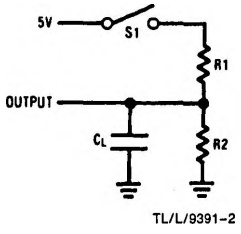
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 25 | 50 | | 25 | 35 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 15 | 25 | | 15 | 25 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 25 | 45 | | 25 | 35 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 25 | 45 | | 25 | 35 | ns |

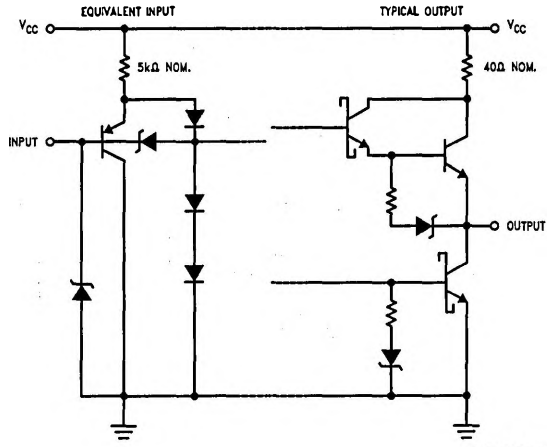
## Test Load




TL/L/9391-2

| MIL | COM'L |
|---|---|
| R1 = 390 | R1 = 200 |
| R2 = 750 | R2 = 390 |

## Schematic of Inputs and Outputs




TL/L/9391-7

## Series-B (PAL16L8B, PAL16R4B, PAL16R6B, PAL16R8B)

### Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Notes 2 and 3) | −1.5V to +5.5V |
| Off-State Output Voltage (Note 2) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | 100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD | 1000V |

### Recommended Operating Conditions

| Symbol | Parameter | | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | −55 | | | 0 | | 75 | °C |
| $T_C$ | Operating Case Temperature | | | | 125 | | | | °C |
| $t_W$ | Clock Pulse Width | Low | 12 | 5 | | 10 | 5 | | ns |
| | | High | 12 | 5 | | 10 | 5 | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 20 | 10 | | 15 | 10 | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −5 | | 0 | −5 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 28.6 | | | 40 | MHz |
| | | Without Feedback | | | 41.7 | | | 50 | MHz |

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | | −0.8 | −1.5 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.02 | −0.25 | mA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 12 mA | MIL | | 0.3 | 0.5 | V |
| | | | $I_{OL}$ = 24 mA | COM | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = −2 mA | MIL | 2.4 | 3.4 | | V |
| | | | $I_{OH}$ = −3.2 mA | COM | | | | |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 0.4V | | | | −100 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 2.4V | | | | 100 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | | | 120 | 180 | mA |

## Series-B (PAL16L8B, PAL16R4B, PAL16R6B, PAL16R8B) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(t_{WLOW} + t_{WHIGH})^{-1}$.

**Note 5:** All typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

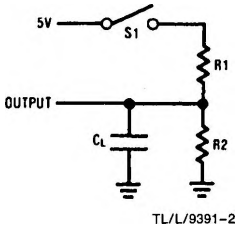
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 11 | 20 | | 11 | 15 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 8 | 15 | | 8 | 12 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 10 | 20 | | 10 | 15 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 10 | 20 | | 10 | 15 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 11 | 20 | | 11 | 15 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 11 | 20 | | 11 | 15 | ns |

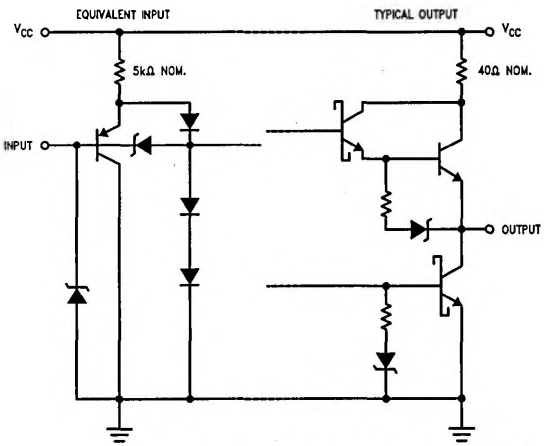
## Test Load




TL/L/9391-2

| MIL | COM'L |
|---|---|
| R1 = 390 | R1 = 200 |
| R2 = 750 | R2 = 390 |

## Schematic of Inputs and Outputs




TL/L/9391-7

## Series-B2 (PAL16L8B2, PAL16R4B2, PAL16R6B2, PAL16R8B2)

### Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Note 2) | −1.5V to +5.5V |
| Off-State Output Voltage (Note 2) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | 100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD Tolerance (Note 3) | 2000V |

$C_{ZAP}$ = 100 pF
$R_{ZAP}$ = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

### Recommended Operating Conditions

| Symbol | Parameter | | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | −55 | | 125 | 0 | | 75 | °C |
| $t_W$ | Clock Pulse Width | Low | 15 | 8 | | 10 | 8 | | ns |
| | | High | 20 | 10 | | 15 | 10 | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 25 | 11 | | 20 | 11 | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −10 | | 0 | −10 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 22.2 | | | 28.6 | MHz |
| | | Without Feedback | | | 28.6 | | | 40 | MHz |

### Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | | −0.8 | −1.5 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | | −0.02 | −0.25 | mA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min | $I_{OL}$ = 12 mA | MIL | | 0.3 | 0.5 | V |
| | | | $I_{OL}$ = 24 mA | COM | | | | |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min | $I_{OH}$ = −2 mA | MIL | 2.4 | 3.4 | | V |
| | | | $I_{OH}$ = −3.2 mA | COM | | | | |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 0.4V | | | | −100 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max | $V_O$ = 2.4V | | | | 100 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | | | −30 | −70 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | 16L8B2 | | | 60 | 90 | mA |
| | | | 16R4B2, 16R6B2, 16R8B2 | | | 70 | 100 | |

## Series-B2 (PAL16L8B2, PAL16R4B2, PAL16R6B2, PAL16R8B2) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** It is recommended that precautions be taken to minimize electrostatic discharge when handling and testing this product. Pins 1 and 11 are connected directly to the security fuses, and, although the input circuitry can withstand the specified ESD conditions, the security fuses may be damaged, preventing subsequent programming and verification operations.

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(t_{WLOW} + t_{WHIGH})^{-1}$.

**Note 5:** All typical values are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

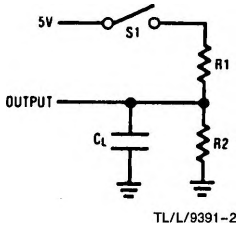
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 sec. each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Military | | | Commercial | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 15 | 30 | | 15 | 25 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 10 | 20 | | 10 | 15 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 15 | 25 | | 15 | 20 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 11 | 25 | | 11 | 20 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 10 | 30 | | 10 | 25 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 13 | 30 | | 13 | 25 | ns |

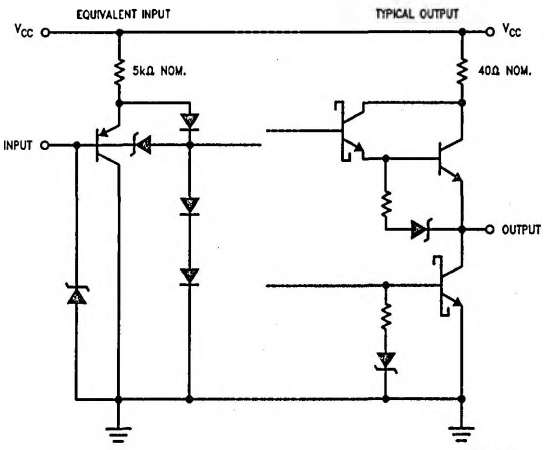
## Test Load




TL/L/9391-2

| MIL | COM'L |
|---|---|
| R1 = 390 | R1 = 200 |
| R2 = 750 | R2 = 390 |

## Schematic of Inputs and Outputs




TL/L/9391-7

## Series-D (PAL16L8D, PAL16R4D, PAL16R6D, PAL16R8D)

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Note 2) | −1.5V to +7.0V |
| Off-State Output Voltage ($V_O$) (Notes 2 & 3) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | +100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD Tolerance | 2000V |

$C_{ZAP}$ = 100 pF
$R_{ZAP}$ = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

## Recommended Operating Conditions

| Symbol | Parameter | | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | 0 | 25 | 75 | °C |
| $t_W$ | Clock Pulse Width | Low | 7 | 3.5 | | ns |
| | | High | 7 | 2 | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 10 | 5.5 | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | −3.7 | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 55.5 | MHz |
| | | Without Feedback | | | 71 | MHz |
| $V_Z$ | Register Preload Control Voltage | | 9.5 | 9.75 | 10.0 | V |

## Electrical Characteristics Over Recommended Operating Conditions (Note 5)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 6) | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 6) | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | −0.8 | −1.2 | V |
| $I_{IL}$ | Low Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 0.4V | | −60 | −250 | μA |
| $I_{IH}$ | High Level Input Current (Note 7) | $V_{CC}$ = Max, $V_I$ = 2.4V | | 0 | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | 20 | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = 24 mA | | 0.3 | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −3.2 mA | 2.7 | 3.1 | | V |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 7) | $V_{CC}$ = Max, $V_O$ = 0.4V | | 0 | −50 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 7) | $V_{CC}$ = Max, $V_O$ = 2.4V | | 0 | 50 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 8) | $V_{CC}$ = 5V, $V_O$ = 0V | −50 | −77 | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | 125 | 180 | mA |
| $C_I$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_I$ = 2.0V | | 8 | | pF |
| $C_O$ | Output Capacitance | $V_{CC}$ = 5.0V, $V_O$ = 2.0V | | 8 | | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V | | 8 | | pF |

## Series-D (PAL16L8D, PAL16R4D, PAL16R6D, PAL16R8D) (Continued)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** $V_O$ must not exceed $V_{CC}$ + 1V

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(2t_W)^{-1}$.

**Note 5:** All typical values are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.

**Note 6:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

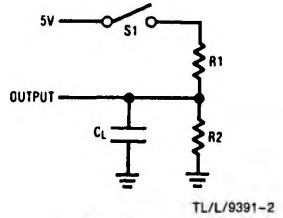
**Note 7:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 8:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | 7.1 | 10 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | | 5.5 | 8 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 5.5 | 10 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 4.0 | 10 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | | 7.2 | 10 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | | 5.0 | 10 | ns |
| $t_{RESET}$ | Power-Up to Registered Output High | | | | 1000 | ns |

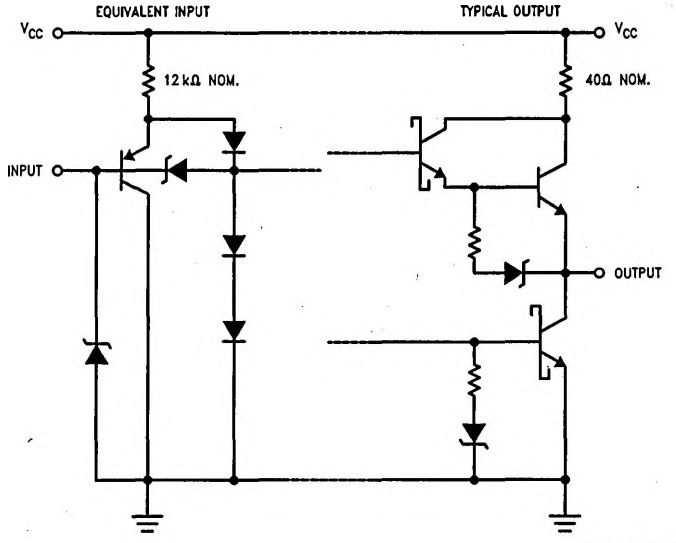
## Test Load




TL/L/9391-2

R1 = 200
R2 = 390

## Schematic of Inputs and Outputs




TL/L/9391-24

# 7 ns Series (PAL16L8-7, PAL16R4-7, PAL16R6-7, PAL16R8-7)

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 2) | −0.5V to +7.0V |
| Input Voltage (Note 2) | −1.5V to +7.0V |
| Off-State Output Voltage ($V_O$) (Notes 2 & 3) | −1.5V to +5.5V |
| Input Current (Note 2) | −30.0 mA to +5.0 mA |
| Output Current ($I_{OL}$) | +100 mA |
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature with Power Applied | −65°C to +125°C |
| Junction Temperature | −65°C to +150°C |
| ESD Tolerance | TBD |

$C_{ZAP}$ = 100 pF
$R_{ZAP}$ = 1500Ω
Test Method: Human Body Model
Test Specification: NSC SOP-5-028

## Recommended Operating Conditions

| Symbol | Parameter | | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $T_A$ | Operating Free-Air Temperature | | 0 | 25 | 75 | °C |
| $t_W$ | Clock Pulse Width | Low | 5.0 | | | ns |
| | | High | 5.0 | | | ns |
| $t_{SU}$ | Setup Time from Input or Feedback to Clock | | 6.5 | | | ns |
| $t_H$ | Hold Time of Input after Clock | | 0 | | | ns |
| $f_{CLK}$ | Clock Frequency (Note 4) | With Feedback | | | 77 | MHz |
| | | Without Feedback | | | 100 | MHz |
| $V_Z$ | Register Preload Control Voltage | | 9.5 | 9.75 | 10.0 | V |

## Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage (Note 5) | | | | 0.8 | V |
| $V_{IH}$ | High Level Input Voltage (Note 5) | | 2 | | | V |
| $V_{IC}$ | Input Clamp Voltage | $V_{CC}$ = Min, I = −18 mA | | | −1.2 | V |
| $I_{IL}$ | Low Level Input Current (Note 6) | $V_{CC}$ = Max, $V_I$ = 0.4V | | | −250 | μA |
| $I_{IH}$ | High Level Input Current (Note 6) | $V_{CC}$ = Max, $V_I$ = 2.4V | | | 25 | μA |
| $I_I$ | Maximum Input Current | $V_{CC}$ = Max, $V_I$ = 5.5V | | | 100 | μA |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = 24 mA | | | 0.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = −3.2 mA | 2.7 | | | V |
| $I_{OZL}$ | Low Level Off-State Output Current (Note 6) | $V_{CC}$ = Max, $V_O$ = 0.4V | | | −50 | μA |
| $I_{OZH}$ | High Level Off-State Output Current (Note 6) | $V_{CC}$ = Max, $V_O$ = 2.4V | | | 50 | μA |
| $I_{OS}$ | Output Short-Circuit Current (Note 7) | $V_{CC}$ = 5V, $V_O$ = 0V | −50 | | −130 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max, Outputs Open | | 125 | 180 | mA |
| $C_I$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_I$ = 2.0V | | 8 | | pF |
| $C_O$ | Output Capacitance | $V_{CC}$ = 5.0V, $V_O$ = 2.0V | | 8 | | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V | | 8 | | pF |

# 7 ns Series (PAL16L8-7, PAL16R4-7, PAL16R6-7, PAL16R8-7)

**Note 1:** Absolute maximum ratings are those values beyond which the device may be permanently damaged. Proper operation is not guaranteed outside the specified recommended operating conditions.

**Note 2:** Some device pins may be raised above these limits during programming and preload operations according to the applicable specification.

**Note 3:** $V_O$ must not exceed $V_{CC}$ + 1V

**Note 4:** $f_{CLK}$ with feedback is derived as $(t_{CLK} + t_{SU})^{-1}$.
$f_{CLK}$ without feedback is derived as $(2t_W)^{-1}$.

**Note 5:** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

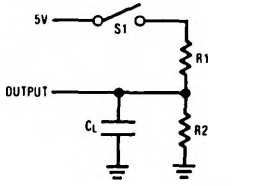
**Note 6:** Leakage current for bidirectional I/O pins is the worst case between $I_{IL}$ and $I_{OZL}$ or between $I_{IH}$ and $I_{OZH}$.

**Note 7:** To avoid invalid readings in other parameter tests it is preferable to conduct the $I_{OS}$ test last. To minimize internal heating, only one output should be shorted at a time with a maximum duration of 1.0 second each. Prolonged shorting of a High output may raise the chip temperature above normal and permanent damage may result.

## Switching Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Commercial | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | $C_L$ = 50 pF, S1 Closed | | | 7.0 | ns |
| $t_{CLK}$ | Clock to Registered Output or Feedback | $C_L$ = 50 pF, S1 Closed | 3.0 | | 6.5 | ns |
| $t_{PZXG}$ | $\overline{G}$ Pin to Registered Output Enabled | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | 3.0 | | 7.0 | ns |
| $t_{PXZG}$ | $\overline{G}$ Pin to Registered Output Disabled | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | 3.0 | | 7.0 | ns |
| $t_{PZXI}$ | Input to Combinatorial Output Enabled via Product Term | $C_L$ = 50 pF, Active High: S1 Open, Active Low: S1 Closed | 3.0 | | 7.0 | ns |
| $t_{PXZI}$ | Input to Combinatorial Output Disabled via Product Term | $C_L$ = 5 pF, From $V_{OH}$: S1 Open, From $V_{OL}$: S1 Closed | 3.0 | | 7.0 | ns |
| $t_{SKEW}$ | Skew between Registered Outputs | | | | 1.0 | ns |
| $t_{RESET}$ | Power-Up to Registered Output High | | | | 1000 | ns |

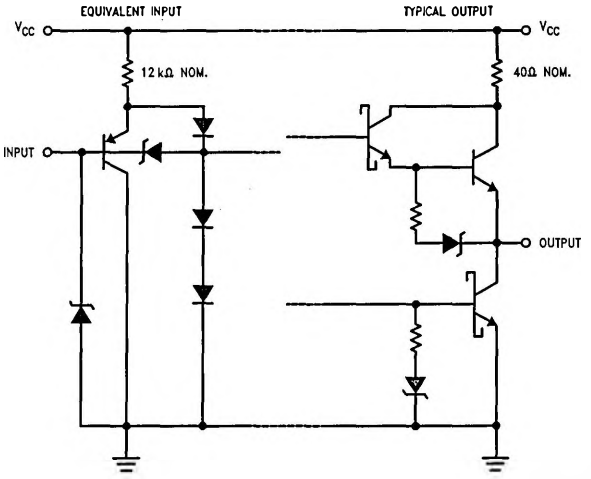
## Test Load




TL/L/9391-28

R1 = 200
R2 = 390

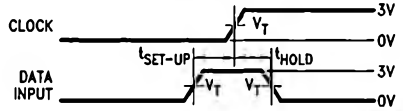
## Schematic of Inputs and Outputs




TL/L/9391-29

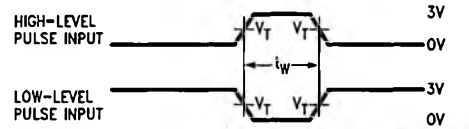
## Test Waveforms

### Set-Up and Hold



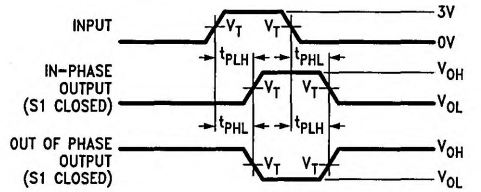

TL/L/9391-3

### Pulse Width



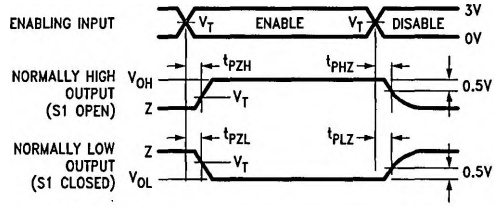

TL/L/9391-4

### Propagation Delay




TL/L/9391-5

### Enable and Disable




TL/L/9391-6

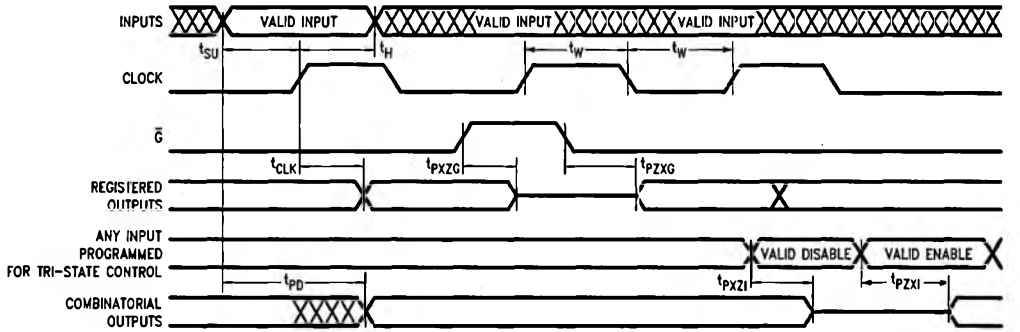
**Notes:**

$V_T$ = 1.5V

$C_L$ includes probe and jig capacitance.

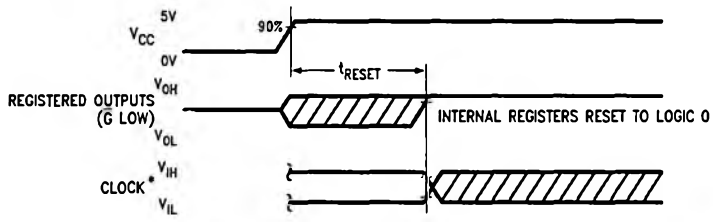
In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

## Switching Waveforms




TL/L/9391-8

## Power-Up Reset Waveform




TL/L/9391-9

*The clock input should not be switched from low to high until after time $t_{RESET}$.

## Functional Description

All of the 20-pin Medium PAL logic arrays consist of 16 complementary input lines and 64 product-term lines with a programmable cell at each intersection (2048 cells). The product terms are organized into eight groups of eight each. Seven or eight of the product terms in each group connect into an OR-gate to produce the sum-of-products logic function, depending on whether the output is combinatorial or registered.

For the fuse-link PAL devices (all PAL devices excluding D and -7) an unprogrammed (intact) fuse establishes a connection between an input line (true or complement phase of an array input signal) and a product term; programming the fuse removes the connection. In the National Series-D/-7 vertical fuse PAL devices, a programmed vertical fuse cell establishes a connection between an input line and a product term. A product term is satisfied (logically true) while all of the input lines connected to it (via unprogrammed fuses for the fuse-link devices, or by programming the corresponding cells for the vertical fuse devices) are in the high logic state. Therefore, if both the true and complement of at least one array input is connected to a product line, that product term is always held in the low logic state (which is the state of all product terms in an unprogrammed fuse-link device). Conversely, if all input lines are disconnected from a product line, the product term and the resulting logic function would be held in the high state (which is the state of all product terms in an unprogrammed National Series-D/-7 PAL device).

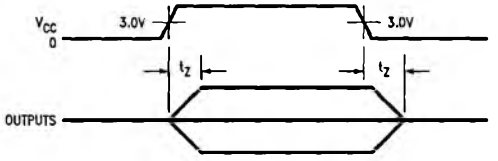
The medium PAL family consists of four device types with differing mixtures of combinatorial and registered outputs. The 16L8, 16R4, 16R6 and 16R8 architectures have 0, 4, 6 and 8 registered outputs, respectively, with the balance of the 8 outputs combinatorial. All outputs are active-low and have TRI-STATE capability.

Each combinatorial output has a seven product-term logic function, with the eighth product term being used for TRI-STATE control. A combinatorial output is enabled while the TRI-STATE product term is satisfied (true). Combinatorial outputs also have feedback paths from the device pins into the logic array (except for two outputs on the 16L8). This allows a pin to perform bidirectional I/O or, if the associated TRI-STATE control product term were programmed to remain unsatisfied (always false), the output driver would remain disabled and the pin could be used as an additional dedicated input.

Registered outputs each have an eight product-term logic function feeding into a D-type flip-flop. All registers are triggered by the high-going edge of the clock input pin. All registered outputs are controlled by a common output enable ($\overline{G}$) pin (enabled while low). The output of each register is also fed back into the logic array via an internal path. This provides for sequential logic circuits (state machines, counters, etc.) which can be sequenced even while the outputs are disabled.

Series-D/-7 Medium PAL devices reset all registers to a low state upon power-up (active-low outputs assume high logic levels if enabled). This may simplify sequential circuit design and test. To ensure successful power-up reset, $V_{CC}$ must rise monotonically until the specified operating voltage is attained. During power-up, the clock input should assume a valid, stable logic state as early as possible to avoid interfering with the reset operation. The clock input should also remain stable until after the power-up reset operation is completed to allow the registers to capture the proper next state on the first high-going clock transition.

For the National Series-D/-7 PAL device, during power-up, all outputs are held in the high-impedance state until DC power supply conditions are met ($V_{CC}$ approximately 3.0V), after which they may be enabled by the TRI-STATE control product terms (combinatorial outputs) or the $\overline{G}$ pin (registered outputs). Whenever $V_{CC}$ goes below 3V (at 25°C), the outputs are disabled as shown in *Figure 1* below.




TL/L/9391–25

**Note:** $t_Z$ is less than 100 ns.

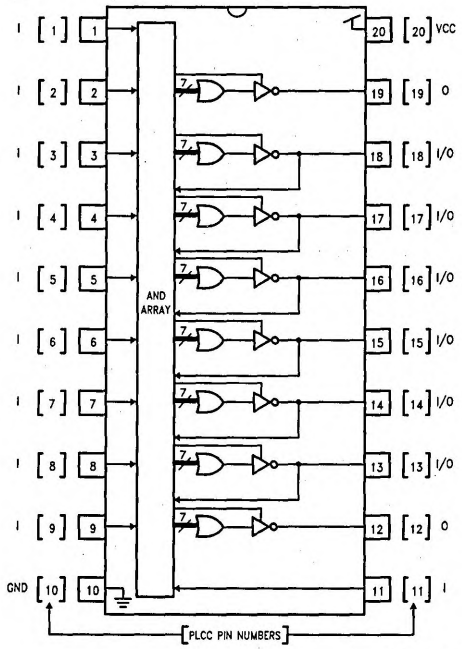
**FIGURE 1. Series-D Power-Up TRI-STATE Waveform**

In an unprogrammed National Series-D/-7 PAL device, no array inputs are connected to any product-term lines. Therefore, all combinatorial outputs would be enabled and driving low logic levels (after power-up is completed). All registers would still initialize to the low state, but would become permanently set (low-level outputs, if enabled) following the first clock transition.

As with any TTL logic circuits, unused inputs to a PAL device should be connected to ground, $V_{OL}$, $V_{OH}$, or resistively to $V_{CC}$. However, switching any input not connected to a product term or logic function has no effect on its output logic state.

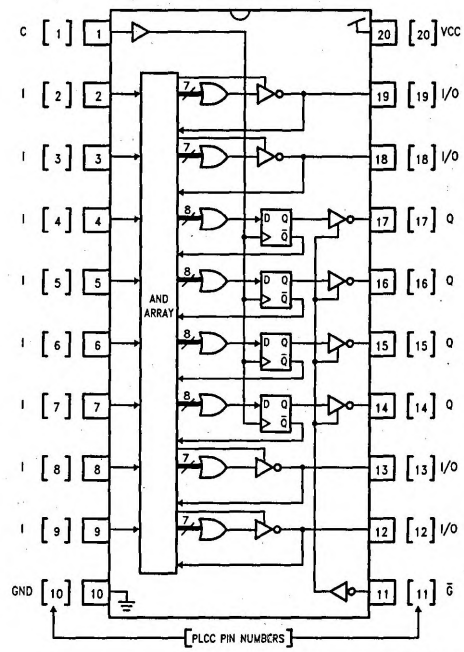
# 20-Pin Medium PAL Family Block Diagrams—DIP Connections

## PAL16L8



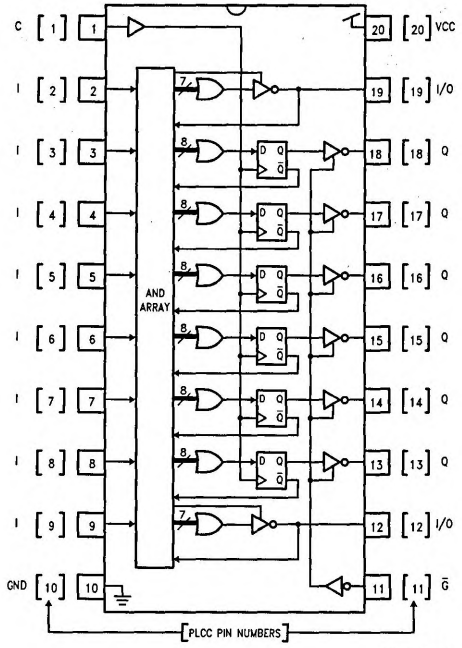

TL/L/9391-10

## PAL16R4



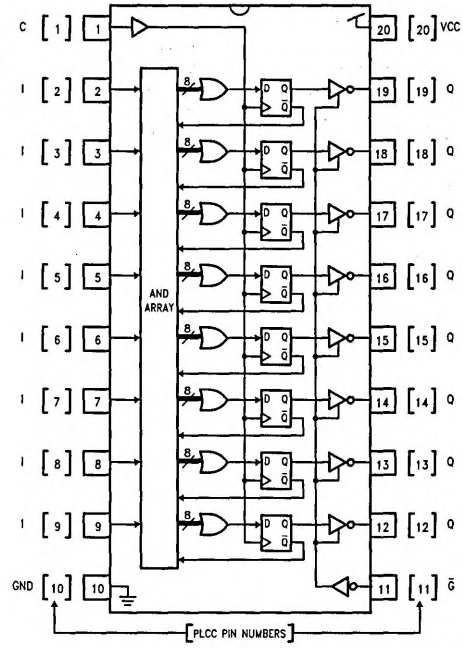

TL/L/9391-11

## PAL16R6



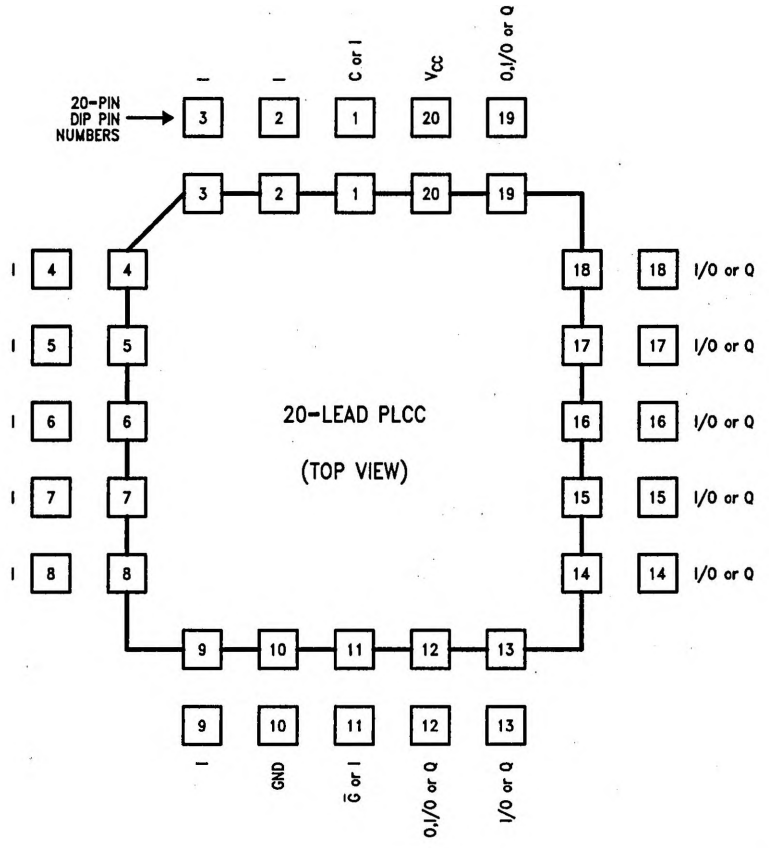

TL/L/9391-12

## PAL16R8



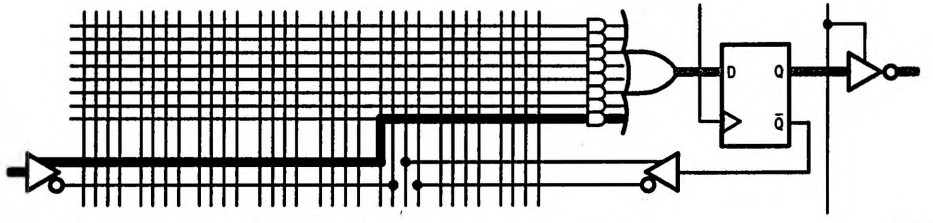

TL/L/9391-13

## 20-Lead PLCC Connection Conversion Diagram



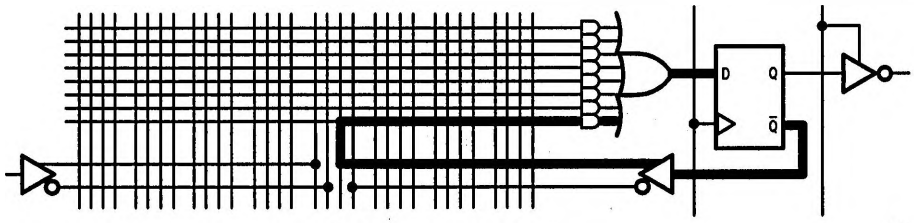

TL/L/9391-14

**Typical Registered Logic Function Without Feedback**




TL/L/9391-15

**Typical Registered Logic Function With Feedback**




TL/L/9391-16

## Functional Description (Continued)

### CLOCK FREQUENCY SPECIFICATION

The clock frequency ($f_{CLK}$) parameter specifies the maximum speed at which a registered PAL device is guaranteed to operate. Clock frequency is defined differently for the two cases in which register feedback is used versus when it is not. In a data-path type application, where the logic functions fed into the registers are not dependent on register feedback from the previous cycle (i.e.—based only on external inputs), the minimum required cycle period ($f_{CLK}^{-1}$ without feedback) is defined as the greater of the minimum clock period ($t_W$ high + $t_W$ low) and the minimum "data window" period ($t_{SU}$ + $t_H$). This assumes optimal alignment between data inputs and the clock input. In sequential logic applications such as state machines, the minimum required cycle period ($f_{CLK}^{-1}$ with feedback) is defined as $t_{CLK}$ + $t_{SU}$. This provides sufficient time for outputs from the registers to feed back through the logic array and set-up on the inputs to the registers before the end of each cycle.

## Output Register Preload

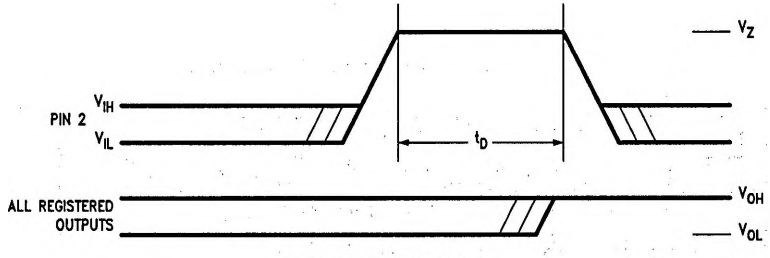
In the 20-pin Medium PAL family, register preload is available on the Series-D/-7 PAL devices only.

The output register preload feature simplifies device testing since any state may be loaded into the registers at any time during the functional test sequence. This allows complete verification of sequential logic circuits, including states that are normally impossible or difficult to reach. Register preload is not an operational mode and is not intended for board level testing because elevated voltage levels are required. The programming system normally provides the preload capability as part of its functional test facility.

The preload function allows the register to be loaded directly and asynchronously with any desired pattern. These vertical-fuse devices provide two register preload operations:

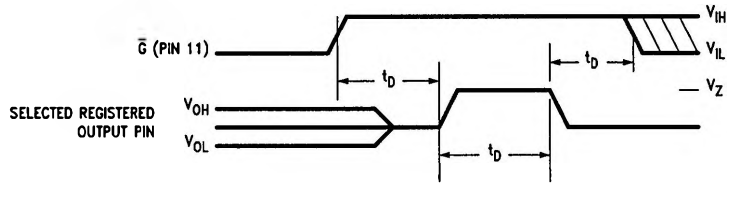
1. All registers can be reset to the low state (high-level outputs) by applying the elevated control voltage ($V_Z$) to input Pin 2* for time $t_D$ *(Figure 2a)*.
2. Selected registers can be set to the high state (low-level outputs) as follows *(Figure 2b)*:
   a. All registered outputs are disabled by raising the $\overline{G}$ input Pin 1* to $V_{IH}$.
   b. After time $t_D$, the selected registered output pins are raised to the elevated control voltage ($V_Z$) for time $t_D$ to set the corresponding registers.

*Applies to both DIP and PCC packages for 20-pin PAL devices.




TL/L/9391-26

**a) To Reset All Registers**




TL/L/9391-27

**b) To Set Selected Registers**

**Note:** $V_Z$ = 9.5V to 10.0V, $t_D$ min. = 500 ns.

**FIGURE 2. Series-D Register Preload Waveforms**

## Security Fuse

Security fuses are provided on all National PAL devices which, when programmed, inhibit any further programming or verifying operations. This feature prevents direct copying of proprietary logic patterns. The security fuses should be programmed only after programming and verifying all other device fuses. Register preload is not affected by the security fuses.

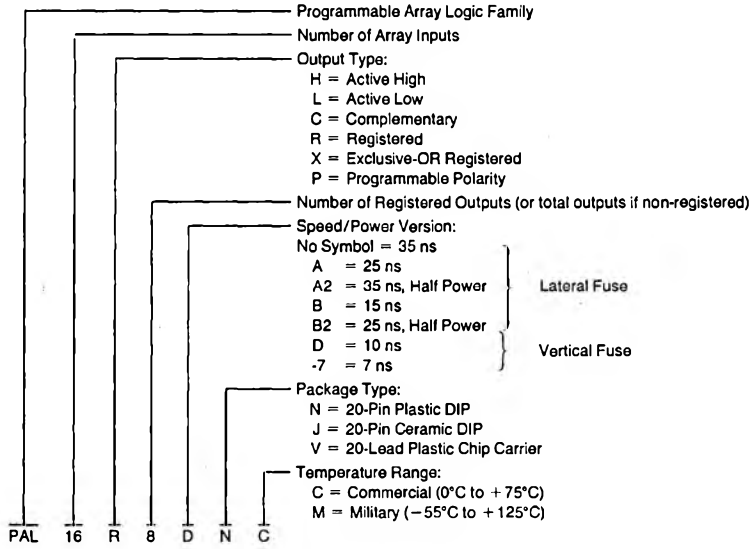
## Design Development Support

A variety of software tools and programming hardware is available to support the development of designs using PAL products. Typical software packages accept Boolean logic equations to define desired functions. Most are available to run on personal computers and generate JEDEC-compatible "fuse maps". The industry-standard JEDEC format ensures that the resulting fuse-map files can be down-loaded into a variety of programming equipment. Many software packages and programming units support a wide variety of programmable logic products as well. The PLAN™ software package from National Semiconductor supports all programmable logic products available from National and is fully JEDEC-compatible. PLAN software also provides automatic device selection based on the designer's Boolean logic equations.

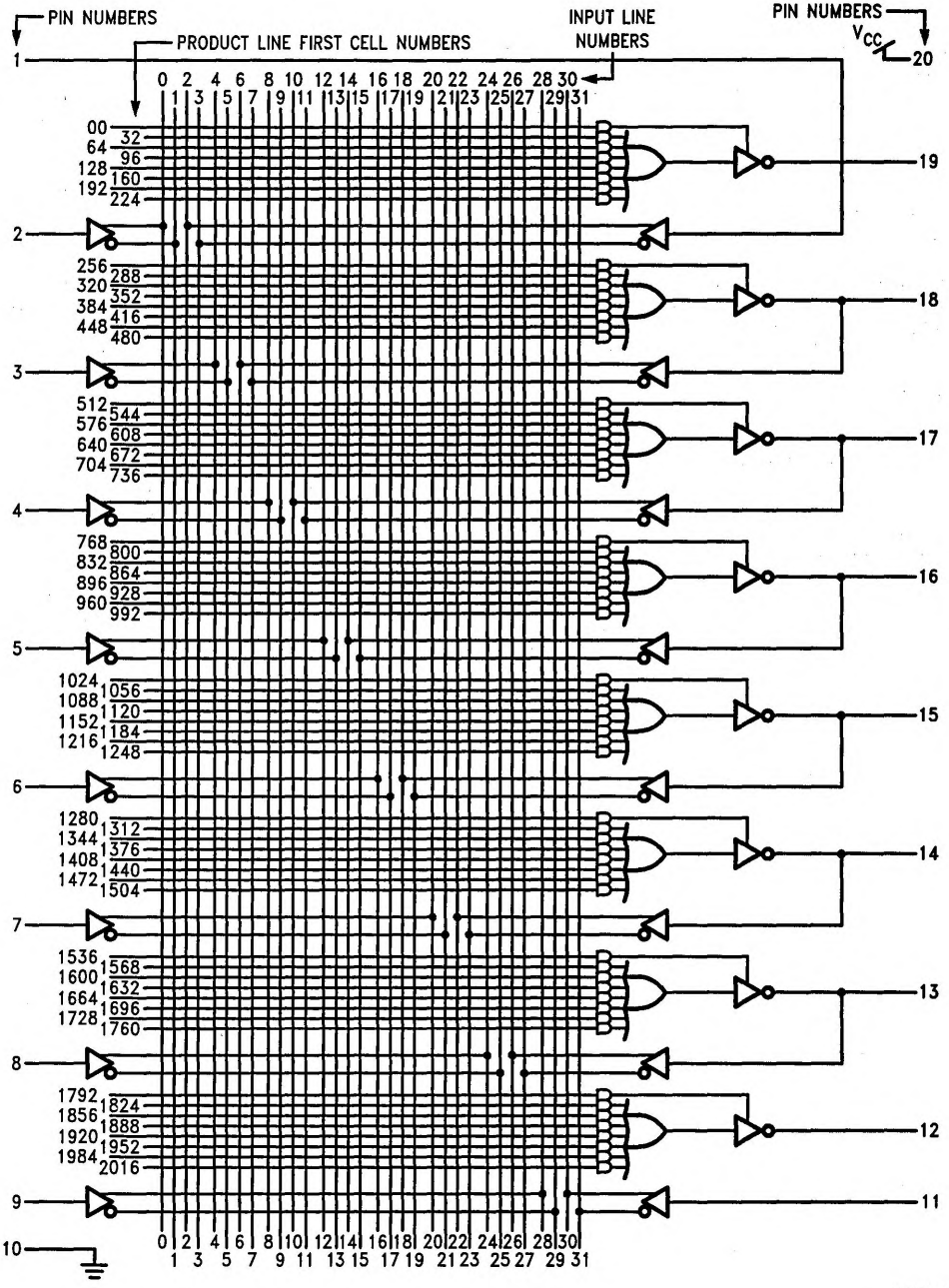
In National Series-D/-7 PAL devices, logical and physical connections between array input lines and product-term lines are established when vertical fuse cells are programmed. This is opposite to other PAL products based on fusible links in which connections are established when fuses are left unprogrammed (intact). This difference is compensated by the vertical-fuse PAL programming algorithm so that the *user's design development process looks the same.* (The only functional difference due to vertical-fuse technology is the behavior of "unprogrammed" devices.) The JEDEC programming maps produced by PAL development software for all Medium PAL devices denote a "connection" with a "0", and a "non-connection" with a "1". The programming algorithms for most fuse-link PLDs program fuses where ones are located in the map to remove corresponding connections, whereas the algorithm for National Series-D PAL products automatically compensates by programming vertical-fuse cells where zeroes are located in the map to establish connections. Therefore, the *same JEDEC map* representing the user's desired logic equations produces the *same functional results* when using either PAL technology. The user need only provide the appropriate device code and/or adapter for the programming equipment to invoke the proper programming algorithm. Only programmers with the certified National Series-D/-7 vertical-fuse PAL programming algorithm can be used to program these vertical-fuse devices.

Detailed logic diagrams showing all JEDEC fuse-map addresses for the 20-pin Medium PAL family are provided for direct map editing and diagnostic purposes. For a list of current software and programming support tools available for these devices, please contact your local National Semiconductor sales representative or distributor. If detailed specifications of the PAL programming algorithm are needed, please contact the National Semiconductor Programmable Device Support Department.

## Ordering Information



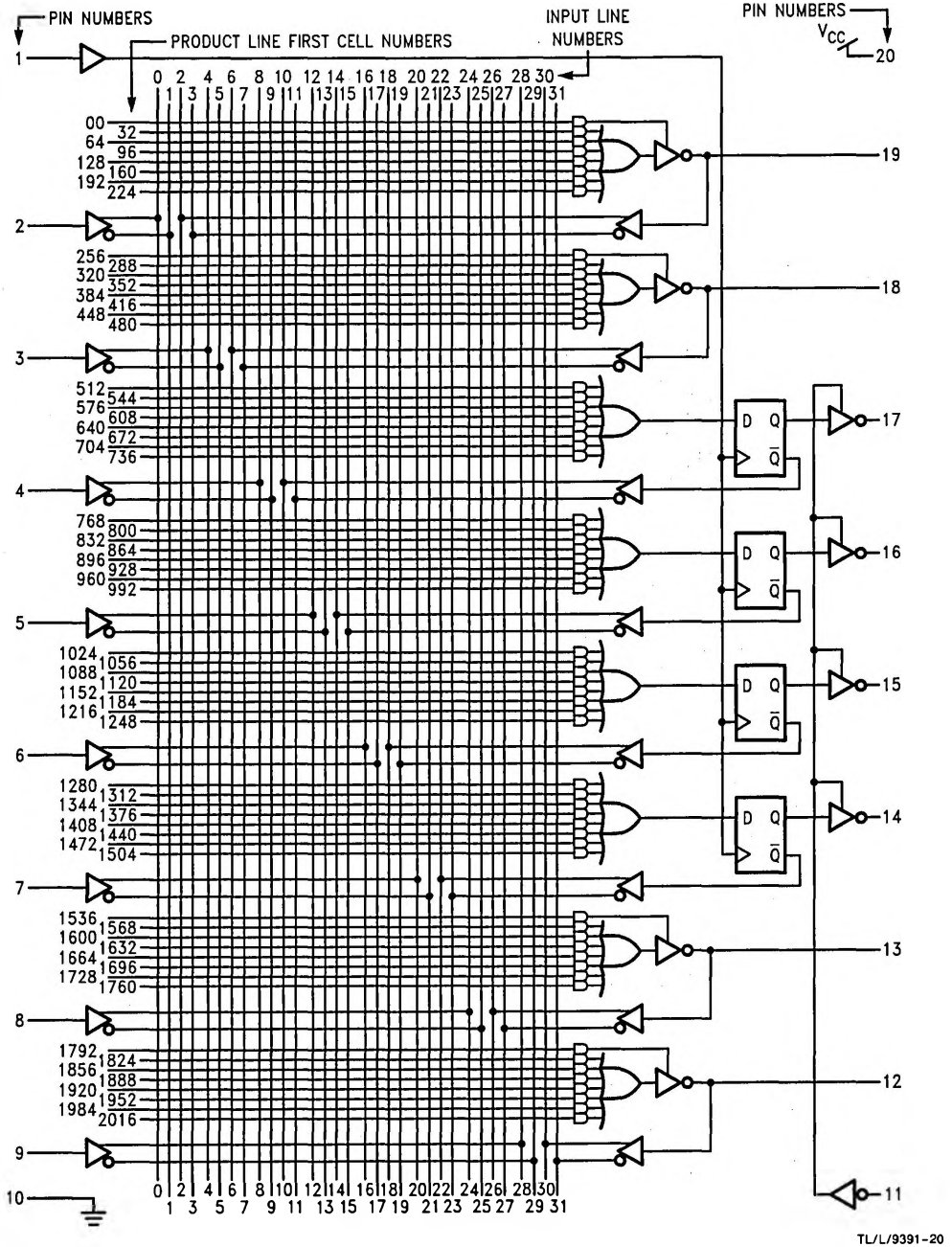
## Logic Diagram—PAL16L8




TL/L/9391–19

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

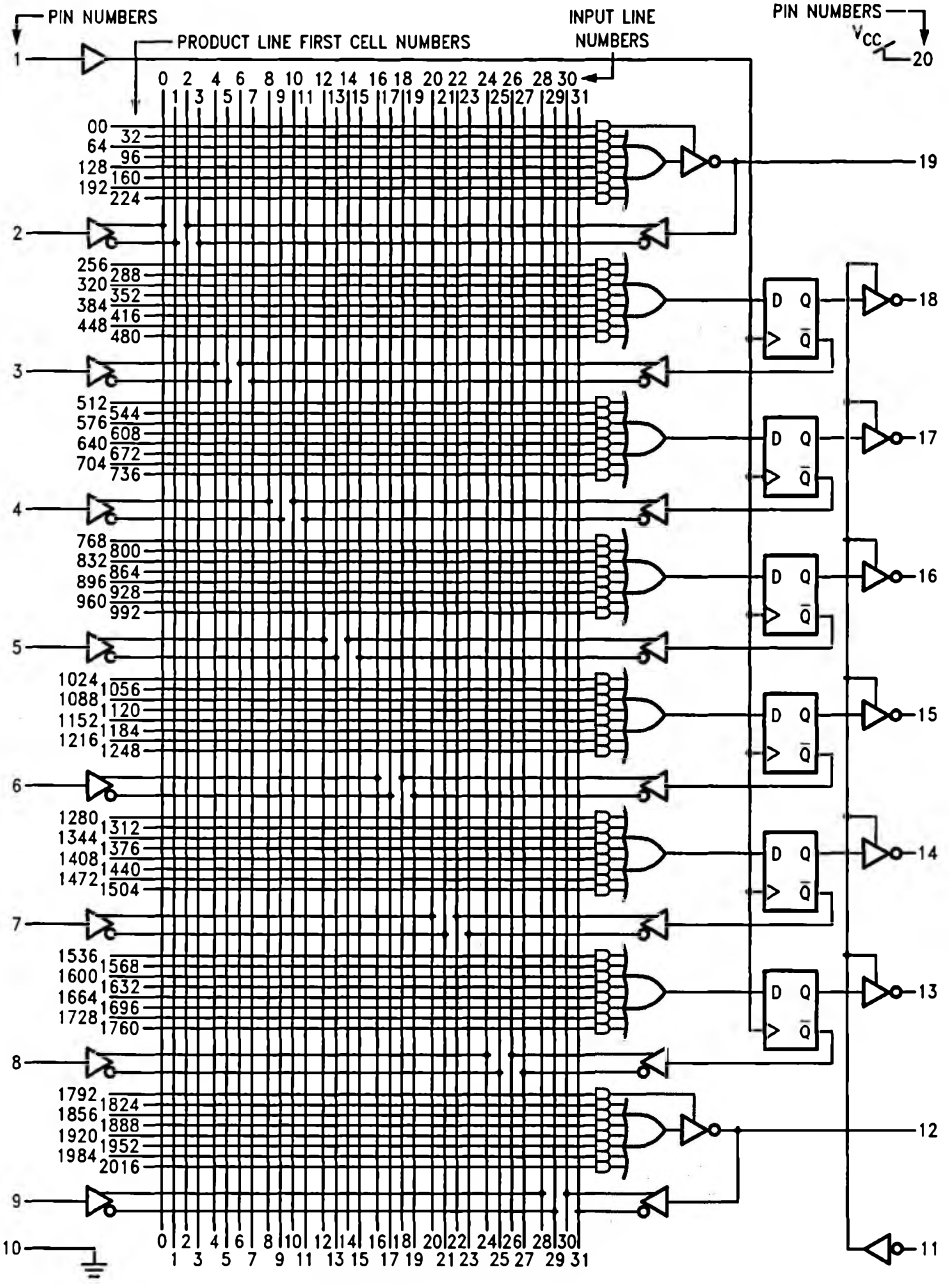
## Logic Diagram—PAL16R4




TL/L/9391-20

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

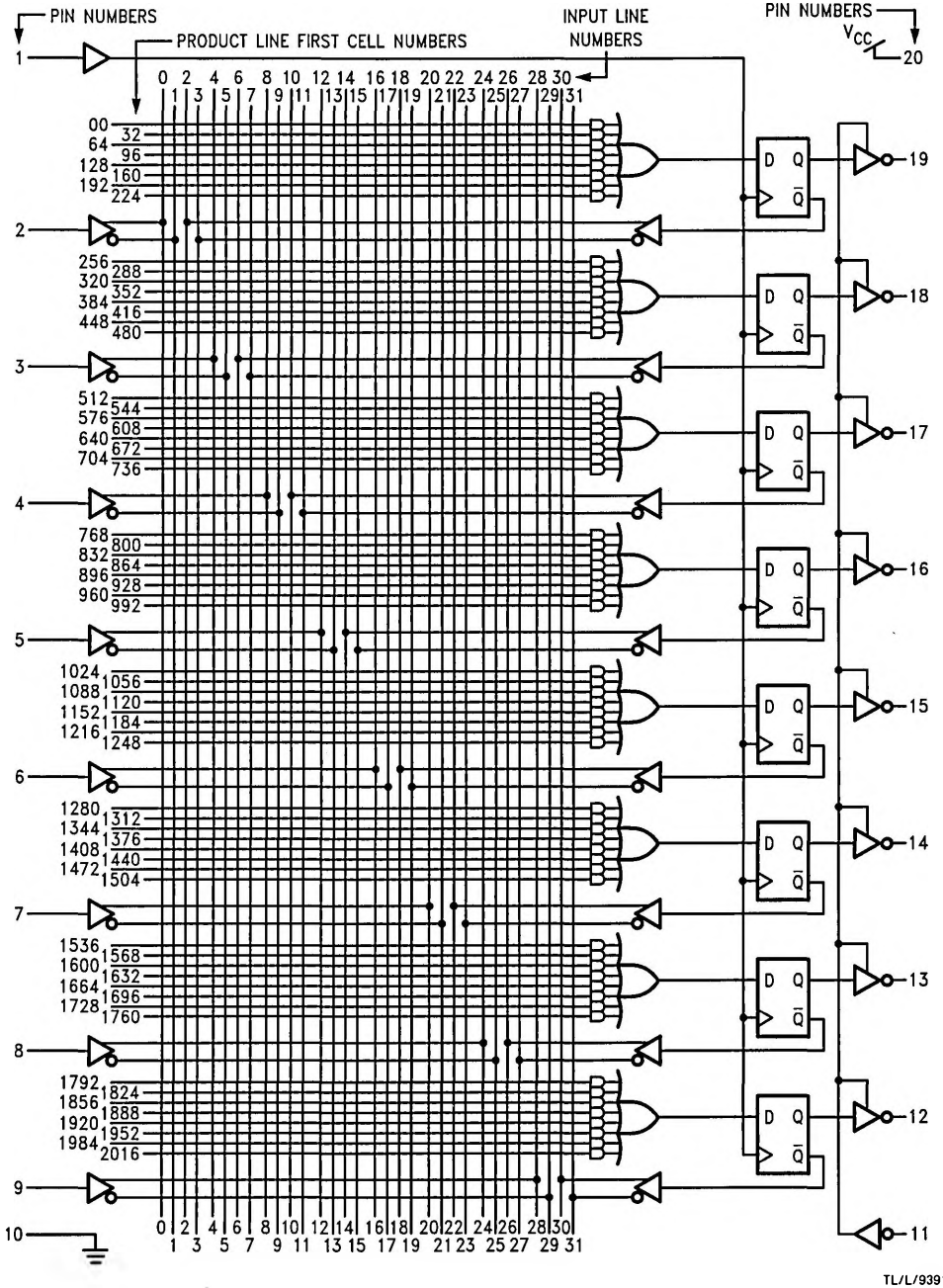
## Logic Diagram—PAL16R6




TL/L/9391–21

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number

## Logic Diagram—PAL16R8




TL/L/9391-22

JEDEC Logic Array Cell Number = Product Line First Cell Number + Input Line Number