NT512S64V8HA0G
512MB : 64M x 64
Unbuffered SDRAM Module

64Mx64 bit Two Bank Unbuffered SDRAM Module
based on 32Mx8, 4Banks, 8K Refresh, 3.3V Synchronous DRAMs with SPD

Features

- 168-Pin Unbuffered 8-Byte Dual In-Line Memory Module
- Intended for PC133 applications
  - Clock Frequency: 133MHz
  - Clock Cycle: 7.5ns
  - Clock Assess Time: 5.4ns
- Inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed RAS interface
- SDRAMs have 4 internal banks
- Module has 2 physical banks
- Fully Synchronous to positive Clock Edge
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge commands
- Programmable Operation:
  - CAS Latency: 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Suspend Mode and Power Down Mode
- 8K Refresh cycles distributed across 64ms
- Gold contacts
- SDRAMs in TSOP Type II Package
- Serial Presence Detect with Write Protect

Description

NT512S64V8HA0G is unbuffered 168-pin Synchronous DRAM Dual In-Line Memory Modules (DIMMs) which is organized as 64Mx64 high-speed memory arrays and is configured as two 32M x 64 physical bank. The DIMM uses sixteen 32Mx8 SDRAMs in 400mil TSOP II packages. The DIMM achieves high-speed data transfer rates of up to 133MHz by employing a prefetch / pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.
All inputs are sampled at the positive edge of each externally supplied clock (CK0 - CK3). Internal operating modes are defined by combinations of $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$ - $\overline{S3}$, DQMB, and CKE0 – CKE1 signals. A command decoder initiates the necessary timings for each operation. A 14-bit address bus accepts address information in a row / column multiplexing arrangement.

Prior to any Access operation, the $\overline{CAS}$ latency, burst type, burst length, and Burst operation type must be programmed into the DIMM by address inputs A0-A9 during the Mode Register Set cycle. The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

Ordering Information

Part Number	Speed				Organization	Leads	Power
	MHz.	CL	t RCD	t RP			
NT512S64V8HA0G-7K	143MHz	3	3	3	64Mx64	Gold	3.3V
	133MHz	2	2	2			
NT512S64V8HA0G-75B	133MHz	3	3	3			
	100MHz	2	2	2			
NT512S64V8HA0G-8B	125MHz	3	3	3			
	100MHz	2	2	2			

* CL = CAS Latency

Pin Description

CK0, CK1 CK2, CK3	Clock Inputs	DQ0-DQ63	Data input/output
		CB0-CB7	Check Bit Data input/output
CKE0 – CKE1	Clock Enable	DQMB0-DQMB7	Data Mask
$\overline{RAS}$	Row Address Strobe	VDD	Power (3.3V)
$\overline{CAS}$	Column Address Strobe	VSS	Ground
$\overline{WE}$	Write Enable	NC	No Connect
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$	Chip Selects	SCL	Serial Presence Detect Clock Input
A0-A9, A12	Address Inputs	SDA	Serial Presence Detect Data input/output
A10 / AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0, BA1	SDRAM Bank Address Inputs	WP	Serial Presence Detect Write Protect Input

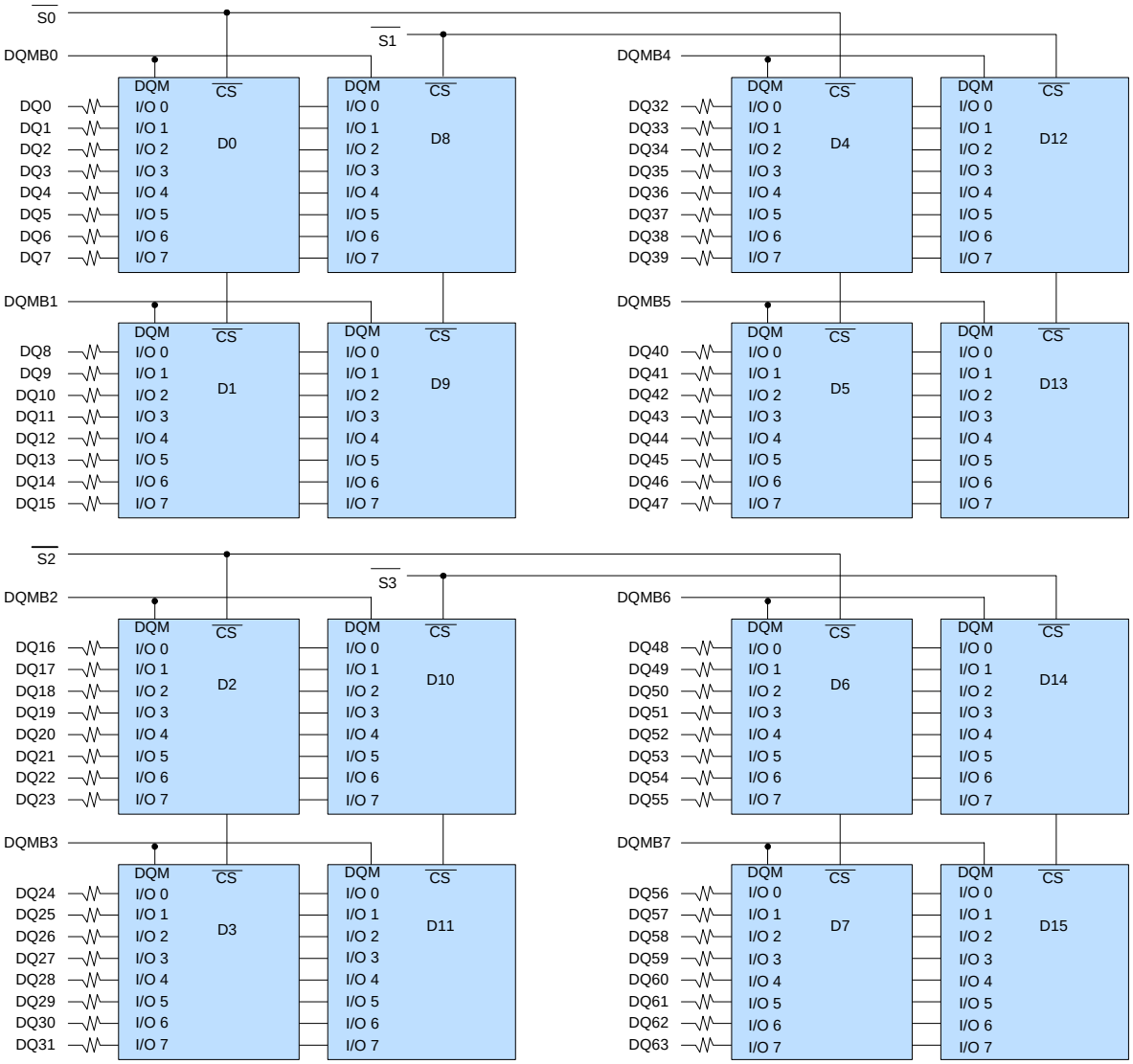
Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	85	VSS	29	DQMB1	113	DQMB5	57	DQ18	141	DQ50
2	DQ0	86	DQ32	30	$\overline{S0}$	114	$\overline{S1}$	58	DQ19	142	DQ51
3	DQ1	87	DQ33	31	NC	115	$\overline{RAS}$	59	VDD	143	VDD
4	DQ2	88	DQ34	32	VSS	116	VSS	60	DQ20	144	DQ52
5	DQ3	89	DQ35	33	A0	117	A1	61	NC	145	NC
6	VDD	90	VDD	34	A2	118	A3	62	NC	146	NC
7	DQ4	91	DQ36	35	A4	119	A5	63	CKE1*	147	NC
8	DQ5	92	DQ37	36	A6	120	A7	64	VSS	148	VSS
9	DQ6	93	DQ38	37	A8	121	A9	65	DQ21	149	DQ53
10	DQ7	94	DQ39	38	A10/AP	122	BA0	66	DQ22	150	DQ54
11	DQ8	95	DQ40	39	BA1	123	A11	67	DQ23	151	DQ55
12	VSS	96	VSS	40	VDD	124	VDD	68	VSS	152	VSS
13	DQ9	97	DQ41	41	VDD	125	CK1	69	DQ24	153	DQ56
14	DQ10	98	DQ42	42	CK0	126	A12	70	DQ25	154	DQ57
15	DQ11	99	DQ43	43	VSS	127	VSS	71	DQ26	155	DQ58
16	DQ12	100	DQ44	44	NC	128	CKE0	72	DQ27	156	DQ59
17	DQ13	101	DQ45	45	$\overline{S2}$	129	$\overline{S3}$	73	VDD	157	VDD
18	VDD	102	VDD	46	DQMB2	130	DQMB6	74	DQ28	158	DQ60
19	DQ14	103	DQ46	47	DQMB3	131	DQMB7	75	DQ29	159	DQ61
20	DQ15	104	DQ47	48	NC	132	NC	76	DQ30	160	DQ62
21	CB0	105	CB4	49	VDD	133	VDD	77	DQ31	161	DQ63
22	CB1	106	CB5	50	NC	134	NC	78	VSS	162	VSS
23	VSS	107	VSS	51	NC	135	NC	79	CK2	163	CK3
24	NC	108	NC	52	CB2	136	CB6	80	NC	164	NC
25	NC	109	NC	53	CB3	137	CB7	81	WP	165	SA0
26	VDD	110	VDD	54	VSS	138	VSS	82	SDA	166	SA1
27	$\overline{WE}$	111	$\overline{CAS}$	55	DQ16	139	DQ48	83	SCL	167	SA2
28	DQMB0	112	DQMB4	56	DQ17	140	DQ49	84	VDD	168	VDD

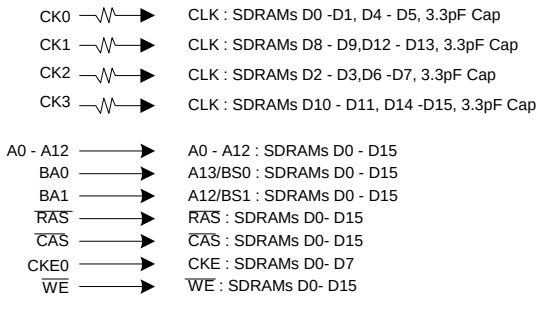
Note: All pin assignments are consistent for all 8-byte unbuffered versions.

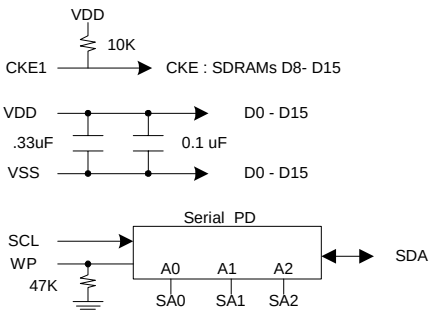
*CKE1 is terminated with a 10k ohm pullup resistor.

SDRAM DIMM Block Diagram (2 Bank, 32Mx8 SDRAMs)



NOTE : Exact DQ wiring may differ from that shown above





*All resistor values are 10 ohms except as shown.

Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0 ~ CK3	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0, CKE1	Input	Level	Active High	Activates the SDRAM CK0 ~ CK3 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self-Refresh mode.
$\overline{S0}$ ~ $\overline{S3}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, BA1	Input	Level	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A12	Input	Level	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63, CB0 - CB7	Input /Output	Level	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQMB0 -DQMB7	Input	Pulse	Active High	The Data input/output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high.
SA0 – SA2	Input	Level	-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	Input /Output	Level	-	Serial Data. Bi-directional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pull-up resistor is required on the system board.
SCL	Input	Pulse	-	Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the “high” state, a pull-up resistor is recommended on the system board.
WP	Input	Level	Active High	Hardware Write Protect. When WP is active, writing to the EEPROM array is inhibited. On the DIMM, this input is connected to the EEPROM Write Protect input and is also tied to ground through a 47K ohm pull-down resistor.
V_{DD}, V_{SS}	Supply			Power and ground for the module.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-0.3 to +4.6	V	1
V_{IN}	Input Voltage	-0.3 to V_{DD} +0.3		
V_{OUT}	Output Voltage	-0.3 to V_{DD} +0.3		
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	16	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70 °C)

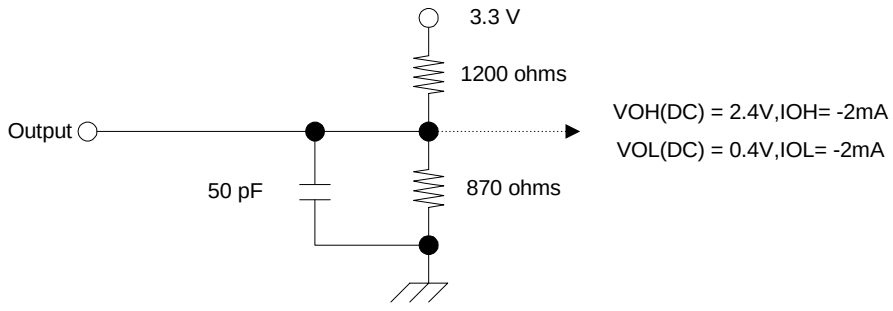
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Power Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	-	V_{DD} + 0.3	V	1,2
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	1,3
V_{OH}	Output High Voltage	2.4	-	-	V	
V_{OL}	Output Low Voltage	-	-	0.4	V	
I_{IL}	Input Leakage current	-10	-	10	uA	

1. All voltages referenced to V_{SS}.
2. V_{IH} (max) = V_{DD} / V_{DDQ} + 1.2V for pulse width ≤ 5ns
3. V_{IL} (min) = V_{SS} / V_{SSQ} - 1.2V for pulse width ≤ 5ns .

Capacitance (T_A=25 °C, f =1MHz, V_{DD}=3.3 ± 0.3V)

Symbol	Parameter	Max.	Unit
C_{I1}	Input Capacitance (A0-A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	100	pF
C_{I2}	Input Capacitance (CKE0 ~ CKE1)	60	
C_{I3}	Input Capacitance ($\overline{S0}$, $\overline{S2}$)	30	
C_{I4}	Input Capacitance (CK0 - CK3)	45	
C_{I5}	Input Capacitance (DQMB0 - DQMB7)	20	
C_{I6}	Input Capacitance (SA0 - SA2, SCL, WP)	9	
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	20	
C_{IO2}	Input/Output Capacitance (SDA)	11	

DC Output Load Circuit



Operating, Standby, and Refresh Currents (T_A =0 to 70 °C , V_{DD} =3.3 ± 0.3V)

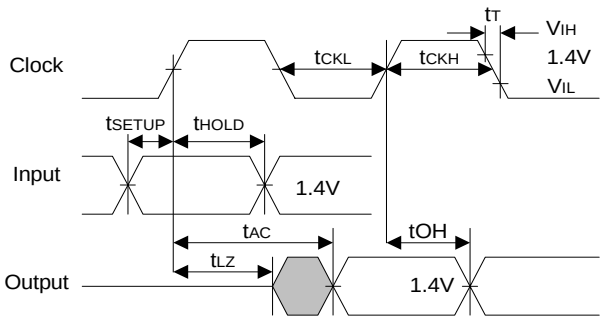
Parameter	Symbol	Test condition	Speed			Unit	Note
			- 7K	- 75B	- 8B		
Operating current	I_{CC1}	1 bank operation , t_{RC} = t_{RC}(mim), t_{CK} = min Active-Precharge Command cycling without burst operation	1200	1080	1080	mA	1, 3,4
Precharge standby current in power-down mode	I_{CC2P}	CKE0 ≤ V_{IL} (max), t_{CK} = min, $\overline{S0}$, $\overline{S2}$ = V_{IH} (min)	32	32	32	mA	2
	I_{CC2PS}	CKE0 ≤ V_{IL} (max), t_{CK} =∞, $\overline{S0}$, $\overline{S2}$ = V_{IH} (min)	32	32	32	mA	2
Precharge standby current in non power-down mode	I_{CC2N}	CKE0 ≥ V_{IH} (min), t_{CK} = min $\overline{S0}$, $\overline{S2}$ = V_{IH} (min)	800	720	720	mA	2,5
	I_{CC2NS}	CKE0 ≥ V_{IH} (min), t_{CK} =∞, $\overline{S0}$, $\overline{S2}$ = V_{IH} (min)	144	144	144	mA	2,6
No Operating current (Active state : 4 bank)	I_{CC3P}	CKE0 ≤ V_{IL} (max), t_{CK} =min. $\overline{S0}$, $\overline{S2}$ = V_{IH} (min) (Power Down Mode)	144	144	144	mA	2,7
	I_{CC3N}	CKE0 ≥ V_{IH} (min), t_{CK} =min $\overline{S0}$, $\overline{S2}$ = V_{IH} (min)	960	800	800	mA	2,5
Operating current (Burst mode)	I_{CC4}	t_{CK} =min , Read/ Write command cycling, Multiple banks active, gapless data, BL=4	1560	1360	1360	mA	1,4,8
Auto(CBR) refresh current	I_{CC5}	t_{CK} =min, CBR command cycling	2000	1920	1920	mA	1
Self refresh current	I_{CC6}	CKE0 ≤ 0.2V	48	48	48	mA	2
Serial PD Device Standby Current	I_{SB}	V_{IN} = GND or V_{DD}	30	30	30	µA	9
Serial PD Device Active Power Supply Current	I_{CCA}	SCL Clock Frequency=100 MHz	1	1	1	µA	10

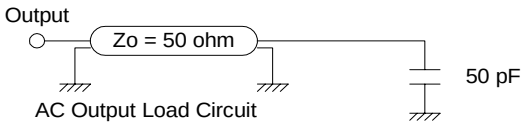
1. The specified values are for one DIMM bank in the specified mode, and the other DIMM bank in Active Standby (I_{CC3N}).
2. The specified values are for both DIMM banks operating in the specified mode.
3. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}.
   Input signals are changed up to three times during t_{RC} (min).
4. The specified values are obtained with the output open.
5. Input signals are changed once during three clock cycles.
6. Input signals are stable.
7. Active Standby current will be higher if clock suspend is entered during a Burst Read cycle (add 1mA per DQ).
8. Input signals are changed once during $t_{CK(min)}$.
9. V_{DD} =3.3V.
10. As follows:
    - Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9
    - Input rise and fall times 10ns
    - Input and output timing levels V_{DD} x 0.5
    - Output load 1 TTL gate and CL=100pF

AC Characteristics (TA =0 to 70 °C , VDD =3.3 ± 0.3V)

1. An initial pause of 200us,with DQMB0-7 and CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. The Transition time is measured between VIH and VIL (or between VIH and VIL).
3. In addition to meeting the transition rate specification, the CK0, CK2, and CKE0 signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
4. AC timing tests have VIL =0.8Vand VIH = 2.0 V with the timing referenced to the 1.40V crossover point.
5. AC measurements assume t T =1.2 ns.

AC Output Load Circuits





AC Timing Parameters

Clock and Clock Enable Parameters

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tCK3	Clock Cycle Time, $\overline{CAS}$ Latency = 3	7	1000	7.5	1000	8	1000	ns	
tCK2	Clock Cycle Time, $\overline{CAS}$ Latency = 2	7.5	1000	10	1000	10	1000	ns	
tAC3(B)	Clock Access Time, $\overline{CAS}$ Latency = 3	-	5.4	-	5.4	-	6	ns	1
tAC2(B)	Clock Access Time, $\overline{CAS}$ Latency = 2	-	5.4	-	6	-	6	ns	1
tCKH	Clock High Pulse Width	2.5	-	2.5	-	3	-	ns	2
tCKL	Clock Low Pulse Width	2.5	-	2.5	-	3	-	ns	2
tCES	Clock Enable Set-up Time	1.5	-	1.5	-	2	-	ns	
tCEH	Clock Enable Hold Time	0.8	-	0.8	-	1	-	ns	
tSB	Power down mode Entry Time	0	7.5	0	7.5	0	12	ns	
tT	Transition Time (Rise and Fall)	0.5	10	0.5	10	0.5	10	ns	

1. Access time is measured at 1.4V. In AC Characteristics section, see notes.
2. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tCS	Command Setup Time	1.5	-	1.5	-	2	-	ns	
tCH	Command Hold Time	0.8	-	0.8	-	1	-	ns	
tAS	Address and Bank Select Set-up Time	1.5	-	1.5	-	2	-	ns	
tAH	Address and Bank Select Hold Time	0.8	-	0.8	-	1	-	ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	-	20	-	20	-	ns	1
tRC	Bank Cycle Time	60	-	67.5	-	70	-	ns	1
tRFC	Auto Refresh to Active/Auto Refresh	60	-	67.5	-	70	-		
tRAS	Active Command Period	45	100K	45	100K	50	100K	ns	1
tRP	Precharge Time	20	-	20	-	20	-	ns	1
tRRD	Bank to Bank Delay Time	15	-	15	-	20	-	ns	1
tCCD	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	-	1	-	1	-	CLK	

1.These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tRSC	Mode Register Set Cycle Time	2	-	2	-	2	-	CLK	1

1.These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tOH	Data Out Hold Time	-	-	-	-	2.5	-	ns	
		2.7	-	2.7	-	3	-	ns	
tLZ	Data Out to Low Impedance Time	0	-	0	-	0	-	ns	
tHZ3	Data Out to High Impedance Time	3	5.4	3	5.4	3	6	ns	1
tDQZ	DQM Data Out Disable Latency	2	-	2	-	2	-	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

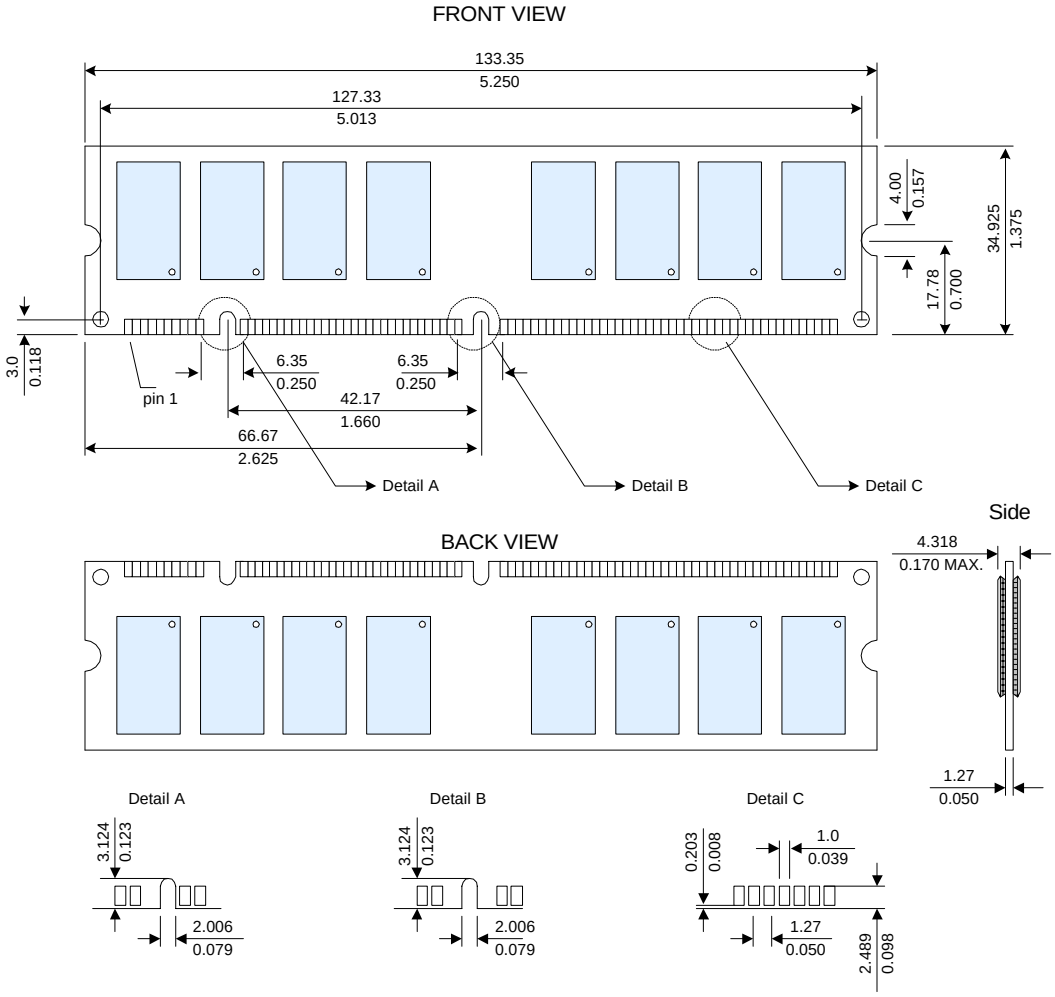
Refresh Cycle

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tREF	Refresh Period	-	64	-	64	-	64	ms	
tSREX	Self Refresh Exit Time	10	-	10	-	10	-	ns	

Write Cycle

Symbol	Parameter	- 7K		- 75B		- 8B		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
tDS	Data In Set-up Time	1.5	-	1.5	-	2	-	ns	
tDH	Data In Hold Time	0.8	-	0.8	-	1	-	ns	
tDPL	Data input to Precharge	15	-	15	-	15	-	ns	
tDAL3	Data In to Active Delay $\overline{CAS}$ Latency = 3	5	-	5	-	5	-	CLK	
tDAL2	Data In to Active Delay $\overline{CAS}$ Latency = 2	5	-	-	-	-	-	CLK	
tDQW	DQM Write Mask Latency	0	-	0	-	0	-	ns	

Package Dimensions



Note : All dimensions are typical unless otherwise stated.

Unit : Millimeters
Inches