ADDRESSABLE RELAY DRIVER — NE5090

DESCRIPTION

The NE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

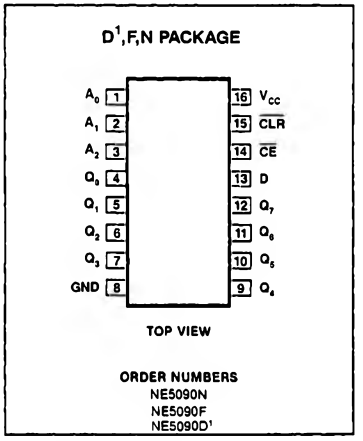
FEATURES

- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

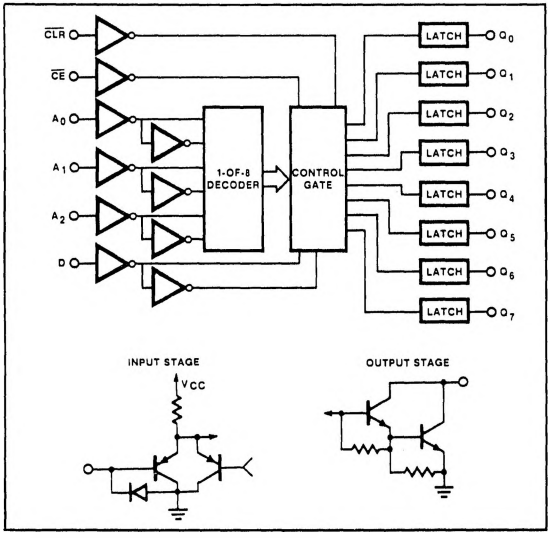
PIN CONFIGURATION



ORDER NUMBERS
NE5090N
NE5090F
NE5090D[1]

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C unless otherwise specified.

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7	V
V_{IN}	Input voltage	− 0.5 to + 15	V
V_{OUT}	Output voltage	0 to + 30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	NE5090	0 to + 70	
T_J	Junction	150	
T_{STG}	Storage	− 65 to + 150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

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PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input conditions.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75V to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified (NE5090)[2].

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH} V_{IL}	Input voltage High Low		2.0		 0.8	V
V_{OL}	Output voltage Low	I_{OL} = 150mA, T_A = 25°C Over temperature		1.05	1.30 1.50	V
I_{IH} I_{IL}	Input current High Low	$V_{IN} = V_{CC}$ V_{IN} = 0V		<1.0 −3.0	10 −250	μA
I_{OH}	Leakage current	V_{OUT} = 28V,		5	250	μA
I_{CCL} I_{CCH}	Supply current All outputs low All outputs high	V_{CC} = 5.25V NE5090		35 22	60 50	mA

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature
   NE5090 N at 9.3mW/°C above 85°C
   NE5090 F at 7.5mW/°C above 65°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C

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SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, V_{OUT} = 5V, I_{OUT} = 100mA, V_{IL} = 0.8V, V_{IH} = 2.0V

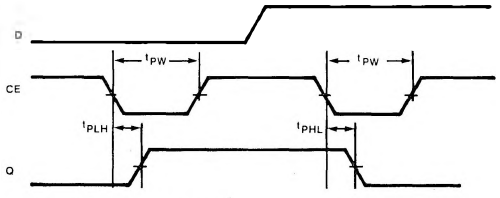
	PARAMETER	TO	FROM	Min	Typ	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay time Low to high[1] High to low[1]	Output	$\overline{CE}$		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[2] High to low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low to high[3] High to low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[4] High to low[4]	Output	$\overline{CLR}$		920	1850	ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}$[5] $t_{s(L)}$[5]		Chip enable Chip enable	High data Low data	5 10	20 30		ns
$t_{s(A)}$[6]		Chip enable	Address	0	20		ns
$t_{h(H)}$[5] $t_{H(L)}$[5]		Chip enable Chip enable	High data Low data	+ 10 + 10	0 0		ns
$t_{pw(E)}$[1]	Chip enable pulse width[1]			0	20		ns

NOTES

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

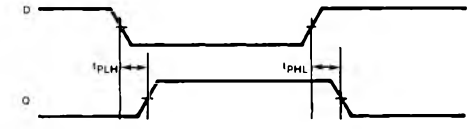
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



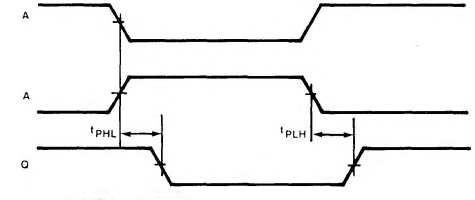
Other Inputs: $\overline{CLR}$ = H, A = Stable.

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



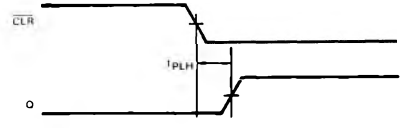
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = H, A = Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

TURN-OFF DELAY, CLEAR TO OUTPUT



Other Inputs: $\overline{CE}$ = H.

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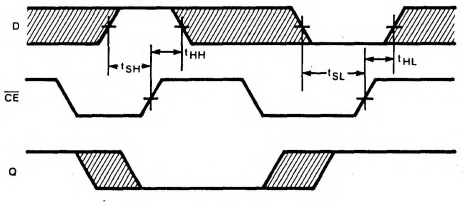
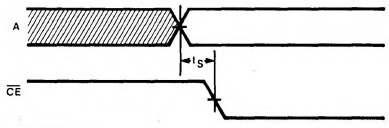
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE



Other Inputs: $\overline{CLR}$ = H, A = Stable.

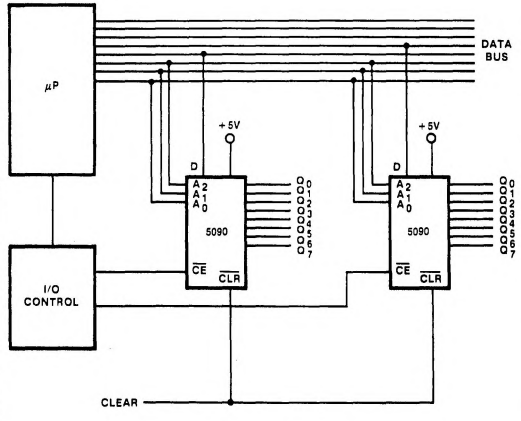
SETUP TIME, ADDRESS TO ENABLE



Other Inputs: $\overline{CLR}$ = H.

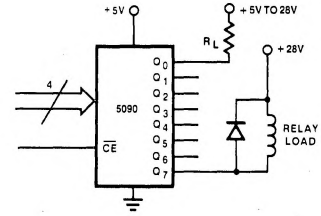
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

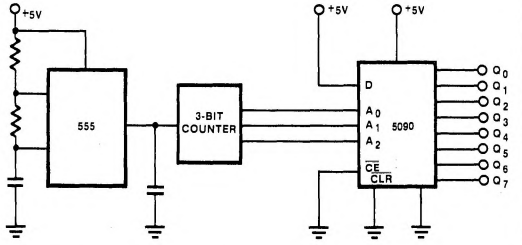


A_0, A_1, A_2, may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS



OPERATING IN DEMULTIPLEX MODE



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TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT