Signetics

NE5034
8-Bit High-Speed A/D Converter

Product Specification

Linear Products

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit analog-to-digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and 3-State buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

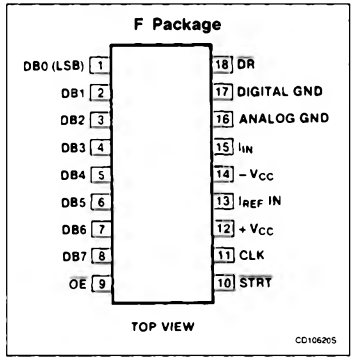
FEATURES

- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **3-State output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high-speed 8-bit building blocks**

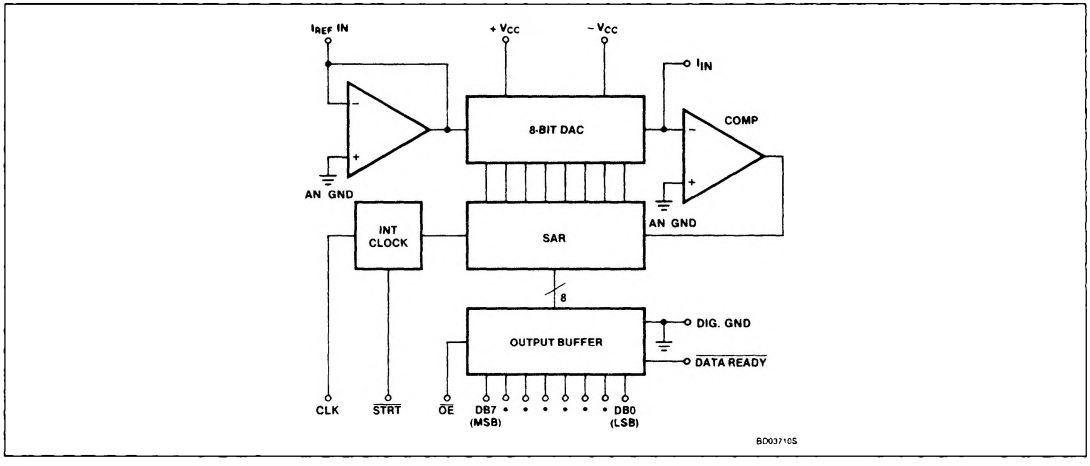
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
18-Pin Cerdip	0 to +70°C	NE5034F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to -15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
V_L	Analog GND to Digital GND Logic input voltage	1.0 -1 to $V_{CC}+$	V V
P_D	Maximum power dissipation, T_A = 25°C (still-air)[1] F package	 1500	 mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE:
1. Derate above 25°C at the following rates:
   F package at 12.0mW/°C.

DC ELECTRICAL CHARACTERISTICS

+V_{CC} = 5.0V, -V_{CC} = -12V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				± ½	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		-11.4	-12	-12.6	V
ϵ_{FS}	Full-scale gain error	I_{REF} = 1.0mA, T_A = 25°C		± 2	± 5	LSB
ϵ_{ZS}	Zero-scale offset error	I_{REF} = 1.0mA, T_A = 25°C		± 0.5	± 1	LSB
PSR	Power supply rejection[3]	I_{REF} = 1.0mA, V_{CC} = +4.75 to +5.25V, V_{CC} = -11.4 to -12.6V			± ½	LSB
V_{IH}	Logic 1 input voltage ($\overline{STRT}$ and $\overline{OE}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{STRT}$ and $\overline{OE}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{STRT}$ and $\overline{OE}$)	V_{IN} = 2.4V			20	μA
I_{IH}	Logic 1 input current ext clock	V_{IN} = 2.4V		100		μA
I_{IL}	Logic 0 input current ($\overline{STRT}$ and $\overline{OE}$)	V_{IN} = 0.4V		-20	-100	μA
I_{IL}	Logic 0 input current ext. clock	V_{IN} = 0.7V		-100		μA
V_{OL}	Logic 0 output voltage	I_{OL} = 1.6mA, $\overline{OE}$ = 0.8V			0.4	V
V_{OH}	Logic 1 output voltage	I_{OH} = 400μA, $\overline{OE}$ = 0.8V	2.4			V
I_{OZ}	Three-state leakage	$\overline{OE}$ = 2.0V, V_{OL} = 0V or 5V		± 10		μA
$I_{CC}+$	Positive supply current	V_{CC} = +5V, V_{CC} = -12V		18	36	mA
I_{CC}	Negative supply current	V_{CC} = +5V, V_{CC} = -12V		-11	-22	mA

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full-scale voltage.
3. Maximum change in full-scale.

AC ELECTRICAL CHARACTERISTICS V+ = +5V, V– = –12V, T_A = 25°C

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
	Internal clock frequency			C_L = 60pF (See Figure 1)		500		kHz
	External clock frequency						700	kHz
t_W	$\overline{STRT}$ pulse width			Clock freq. = 500kHz	400			ns
	External clock pulse width positive/negative				600			ns
t_S	Setup time[1]			See Figure 3	300			ns
t_{PD}	(Out data) propagation delay	data out	$\overline{OE}$	See Figure 2		50	200	ns
t_{PD}	(Out $\overline{DR}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
t_{PD}	(3-State) propagation delay	high impedance o/p	$\overline{OE}$	See Figure 2		60	200	ns
t_{PD}	(DB0) propagation delay	DB0	$\overline{DR}$	See Figure 3			500	ns
t_{PD}	(SDR) $\overline{STRT}$ low to $\overline{DR}$ high	data ready high	$\overline{STRT}$ low	See Figure 3		700		ns

NOTE:
1. See description of "Setup time".

TYPICAL PERFORMANCE CHARACTERISTICS

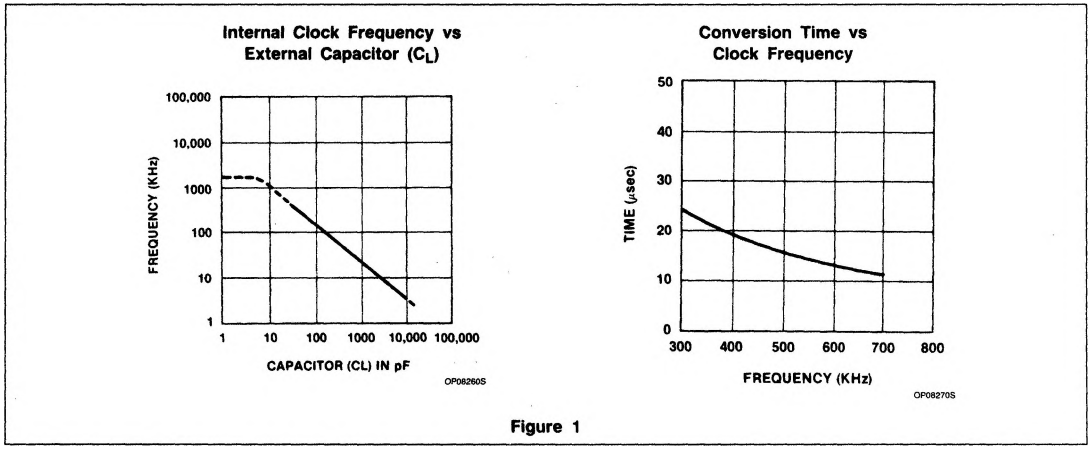
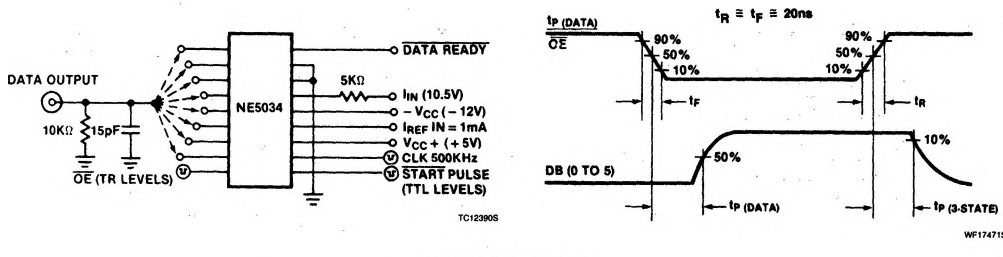
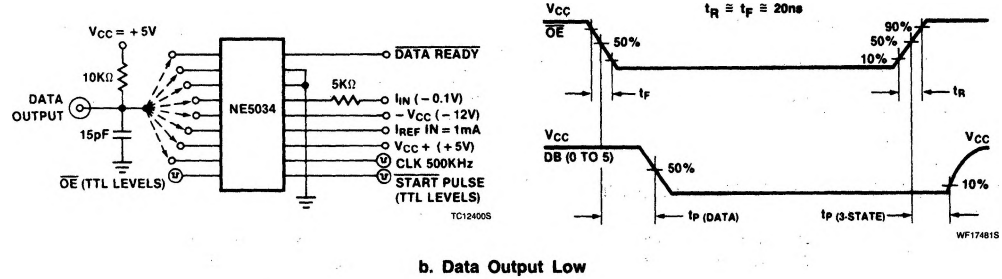


Figure 1

TEST LOAD CIRCUITS



a. Data Output High



b. Data Output Low

Figure 2

FUNCTIONAL PIN DEFINITIONS

DATA READY (DR)

This is an output pin used to indicate that a conversion is in progress. DR goes to a logic "1" when STRT is at a logic "0". At the completion of a conversion DR returns to a logic "0". There is a delay (MAX 0.5μs) from the time DR goes to "0" to the time DB0 data is valid.

DB0 – DB7

Eight 3-State data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

OE

Output enable input. When OE is at a logic "1" the data outputs assume a high impedance state. With OE at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both OE and DR are at logic "0" (see note on DR timing).

STRT

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause DR to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after STRT returns to a logic "1" (see notes on setup time required). A STRT pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation).

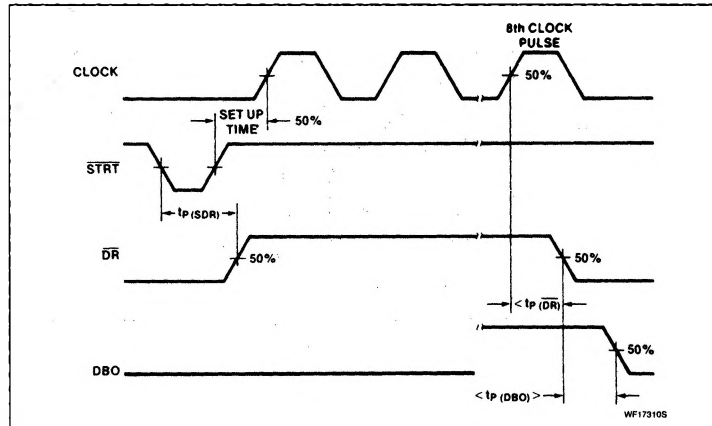


Figure 3

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type, e.g., 1N914) should be connected between STRT and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "setup" time. Applying an external TTL- or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set-up" time requirements should be noted.

8-Bit High-Speed A/D Converter NE5034

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the $\overline{STRT}$ pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± ½LSB (± 0.2%). This binary output will now remain in the SAR until another $\overline{STRT}$ pulse is applied.

During the successive-approximation sequence, the $\overline{DATA\ READY}$ signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the $\overline{OE}$ input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the $\overline{OE}$ line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the $\overline{OE}$ is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With $\overline{STRT}$ at a logic "0" the converter is reset to a condition with DB7 at a logic "1", $\overline{DR}$ at a logic "1" and DB0 – DB6 at logic "0".

Conversion starts after $\overline{STRT}$ returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive-going edge of the clock. Starting with the first positive edge after $\overline{STRT}$ returns to logic "1" (see note on "setup" time). The eighth positive-going edge makes the decision on DB0 (LSB) and also causes $\overline{DR}$ to return to a logic "0" to indicate the conversion is complete. (See note on $\overline{DR}$ timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required, the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) $\overline{DR}$ will still be at a logic "1" state.

$\overline{OE}$ can be used to 3-State the outputs even during short-cycle operation.

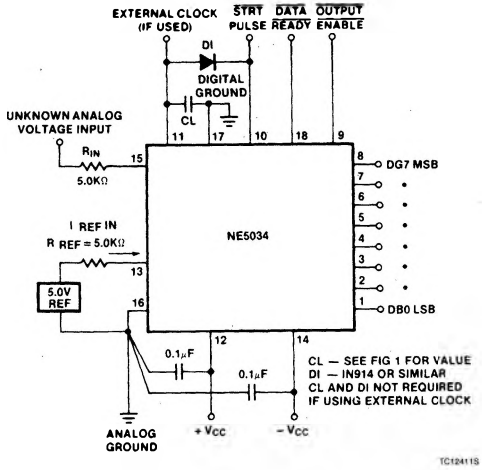


Figure 4. Basic Setup Diagram Unipolar Input Values (0 – 10V)

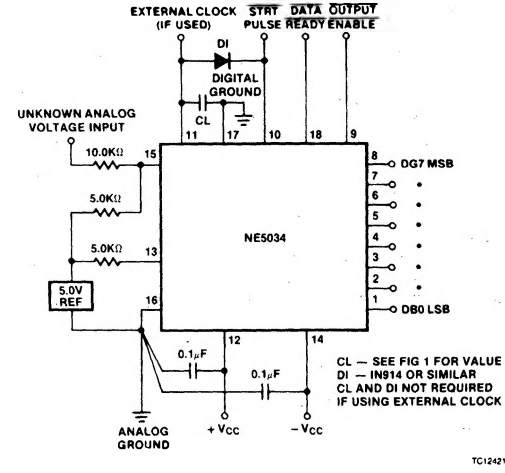


Figure 5. Basic Setup Diagram Bipolar Input Values (± 10V Range)

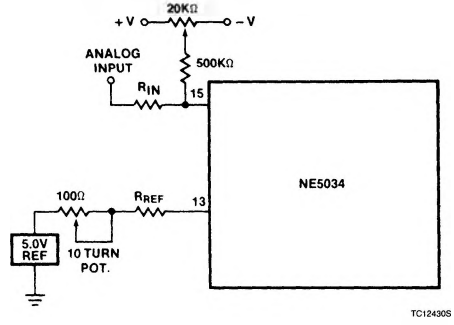


Figure 6. Suggested Zero-/Full-Scale Adjust Circuit

SETUP TIME

When using an external clock, the positive-going edge of the start pulse must be synchronized to the clock pulse. There is a "setup" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive-going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.

b) The conversion starts one clock pulse later.

c) The conversion never starts. This will be indicated by the fact that $\overline{DR}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{DR}$) TIMING

After $\overline{DR}$ returns to a logic "0", indicating a conversion is complete, there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL-SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply ½ LSB in the case of unipolar operation, or ½ LSB above — FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

FULL-SCALE (POSITIVE FULL-SCALE) CALIBRATION:

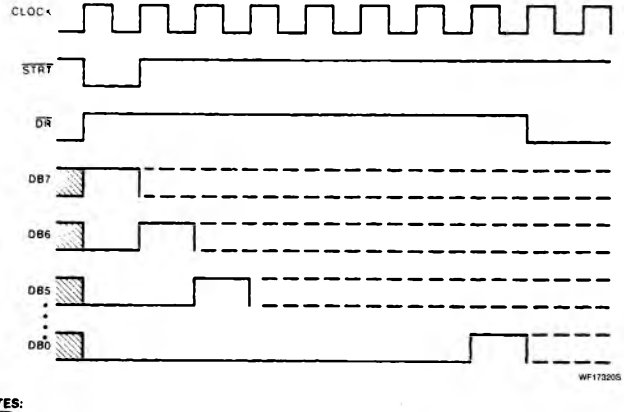
1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply full-scale minus 1½ LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to V_{REF} in (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTES:

1. Where an input of ½ LSB is called for, the voltage is equal to:
   $\frac{FS}{256}$.
2. The sequence of calibration should be:
   a. Zero offset
   b. Full-scale adjust
   c. Zero offset
   d. Full-scale adjust

OPERATING PRECAUTIONS

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.



NOTES:
1. $\overline{OE}$ = Logic '0'
2. See 'Short-Cycle' section

Figure 7. NE5034 Timing Diagram

UNIPOLAR BINARY OPERATION

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5V, is shown in Figure 4. The NE5034 can quantize full-scale ranges of 1V to 10V. It should be noted, however, that for smaller full-scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full-scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar — Binary

ANALOG INPUT 1, 2, 3	DIGITAL OUTPUT CODE	
	MSB	LSB
FS – 1 LSB	1 1 1 1 1 1 1 1	
FS – 2 LSB	1 1 1 1 1 1 1 0	
¾ FS	1 1 0 0 0 0 0 0	
½ FS + 1 LSB	1 0 0 0 0 0 0 1	
½ FS	1 0 0 0 0 0 0 0	
½ FS – 1 LSB	0 1 1 1 1 1 1 1	
¼ FS	0 1 0 0 0 0 0 0	
1 LSB	0 0 0 0 0 0 0 1	
0	0 0 0 0 0 0 0 0	

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $21_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})(FS)$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

Table 2. Bipolar — Offset Binary

ANALOG INPUT 1, 3, 4	DIGITAL OUTPUT CODE	
	MSB	LSB
+(FS – 1 LSB)	1 1 1 1 1 1 1 1	
+(FS – 2 LSB)	1 1 1 1 1 1 1 0	
+(½ FS)	1 1 0 0 0 0 0 0	
+(1 LSB)	1 0 0 0 0 0 0 1	
0	1 0 0 0 0 0 0 0	
–(1 LSB)	0 1 1 1 1 1 1 1	
–(½ FS)	0 1 0 0 0 0 0 0	
–(FS – 1 LSB)	0 0 0 0 0 0 0 1	
–FS	0 0 0 0 0 0 0 0	

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full-scale; i.e., $21_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals $(2^{-8})(FS)$.
4. "FS" is full-scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

BIPOLAR (OFFSET BINARY) OPERATION

A standard connection for a –5 to +5V or –10 to +10V bipolar operation is shown in Figure 5.