Signetics

NE5020
10-Bit μP-Compatible D/A Converter

Product Specification

Linear Products

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital-to-analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds, and addressing capability allow the NE5020 to directly interface with most microprocessor- and logic-controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

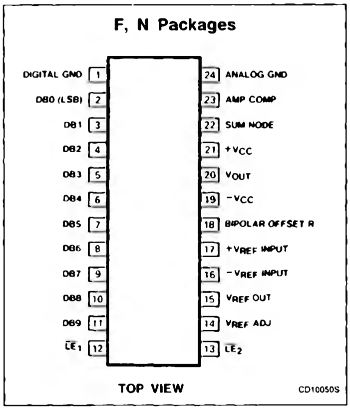
FEATURES

- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and bipolar (±5V) output range**
- **Logic bus compatible**
- **5μs settling time**

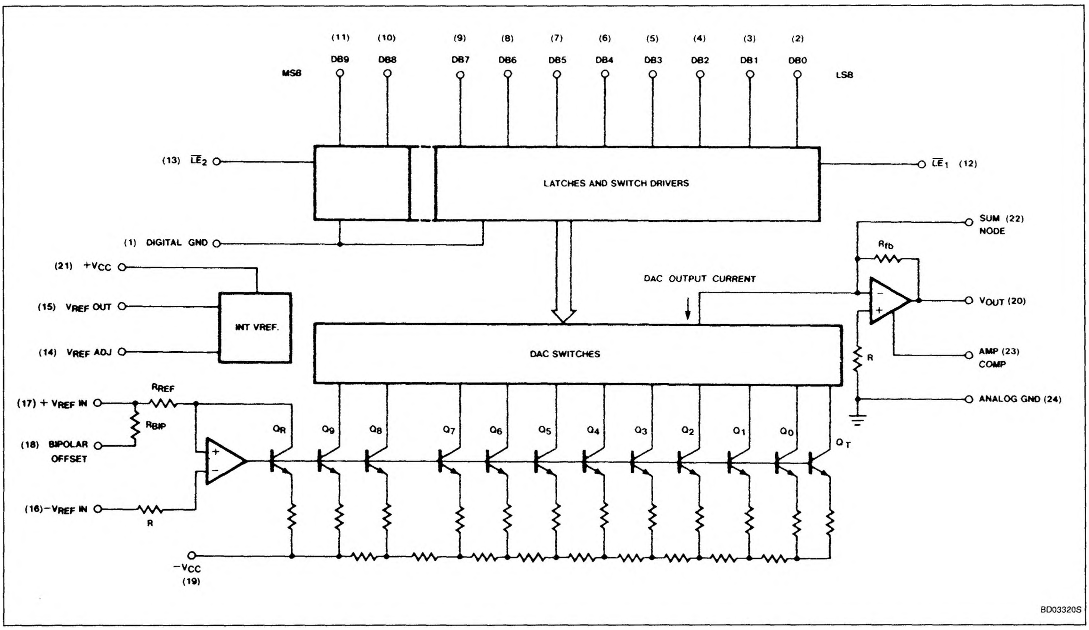
APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit analog-to-digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION



BLOCK DIAGRAM



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ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Cerdip	0 to 70°C	NE5020F
24-Pin Plastic DIP	0 t0 70°C	NE5020N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC^+}	Positive supply voltage	18	V
V_{CC^-}	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF\ IN}$	Voltage at $+V_{REF}$ input	12	V
$V_{REF\ ADJ}$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at $V_{REF\ OUT}$	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Maximum power dissipation $T_A = 25°C$, (still-air)[1] F package N package	 2150 2150	 mW mW
T_A	Operating temperature range NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 sec. max)	300	°C

NOTES:
1. Derate above 25°C at the following rates:
   F package at 17.2mW/°C.
   N package at 17.2mW/°C.

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution Monotonicity Relative accuracy				10 10 ±0.1	Bits Bits %FS
V_{CC^+} V_{CC^-}	Positive supply voltage Negative supply voltage		11.4 −11.4	15 −15	16.5 −16.5	V V
$V_{IN(1)}$ $V_{IN(0)}$	Logic "1" input voltage Logic "0" input voltage	Pin 1 = 0V Pin 1 = 0V	2.0 		 0.8	V V
$I_{IN(1)}$ $I_{IN(0)}$	Logic "1" input current Logic "0" input current	Pin 1 = 0V, $2 < V_{IN} < 18V$ Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		0.1 −2.0	10 −10	μA μA
V_{FS}	Full-scale output	Unipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	9.5		10.5	V
$+V_{FS}$	Full-scale output	Bipolar mode, $V_{REF} = 5.000V$, all bits high, $T_A = 25°C$	4.75		5.25	V
$-V_{FS}$	Negative full-scale	Bipolar mode, $V_{REF} = 5.000V$, all bits low, $T_A = 25°C$	−5.25		−4.75	V

NOTE:
1. Refer to Figure 1.

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0 \leq T_A \leq 70°C$, unless otherwise specified.[1] Typical values are specified at 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{ZS}	Zero-scale output	Unipolar mode, V_{REF} = 5.000V, all bits low, T_A = 25°C	−30		+30	mV
I_{OS}	Output short-circuit current	T_A = 25°C V_{OUT} = 0V		±15	±40	mA
$PSR+_{(OUT)}$ $PSR-_{(OUT)}$	Output power supply rejection (+) Output power supply rejection (−)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, external $V_{REF\ IN}$ = 5.000V V+ = 15V, −13.5V ≤ V− ≤ −16.5V, external $V_{REF\ IN}$ = 5.000V		0.001 0.001	0.01 0.01	%FS/%VS %FS/%VS
TC_{FS} TC_{ZS}	Full-scale temperature coefficient Zero-scale temperature coefficient	$V_{REF\ IN}$ = 5.000V		20 5		ppmFS/°C ppmFS/°C
I_{REF}[2] $I_{REF\ SC}$	Reference output current Reference short circuit current	T_A = 25°C $V_{REF\ OUT}$ = 0V		 15	3 30	mA mA
$PSR+_{REF}$ $PSR-_{REF}$	Reference power supply rejection (+) Reference power supply rejection (−)	V− = −15V, 13.5V ≤ V+ ≤ 16.5V, I_{REF} = 1.0mA V+ = 15V, −13.5V ≤ V− ≤ 16.5V,		.003 .003	.01 .01	%VR/%VS %VR/%VS
V_{REF} TC_{REF}	Reference voltage Reference voltage temperature coefficient	I_{REF} = 1.0mA, T_A = 25°C I_{REF} = 1.0mA	4.9	5.0 60	5.25	V ppm/°C
Z_{IN}	DAC $V_{REF\ IN}$ input impedance	I_{REF} = 1.0mA		5.0		kΩ
$I_{CC}+$ $I_{CC}-$	Positive supply current Negative supply current	$V_{CC}+$ = 15V $V_{CC}-$ = −15V		7 −10	14 −15	mA mA
P_D	Power dissipation	I_{REF} = 1.0mA, V_{CC} = ±15V		255	435	mW

NOTE:
1. Refer to Figure 1.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[1] V_{CC} = ±15V, T_A = 25°C.

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{SLH}	Settling time	±½ LSB	Input	All bits low-to-high[2]		5		μs
t_{SHL}	Settling time	±½ LSB	Input	All bits high-to-low[3]		5		μs
t_{PLH}	Propagation delay	Output	Input	All bits switched low-to-high[2]		30		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched high-to-low[3]		150		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change[2,3]		150		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition[4]		300		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition[5]		150		ns
t_S	Set-up time	$\overline{LE}$	Input	[1,6]	100			ns
t_H	Hold time	Input	$\overline{LE}$	[1,6]	50			ns
t_{PW}	Latch enable pulse width			[1,6]	150			ns

NOTES:
1. Refer to Figure 2.
2. See Figure 5.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.

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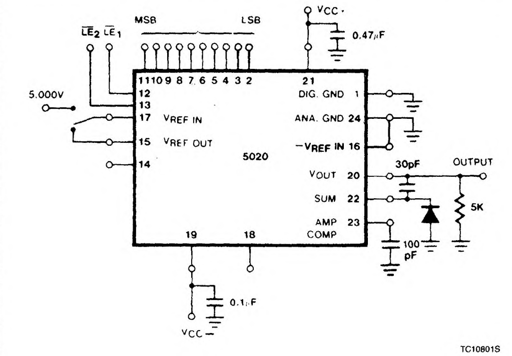

Figure 1. DC Parametric Test Configuration

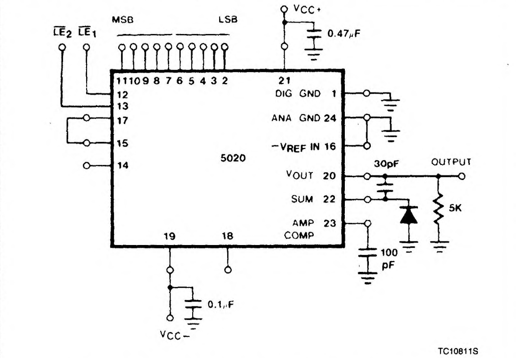

Figure 2. AC Parametric Test Configuration

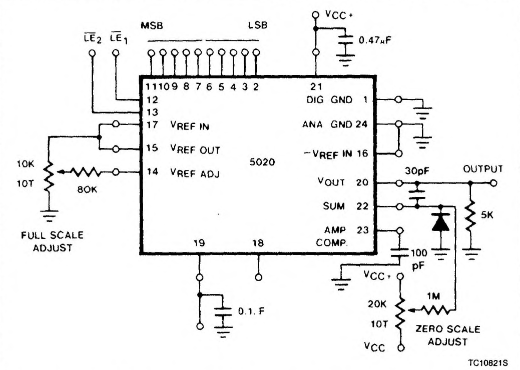

Figure 3. Full-/Zero-Scale Adjust — Unipolar Output (0 - 10V)

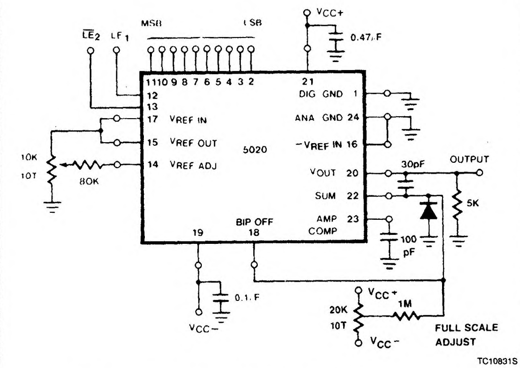

Figure 4. Bipolar Output Operation (−5 to +5V)

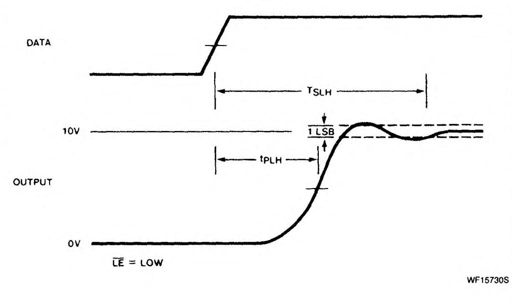

Figure 5. Settling Time and Propagation Delay, Low-to-High Data

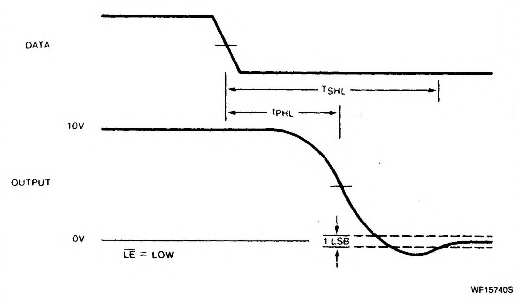

Figure 6. Settling Time and Propagation Delay, High-to-Low Data

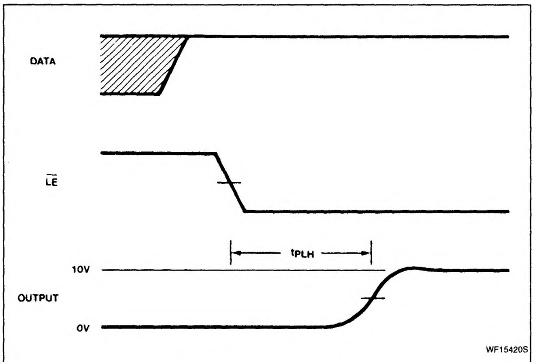

Figure 7. Propagation Delay, Latch Enable to Output

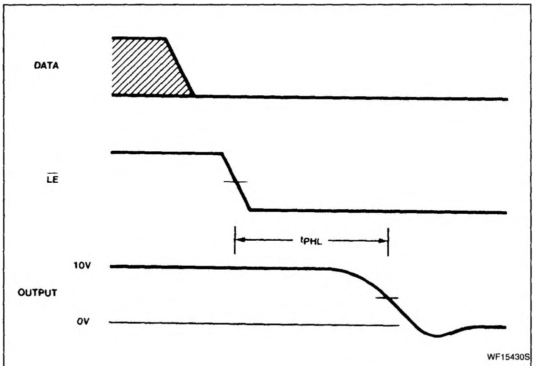

Figure 8. Propagation Delay, Latch Enable to Output

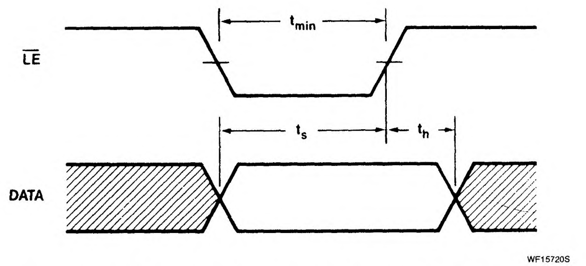

Figure 9. Latch Enable Pulse Width, Setup and Hold Times

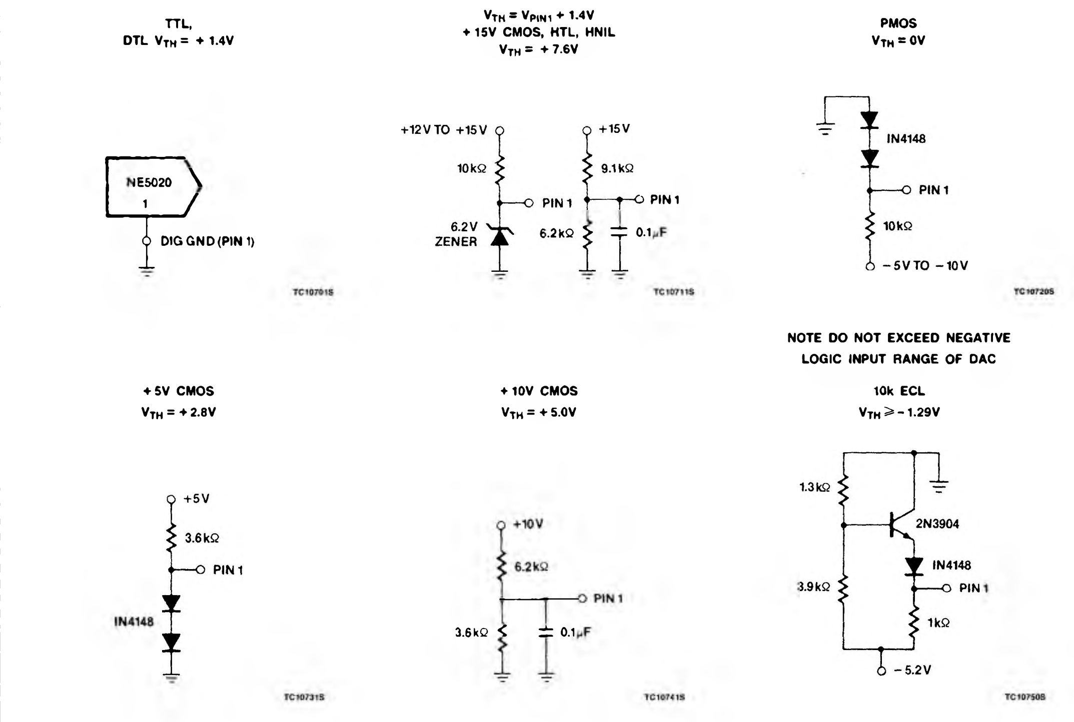

Figure 10

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage in addition to the basic DAC components (see Block Diagram).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_ϕ). Both the latch enable ports ($\overline{LE}$) and the data inputs are static- and threshold-sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low static (Logic '0'), the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on

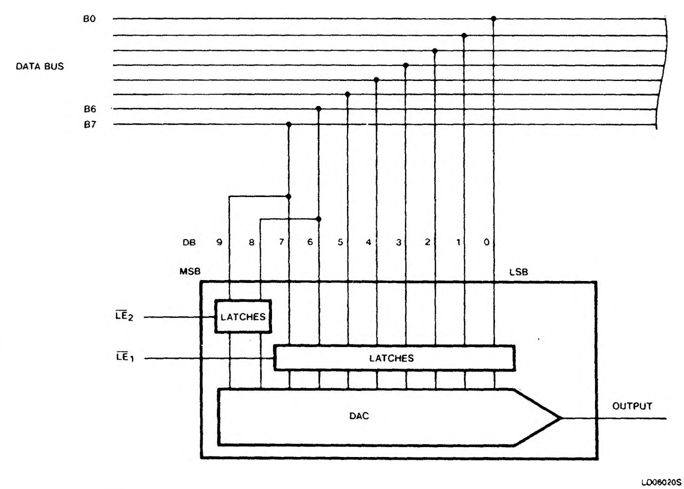

Figure 11. NE5020 μP Interface 8-Bit Data Bus Example

which $\overline{LE}$ goes high) 'memorizes' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (0.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4V with respect to the voltage level on the digital ground pin (Pin 1). Figure 10 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus-oriented system, the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 9 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50ns after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8-bit data bus (see Figure 11). Data for the two MSBs is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSBs of data are transferred into the DAC. With $\overline{LE}_1$ returning high, the loading of 10-bit data word from an 8-bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16-bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8-bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 12 shows the circuit configuration.

After preloading (via $\overline{LE}$ preload) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSBs and the two MSBs are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

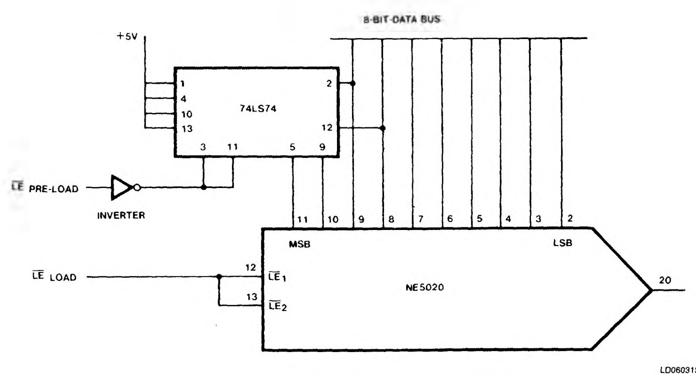

Figure 12. Preloading the 2 MSBs to Provide a Single-Step Output

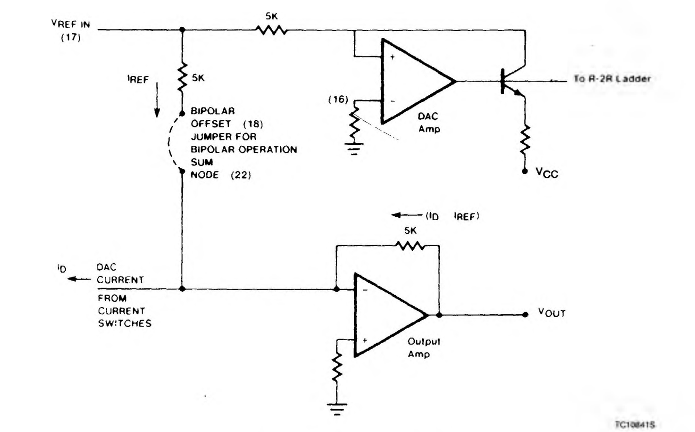

Figure 13. Bipolar Output

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long-term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5V reference output. Providing a $V_{REF\ ADJ}$ (Pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in Figure 15 performs not only V_{REF} adjustment, but also full-scale output adjust. Notice that the $V_{REF\ ADJ}$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF\ ADJ}$ pin and observing good layout practices.

The $V_{REF\ OUT}$ node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier be used.

Input Amplifier

The DAC reference amplifier is a high gain internally-compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

The Block Diagram details the input reference amplifier and current ladder. The voltage-to-current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5V V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA, and so on. These current values act as current

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sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}} \left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024} \right).$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/μs and source impedances at the $V_{REF\ INPUT}$ greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF\ INPUT}$ pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF\ INPUT}$ is grounded and the negative reference is tied directly to the $-V_{REF\ INPUT}$. The $-V_{REF\ INPUT}$ contains a 5kΩ resistor that matches a like resistor in the $+V_{REF\ INPUT}$ to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on-chip output op amp to eliminate the need for additional external active circuits. Its two-stage design with feed-forward compensation allows it to slew at 15V/μs and settle to within ± ½LSB in 5μs. These times are typical when driving the rated loads of $R_L \geqslant 5k$ and $C_L \leqslant 50pF$ with recommended values of C_{FF} = 1nF and C_{FB} = 30pF. Typical input offset voltages of 5mV and 50kΩ open-loop gain insure that an accurate current-to-voltage conversion is performed when using the on-chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ± 15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short-circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5V to obtain −5V to +5V output voltage range operation. This is accomplished by shorting

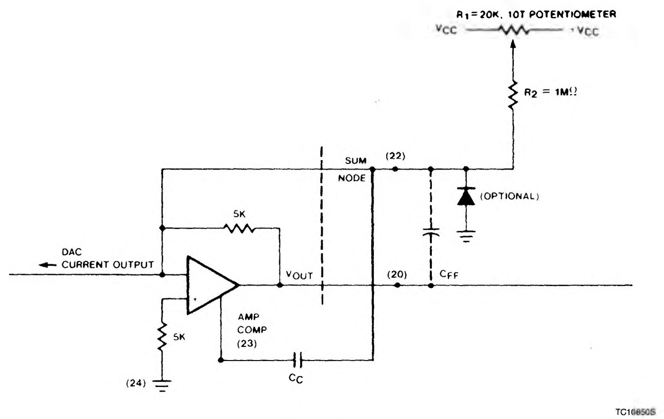

Figure 14. Zero-Scale Adjustment

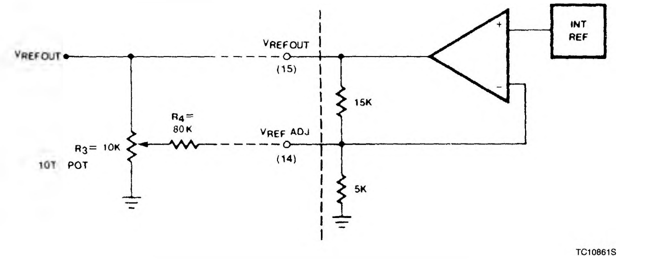

Figure 15. Reference Adjust Circuit

Pins 18 and 22 (see Figure 13). This connection produces a current equal to (V_{REFIN} − SUM NODE) ÷ R_{BIP} (1mA nominal), which is injected into the sum node. Since full-scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5kΩ = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum node and V_{OUT} = −(5kΩ) (1mA) = −5V. Zero-scale adjust and full-scale adjust are performed as described below, noting that full-scale voltage is now approximately +5V. Zero-scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = −5.0V with all bits off.

Zero-Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in Figure 14. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000V in the unipolar mode or −5.000V in the bipolar mode (see bipolar section) accomplishes this trim.

Full-Scale Adjustment

A recommended full-scale adjustment circuit, when using the internal voltage reference, is shown in Figure 15. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accuracy of full-scale is of low importance when compared to the other system accuracy factors this adjustment circuit is optional.

As resistors R_{REF}, R_{FB}, and R_{BIP} shown in the Block Diagram are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full-scale (or gain) error is less than ±0.3% of ideal full-scale value.