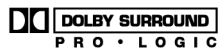


DATA SHEET

MSP 34x2G Multistandard Sound Processor Family with Dolby Pro Logic



Edition June 3, 2003
6251-520-1DS

 **MICRONAS**

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Multistandard Sound Processor Family with Dolby Pro Logic

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x2G version B3 and following versions.

1. Introduction

The MSP 34x2G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip.

The family's latest member, the MSP 34x2G has all functions of the MSP 34x0G with the addition of Dolby Pro Logic and Virtual Dolby Surround sound processing (See License Notice on page 6). The MSP 34x2G forms a superset of the functions of the MSP 34x1G, which contains the virtualizer algorithms but does not contain any multi-channel processing.

Additional output pins DACM_C and DACM_S have been defined which deliver the Dolby Pro Logic processed Center and Surround channels. When DACM_C and DACM_S are active, the headphone outputs DACA_L and DACA_R are muted and vice versa. Simultaneous processing of Headphone signals and Dolby Pro Logic is not possible.

Surround sound can be reproduced to a certain extent with only two loudspeakers. The MSP 34x2G includes a Micronas virtualizer algorithm which has been approved by the Dolby¹⁾ Laboratories for compliance with the "Virtual Dolby Surround" technology. This algorithm is called 3D-PANORAMA[®] and enables convincing acoustical sensations. Virtual Dolby Surround can be processed together with headphone signals.

The ICs are produced in submicron CMOS technology. The MSP 34x2G is available in the following packages: PMQFP80-11, PMQFP64-2, and PSDIP64-1.

1.1. Features

- All MSP 34x0G standard features
- All MSP 34x1G standard features:
 - the 3D-PANORAMA[®] virtualizer algorithm (to be used for Virtual Dolby Surround)
 - the PANORAMA virtualizer algorithm
 - Noise Generator
- Virtualizer able to work with 2 or 3 front loudspeakers
- Dolby Pro Logic processing
- Various other multichannel sound modes
- Additional pins for Center and Surround channels
- Pin and software compatible to MSP 34x0G

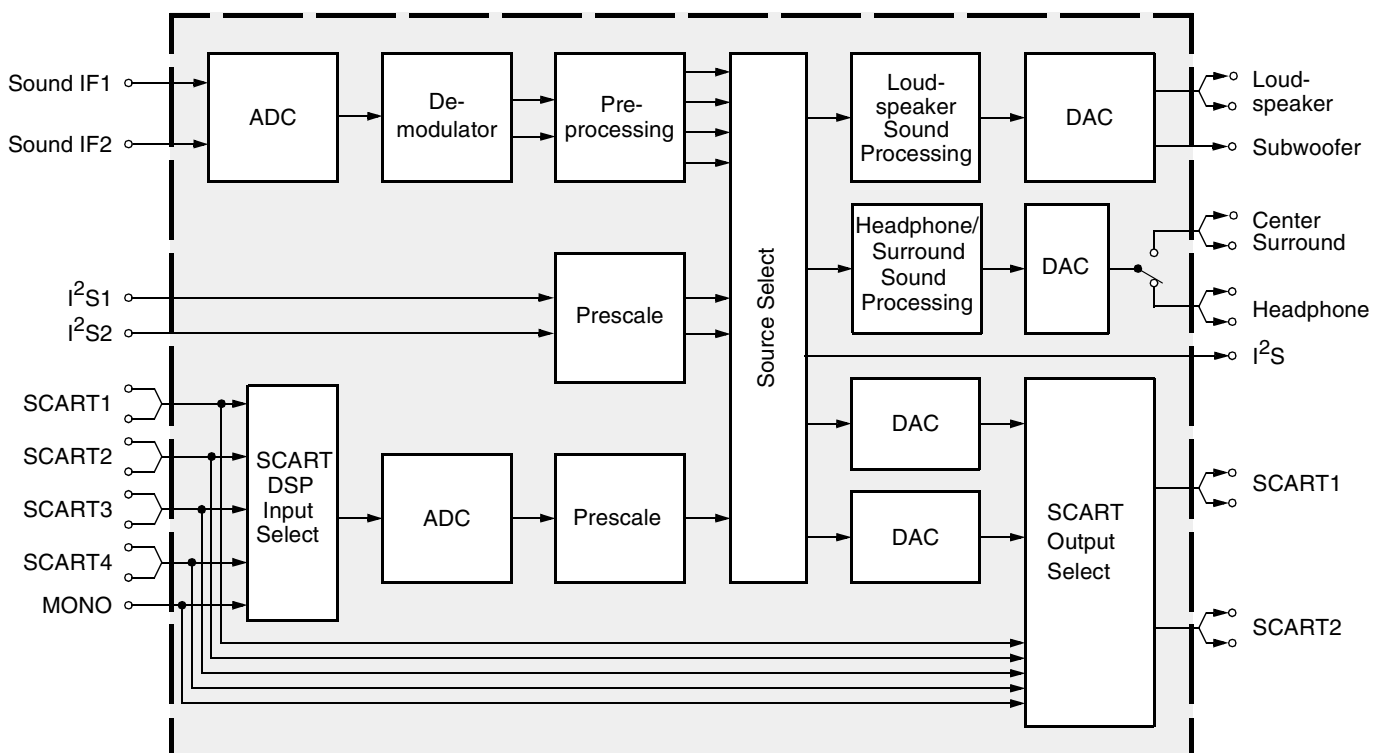


Fig. 1–1: Block diagram of the MSP 34x2G

1.2. Features of the MSP 34x2G Family

| Feature | 3402 | 3412 | 3422 | 3442 | 3452 |
|--|------|------|------|------|------|
| Dolby Pro Logic | X | X | X | X | X |
| Virtual Dolby Surround Processing with 3D-PANORAMA virtualizer | X | X | X | X | X |
| PANORAMA virtualizer algorithm | X | X | X | X | X |
| Standard Selection with single I ² C transmission | X | X | X | X | X |
| Automatic Standard Detection of terrestrial TV standards/Automatic Carrier Mute function | X | X | X | X | X |
| Automatic Sound Selection (mono/stereo/bilingual) | X | X | X | X | X |
| Two selectable sound IF (SIF) inputs | X | X | X | X | X |
| Interrupt output programmable (indicating status change) | X | X | X | X | X |
| Loudspeaker / Headphone channel with volume, balance, bass, treble, loudness | X | X | X | X | X |
| AVC: Automatic Volume Correction | X | X | X | X | X |
| Subwoofer output with programmable low-pass and complementary high-pass filter | X | X | X | X | X |
| Micronas BASS (MB) and 5-band graphic equalizer for loudspeaker channel | X | X | X | X | X |
| Spatial effect for loudspeaker channel | X | X | X | X | X |
| Four Stereo SCART (line) inputs, one Mono input; two Stereo SCART outputs | X | X | X | X | X |
| Complete SCART in/out switching matrix | X | X | X | X | X |
| Two I ² S inputs; one I ² S output | X | X | X | X | X |
| All analog Mono sound carriers including AM-SECAM L | X | X | X | X | X |
| All analog FM-Stereo A2 and satellite standards | X | X | x | x | X |
| Simultaneous demodulation of (very) high-deviation FM-Mono and NICAM | | X | | | X |
| Adaptive deemphasis for satellite (Wegener-Panda, acc. to ASTRA specification) | X | X | | | X |
| ASTRA Digital Radio (ADR) together with DRP 3510A | X | X | | | X |
| All NICAM standards | | X | | | X |
| Demodulation of the BTSC multiplex signal and the SAP channel | | | X | X | X |
| Alignment free digital DBX noise reduction for BTSC Stereo and SAP | | | | X | X |
| Alignment free digital Micronas Noise Reduction (MNR) for BTSC Stereo and SAP | | | X | | |
| BTSC stereo separation (MSP 3422/42G also EIA-J) significantly better than spec. | | | X | X | X |
| SAP and stereo detection for BTSC system | | | X | X | X |
| Korean FM-Stereo A2 standard | X | X | X | X | X |
| Alignment-free Japanese standard EIA-J | | | X | X | X |
| Demodulation of the FM-Radio multiplex signal | | | X | X | X |

1.3. MSP 34x2G Version List

| Version | Status | Description |
|-----------|---------------|--|
| MSP 3402G | not confirmed | FM Stereo (A2) Version |
| MSP 3412G | available | NICAM and FM Stereo (A2) Version |
| MSP 3422G | not confirmed | NTSC Version (A2 Korea, BTSC with Micronas Noise Reduction (MNR), and Japanese EIA-J system) |
| MSP 3442G | not confirmed | NTSC Version (A2 Korea, BTSC with DBX noise reduction, and Japanese EIA-J system) |
| MSP 3452G | available | Global Version (all sound standards) |

1.4. MSP 34x2G Versions and their Application Fields

Table 1–1 provides an overview of TV sound standards that can be processed by the MSP 34x2G family. In addition, the MSP 34x2G is able to handle the FM-Radio standard. With the MSP 34x2G, a complete

multimedia receiver covering all TV sound standards together with terrestrial/cable and satellite radio sound can be built; even ASTRA Digital Radio can be processed (with a DRP 3510A coprocessor).

Table 1–1: TV Stereo Sound Standards covered by the MSP 34x2G IC Family (details see Appendix A)

| MSP Version | TV-System | Position of Sound Carrier /MHz | Sound Modulation | Color System | Broadcast e.g. in: |
|-------------|-----------|--------------------------------|--|--------------|------------------------|
| 3402 | B/G | 5.5/5.7421875 | FM-Stereo (A2) | PAL | Germany |
| | | 5.5/5.85 | FM-Mono/NICAM | PAL | Scandinavia, Spain |
| | L | 6.5/5.85 | AM-Mono/NICAM | SECAM-L | France |
| | I | 6.0/6.552 | FM-Mono/NICAM | PAL | UK, Hong Kong |
| 3402 | D/K | 6.5/6.2578125 | FM-Stereo (A2, D/K1) | SECAM-East | Slovak. Rep. |
| | | 6.5/6.7421875 | FM-Stereo (A2, D/K2) | PAL | currently no broadcast |
| | | 6.5/5.7421875 | FM-Stereo (A2, D/K3) | SECAM-East | Poland |
| | | 6.5/5.85 | FM-Mono/NICAM (D/K, NICAM) | PAL | China, Hungary |
| 3402 | Satellite | 6.5 | FM-Mono | PAL | Europe Sat. ASTRA |
| | | 7.02/7.2 | FM-Stereo | | |
| | | 7.38/7.56 etc. | ASTRA Digital Radio (ADR) with DRP 3510A | | |
| | | | | | |
| 3422, 3442 | M/N | 4.5/4.724212 | FM-Stereo (A2) | NTSC | Korea |
| | | 4.5 | FM-FM (EIA-J) | NTSC | Japan |
| | | 4.5 | BTSC-Stereo + SAP | NTSC, PAL | USA, Argentina |
| | FM-Radio | 10.7 | FM-Stereo Radio | | USA, Europe |

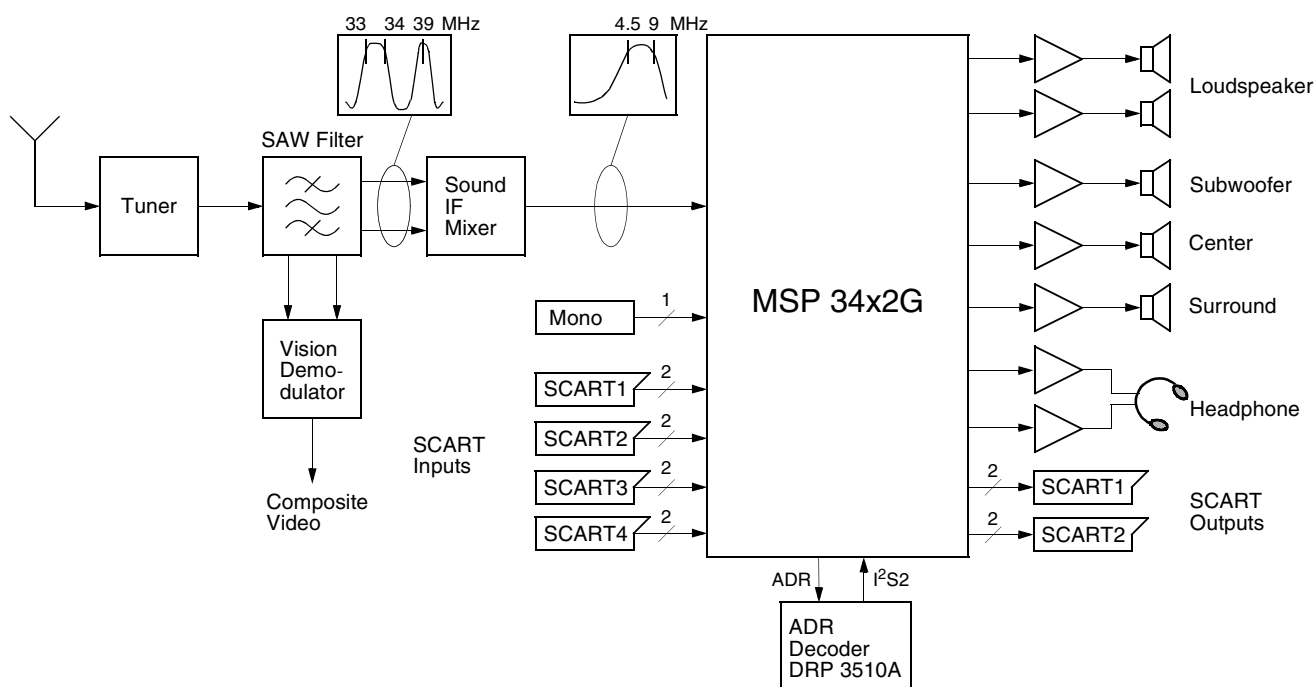


Fig. 1–2: Typical MSP 34x2G application

2. Functional Description

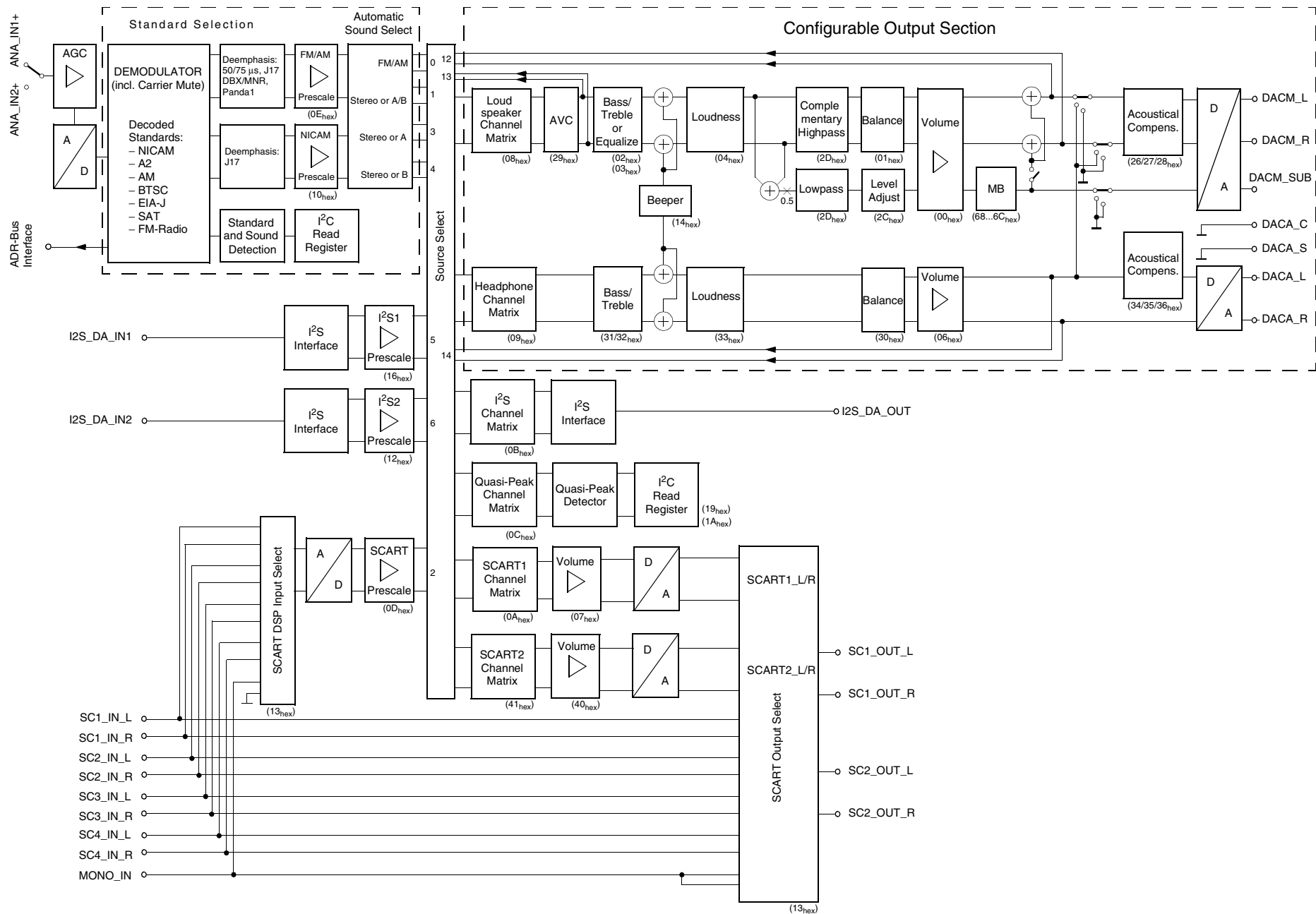


Fig. 2–1: Signal flow block diagram of the MSP 34x2G

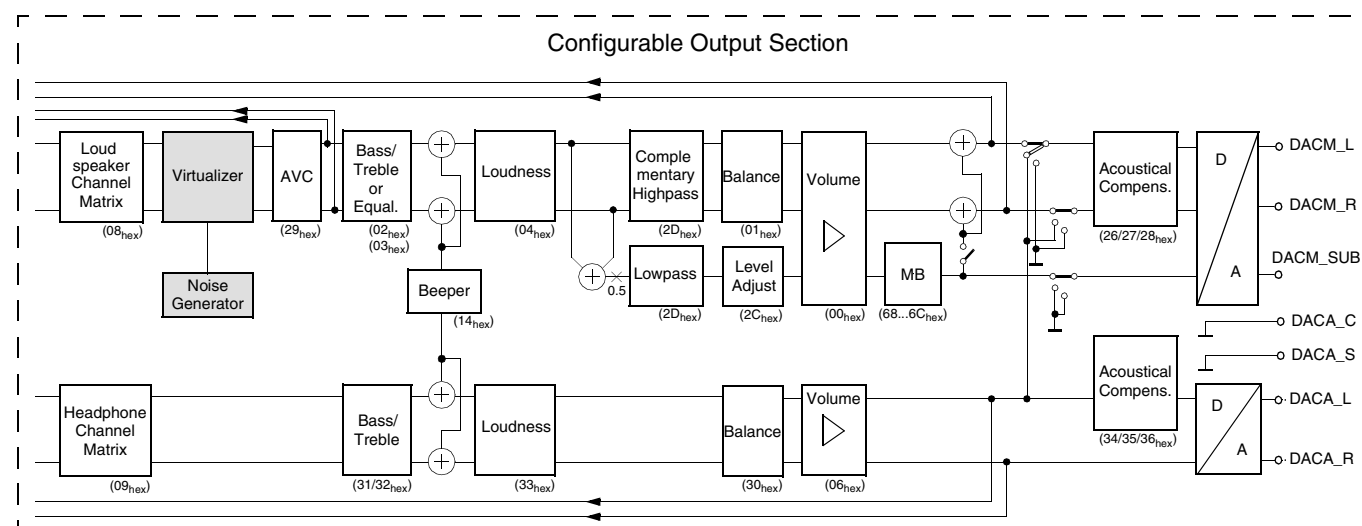


Fig. 2-2: Output section in virtual mode: Output Configuration (register 48_{hex}) = 0100_{hex}

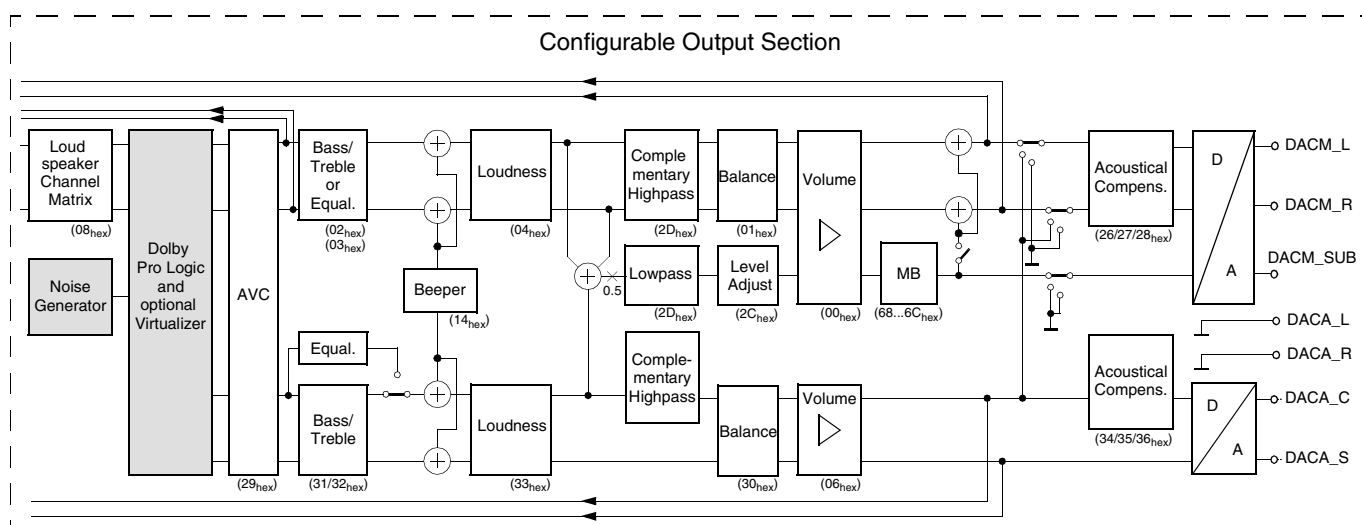


Fig. 2-3: Output section with multi-channel surround: Output Configuration (register 48_{hex}) = 8200_{hex}

2.1. Architecture of the MSP 34x2G Family

The block diagrams in Fig. 2–1, Fig. 2–2, and Fig. 2–3 show the signal flow in the MSP 34x2G in three modes that can be set in the Output Configuration register.

- Standard mode (see Fig. 2–1).
The IC is compatible to the MSP 34x0G family.
- Virtual mode (see Fig. 2–2).
The IC is compatible to the Virtual Dolby MSP 34x1G family.
- Multi-channel mode (see Fig. 2–3).

The three block diagrams show the features of the MSP 34x2G family member.

Other members of the MSP 34x2G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3412G and MSP 3452G.

2.2. Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+, ANA_IN2+, and ANA_IN– offer the possibility to connect two different sound IF (SIF) sources to the MSP 34x2G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filters formed by the coupling capacitors at pins ANA_IN1+ and ANA_IN2+ see Section 7.2. “Application Circuit” on page 112 are sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 34x2G is able to demodulate all TV-sound standards worldwide including the digital NICAM system. Depending on the MSP 34x2G version, the following demodulation modes can be performed:

A2 Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L–R)-carrier and detection of the SAP subcarrier. Processing of DBX noise reduction or Micronas Noise Reduction (MNR).

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP subcarrier. Processing of DBX noise reduction or Micronas Noise Reduction (MNR).

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L–R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L–R)-carrier.

The demodulator blocks of all MSP 34x2G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x2G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x2G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x2G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STANDARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically set by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I²C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono compatible standards (standards that have the same FM mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, D/K3-FM and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x2G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2–1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (see Fig. 2–4). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- **“FM/AM” channel:** Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- **“Stereo or A/B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

- **“Stereo or A” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- **“Stereo or B” channel:** Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2–4 and Table 2–2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the second FM carrier, the L–R signal of the MPX carrier, or the SAP signal.

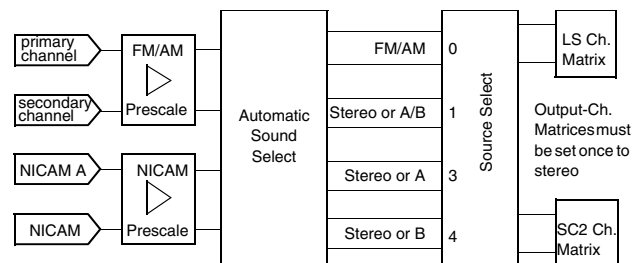


Fig. 2–4: Source channel assignment of demodulated signals in Automatic Sound Select Mode

2.2.5. Manual Mode

Fig. 2–5 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. “Demodulator Source Channels in Manual Mode” on page 109.

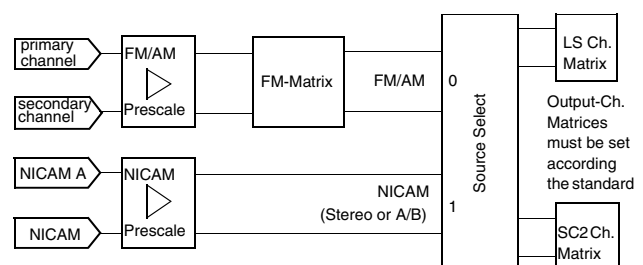


Fig. 2–5: Source channel assignment of demodulated signals in Manual Mode

Table 2–1: Performed actions of the Automatic Sound Selection

| Selected TV Sound Standard | Performed Actions |
|---|--|
| B/G-FM, D/K-FM, M-Korea, and M-Japan | Evaluation of the identification signal and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2. |
| B/G-NICAM, L-NICAM, I-NICAM, and D/K-NICAM | <p>Evaluation of NICAM-C-bits and automatic switching to mono, stereo, or bilingual. Preparing four demodulator source channels according to Table 2–2.</p> <p>In case of bad or no NICAM reception, the MSP switches automatically to FM/AM mono and switches back to NICAM if possible. A hysteresis prevents periodical switching.</p> |
| B/G-FM, B/G-NICAM or D/K1-FM, D/K2-FM, D/K3-FM, and D/K-NICAM | <p>Automatic searching for stereo/bilingual-identification in case of mono transmission. Automatic and non-audible changes between Dual-FM and FM-NICAM standards while listening to the basic FM-Mono sound carrier.</p> <p>Example: If starting with B/G-FM-Stereo, there will be a periodical alternation to B/G-NICAM in the absence of FM-Stereo/Bilingual or NICAM-identification. Once an identification is detected, the MSP keeps the corresponding standard.</p> |
| BTSC-STEREO, FM Radio | Evaluation of the pilot signal and automatic switching to mono or stereo. Preparing four demodulator source channels according to Table 2–2. Detection of the SAP carrier. |
| BTSC-SAP | In the absence of SAP, the MSP switches to BTSC-Stereo if available. If SAP is detected, the MSP switches automatically to SAP (see Table 2–2). |

Table 2–2: Sound modes for the demodulator source channels with Automatic Sound Select

| | | | Source Channels in Automatic Sound Select Mode | | | |
|---|---|--|--|-------------------------------------|-----------------------------------|-----------------------------------|
| Broadcasted Sound Standard | Selected MSP Standard Code ³⁾ | Broadcasted Sound Mode | FM/AM (source select: 0) | Stereo or A/B (source select: 1) | Stereo or A (source select: 3) | Stereo or B (source select: 4) |
| M-Korea B/G-FM D/K-FM M-Japan | 02 03, 08 ¹⁾ 04, 05, 07, 0B ¹⁾ 30 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL: Languages A and B | Left = A Right = B | Left = A Right = B | A | B |
| B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM) | 08, 03 ²⁾ 09 0A 0B, 04 ²⁾ , 05 ²⁾ 0C, 0D | NICAM not available or error rate too high | analog Mono | analog Mono | analog Mono | analog Mono |
| | | MONO | analog Mono | NICAM Mono | NICAM Mono | NICAM Mono |
| | | STEREO | analog Mono | NICAM Stereo | NICAM Stereo | NICAM Stereo |
| | | BILINGUAL: Languages A and B | analog Mono | Left = NICAM A Right = NICAM B | NICAM A | NICAM B |
| BTSC | 20, 21 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |
| | 20 | MONO+SAP | Mono | Mono | Mono | Mono |
| | | STEREO+SAP | Stereo | Stereo | Stereo | Stereo |
| | 21 | MONO+SAP | Left = Mono Right = SAP | Left = Mono Right = SAP | Mono | SAP |
| | | STEREO+SAP | Left = Mono Right = SAP | Left = Mono Right = SAP | Mono | SAP |
| FM Radio | 40 | MONO | Mono | Mono | Mono | Mono |
| | | STEREO | Stereo | Stereo | Stereo | Stereo |

¹⁾ The Automatic Sound Select process will automatically switch to the mono compatible analog standard.

²⁾ The Automatic Sound Select process will automatically switch to the mono compatible digital standard.

³⁾ The MSP Standard Codes are defined in Table 3–7 on page 29.

2.3. Preprocessing for SCART and I²S Input Signals

The SCART and I²S inputs need only be adjusted in level by means of the SCART and I²S prescale registers.

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels, SCART, or I²S input) to the desired output channels (loudspeaker, headphone, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.5. Audio Baseband Processing

2.5.1. SRS WOW (optional)



License Notice: SRS, SRS WOW, and the SRS Logo are trademarks of SRS Labs, Inc. A license from SRS Labs, Inc. is required before an SRS-version of the MSP 34x2G can be purchased.

SRS Labs' WOW technology enlarges the sound image field and improves the bass performance of television speakers. Manufacturers can save costs by licensing WOW while utilizing smaller speakers and still provide a higher quality audio experience.

WOW consists of three sections:

- Clarity Improvement,
- 3D-Audio (SRS, Sound Retrieval System), and
- Bass Enhancement (TruBass).



Key features of WOW include:

- Wider and taller sound image field
- Larger sweet spot
- Deep, rich bass tones
- Quality improvements to audio listening experience
- Improved clarity of speech

All MSP 34x2G are shipped without SRS except otherwise ordered. When an SRS-version of MSP 34x2G is ordered, it carries a special marking on the chip for identification. The SRS WOW functionality must be enabled by writing a "license key" into the MSP 34x2G. For information on how to obtain this license key from Micronas, please contact your Micronas sales representative.

2.5.2. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low-level inputs. The decay time is programmable by means of the AVC register (see page 39).

For input signals ranging from –24 dBr to 0 dBr, the AVC maintains an adjustable output level between –18 dBr and –3 dBr. Fig. 2–6 shows the AVC output level versus its input level with an output level of –18 dBr, maximum attenuation 24 dB and maximum gain of 6 dB. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

- SCART input/output 0 dBr = 2.0 V_{rms}
- Loudspeaker and Aux output 0 dBr = 1.4 V_{rms}

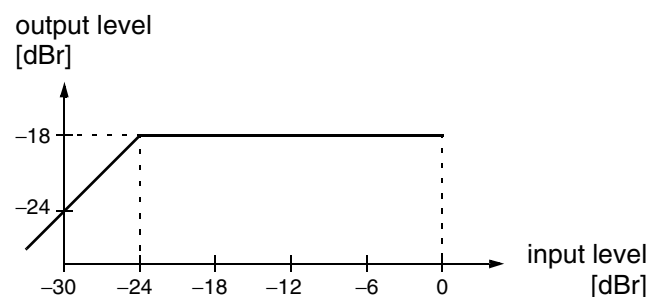


Fig. 2–6: Simplified AVC characteristics

2.5.3. Loudspeaker and Headphone Outputs

The following baseband features are implemented in the loudspeaker and headphone output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker and headphone channel. The loudspeaker channel additionally performs: equalizer (not simultaneously with bass/treble), spatial effects, and a subwoofer cross-over filter.

2.5.4. Subwoofer Output

The subwoofer signal is created by combining the left and right channels directly behind the loudness block using the formula $(L+R)/2$. Due to the division by 2, the D/A converter will not be overloaded, even with full scale input signals. The subwoofer signal is filtered by a third-order low-pass with programmable corner frequency followed by a level adjustment. At the loudspeaker channels, a complementary high-pass filter can be switched on. Subwoofer and loudspeaker output use the same volume (Loudspeaker Volume Register).

2.5.5. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms

decay time: 37 ms

2.5.6. Micronas BASS (MB)



The **Micronas BASS** system extends the frequency range of loudspeakers or headphones.

After the adaption of MB to the loudspeakers and the cabinet, further customizing of MB allows individual fine tuning of the sound.

The Micronas BASS is placed in the subwoofer path. For applications without a subwoofer, the enhanced bass signal can be added back onto the Left/Right channels (see Fig. 2–1 on page 10). MB combines two effects: dynamic amplification and adding harmonics.

2.5.6.1. Dynamic Amplification

Low frequency signals can be boosted while the output signal amplitude is measured. If the amplitude comes close to a definable limit, the gain is reduced automatically in dynamic Volume mode. Therefore, the system adapts to the signal amplitude which is really present at the output of the MSP device. Clipping effects are avoided.

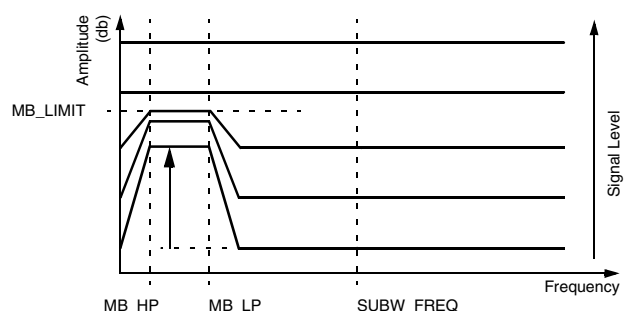


Fig. 2–7: Dynamic amplification

2.5.6.2. Adding Harmonics

Micronas BASS exploits the psychoacoustic phenomenon of the 'missing fundamental'. Adding harmonics of the frequency components below the cutoff frequency gives the impression of actually hearing the low frequency fundamental. In other words: The listener has the impression that a loudspeaker system seems to reproduce frequencies although physically not possible.

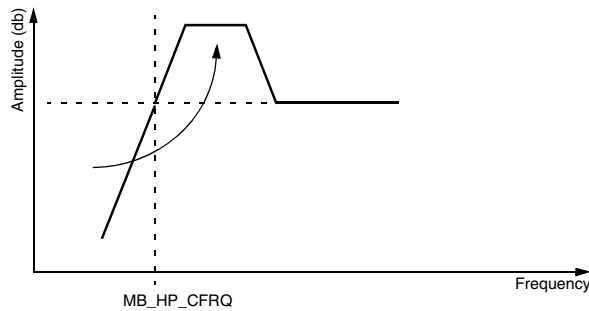


Fig. 2-8: Adding harmonics

2.5.6.3. Micronas BASS Parameters

Several parameters allow tuning the characteristics of Micronas BASS according to the TV loudspeaker, the cabinet, and personal preferences (see Table 3-11 on page 35). For more detailed information on how to set up MB, please refer to the corresponding application note on the Micronas homepage.

2.6. Surround Processing

2.6.1. Output Configuration

Like the MSP 34x1G ICs, the MSP 34x2G can be used for virtual surround sound on the left and right loudspeaker outputs. For multichannel outputs (more than 2 channels), extra output pins have been defined (DACM_C and DACM_S pins). For processing of these output channels, internal resources are shared with the headphone processing. As a result, headphone output is not possible together with multichannel surround processing. When headphone output pins are active, the surround outputs are muted and vice versa. There are two options: the AUX/CS switch and the channel configuration. The output configuration is controlled by means of register 48_{hex} on I²C subaddress 12_{hex}.

2.6.1.1. AUX/CS Switch

This switch defines which output pin pair is driven by the D/A converters that are used for headphone or surround processing. The unselected pins are muted. This makes it convenient to connect the center/surround amplifiers or outputs to the MSP 34x2G without external switches.

Mute the Headphone/Surround channel by setting register 06_{hex} to 0000_{hex} before switching. Allow at least 2 s for settling to avoid audible pops.

2.6.1.2. Channel Configuration

The channel configuration defines whether surround processing is switched on and what resources of the IC are to be used for surround sound processing. There are 3 options:

- **STEREO:**
The IC is in the normal stereo processing mode. No surround processing takes place. In this mode, the IC is compatible to the MSP 34x0G.
- **TWO_CHANNEL:**
Surround sound processing is switched on, but only left and right loudspeaker channels are used for output. This mode is used for virtual surround sound.
- **MULTI_CHANNEL:**
Surround sound processing is switched on, left and right loudspeaker channels together with left and right headphone channels are used for output. The following relationship applies: Center corresponds to the left headphone channel; Surround corresponds to the right headphone channel.

2.6.2. Surround Processing Mode

Surround sound processing is controlled by three functions:

The "Decoder Matrix" defines which method should be used to create a multichannel signal (L, C, R, S) out of a stereo input.

The "Surround Reproduction" determines whether the surround signal "S" is fed to surround speakers. If no surround speaker is actually connected, it defines the method that should be used to create surround effects.

The "Center Mode" determines how the center signal "C" is to be processed. It can be left unmodified, distributed to left and right, discarded or high pass filtered, whereby the low pass signals are distributed to left and right.

The surround processing mode is controlled by means of register 4B_{hex} on I²C subaddress 12_{hex}.

2.6.2.1. Decoder Matrix

The Decoder Matrix allows three settings:

- **ADAPTIVE:**
The adaptive matrix is used for Dolby Surround Pro Logic and Virtual Dolby Surround. Even sound material not encoded in Dolby Surround will produce good surround effects in this mode. The use of the adaptive matrix requires a license from Dolby Laboratories (See License Notice on page 6).
- **PASSIVE:**
A simple fixed matrix is used for other surround modes (Micronas AROUND).
- **EFFECT:**
A fixed matrix that is used for mono sound and special effects. In adaptive or passive mode no surround signal is present in case of mono, moreover in adaptive mode even the left and right output channels carry no signal (or just low frequency signals in case of Center Mode = NORMAL). If surround sound is still required for mono signals, the effect mode can be used. This forces the surround channel to be active. The effect mode can be used together with 3D-PANORAMA. The result will be a pseudo stereo effect or a broadened stereo image respectively.

2.6.2.2. Surround Reproduction

Surround sound can be reproduced with four choices:

- **REAR_SPEAKER:**
If there are any surround speakers connected to the system, this mode should be used. Useful loudspeaker combinations are: (L, C, R, S) or (L, R, S).
- **FRONT_SPEAKER:**
If there is no surround speaker connected, this mode can be used. Surround information is mixed to left and right output but without creating the illusion of a virtual speaker. It is similar to stereo but an additional center speaker can be used. This mode should be used with the adaptive decoder matrix only. Useful loudspeaker combinations are: (L, C, R) (Note: the surround output channel is muted).
- **PANORAMA:**
The surround information is mixed to left and right in order to create the illusion of a virtual surround speaker. Useful loudspeaker combinations are: (L, C, R) or (L, R) (Note: the surround output channel is muted).
- **3D-PANORAMA:**
Like PANORAMA with improved effect. This algorithm has been approved by the Dolby Laboratories for compliance with the "Virtual Dolby Surround" technology. Useful loudspeaker combinations are: (L, C, R) or (L, R) (Note: the surround output channel is muted).

2.6.2.3. Center Modes

Four center modes are supported:

- **NORMAL:**
small center speaker connected, L and R speakers have better bass capability.
- **WIDE:**
L, R, and C speakers all have good bass capability.
- **PHANTOM:**
No center speaker used. Center signal is distributed to L and R (Note: the center output channel C is muted).
- **OFF:**
No center speaker used. Center signal C is discarded (Note: the center output channel C is muted).

2.6.2.4. Useful Combinations of Surround Processing Modes

In principle, "Decoder Matrix", "Surround Reproduction", and "Center Modes" are independent settings (all "Decoder Matrix" settings can be used with all "Surround Reproduction" and "Center Modes") but there are some combinations that do not create "good" sound. Useful combinations are

Surround Reproduction and Center Modes

- **REAR_SPEAKER:**
This mode is used if surround speakers are available. Useful center modes are NORMAL, WIDE, PHANTOM, and OFF.
- **FRONT_SPEAKER:**
This mode can be used if no surround speaker but a center speaker is connected. Useful center modes are NORMAL and WIDE.
- **PANORAMA or 3D-PANORAMA:**
No surround speaker used. Two (L and R) or three (L, R, and C) loudspeakers can be used. Useful center modes are NORMAL, WIDE, PHANTOM, and OFF.

Center Modes and Decoder Matrix

- **PHANTOM:**
Should only be used together with ADAPTIVE Decoder Matrix.
- **NORMAL and WIDE:**
Can be used together with any Surround Decoder Matrix.
- **OFF:**
In special cases, this mode can be used together with the PASSIVE and EFFECT Decoder Matrix (no center speaker connected).

2.6.3. Examples

Table 2–3 shows some examples of how these modes can be used to configure the IC. The list is not intended to be complete, more modes are possible.

Table 2–3: Examples of Surround Configurations

| Configurations | Speaker Configuration ¹⁾ | Output Configuration | | Surround Processing Mode | | |
|---|-------------------------------------|-------------------------------|------------------------------|-------------------------------|-----------------------------|-------------------|
| | | Register (4B _{hex}) | | Register (4B _{hex}) | | |
| | | AUX/CS Switch [15] | Channel Configuration [14:8] | Decoder Matrix [15:8] | Surround Reproduction [7:4] | Center Mode [3:0] |
| Stereo IC is compatible to the MSP34x0G. | | | | | | |
| Stereo | (L,R) | AUX | STEREO | – | – | – |
| Surround Modes as defined by Dolby Laboratories ²⁾ | | | | | | |
| Dolby Pro Logic | (L,C,R,S) | CS | MULTI_CHANNEL | ADAPTIVE | REAR_SPEAKER | NORMAL WIDE |
| | (L,R,S) | CS | MULTI_CHANNEL | ADAPTIVE | REAR_SPEAKER | PHANTOM |
| Dolby 3 Stereo | (L,C,R) | CS | MULTI_CHANNEL | ADAPTIVE | FRONT_SPEAKER | NORMAL WIDE |
| Virtual Dolby Surround | (L,R) | AUX | TWO_CHANNEL | ADAPTIVE | 3D_PANORAMA | PHANTOM |
| Surround Modes that use the Dolby Pro Logic Matrix ²⁾ | | | | | | |
| 3-Channel Virtual Surround | (L,C,R) | CS | MULTI_CHANNEL | ADAPTIVE | 3D_PANORAMA | NORMAL WIDE |
| Passive Matrix Surround Sound | | | | | | |
| Micronas AROUND Multi-channel (4-channel configuration) | (L,C,R,S) | CS | MULTI_CHANNEL | PASSIVE | REAR_SPEAKER | NORMAL WIDE |
| Micronas AROUND Multi-channel (3-channel configuration) | (L,R,S) | CS | MULTI_CHANNEL | PASSIVE | REAR_SPEAKER | OFF |
| Micronas AROUND Virtual (2-channel configuration) | (L,R) | AUX | TWO_CHANNEL | PASSIVE | 3D_PANORAMA | OFF |
| Micronas AROUND Virtual (3-channel configuration) | (L,C,R) | CS | MULTI_CHANNEL | PASSIVE | 3D_PANORAMA | NORMAL WIDE |
| Special Effects Surround Sound | | | | | | |
| Micronas AROUND for mono (4-channel configuration) | (L,C,R,S) | CS | MULTI_CHANNEL | EFFECT | REAR_SPEAKER | NORMAL WIDE |
| Micronas AROUND Virtual for mono (2-channel configuration) | (L,R) | AUX | TWO_CHANNEL | EFFECT | 3D_PANORAMA | OFF |
| Micronas AROUND Virtual for mono (3-channel configuration) | (L,C,R) | CS | MULTI_CHANNEL | EFFECT | 3D_PANORAMA | NORMAL WIDE |
| ¹⁾ Speakers not in use are muted automatically. | | | | | | |
| ²⁾ The implementation in products requires a license from Dolby Laboratories Licensing Corporation (see note on page 6). | | | | | | |

2.6.4. Application Tips for using 3D-PANORAMA

2.6.4.1. Sweet Spot

Good results are only obtained in a rather close area along the middle axis between the two loudspeakers: the sweet spot. Moving away from this position degrades the effect.

2.6.4.2. Clipping

For the test at Dolby Labs, it is very important to have no clipping effects even with worst case signals. That is, 2 V_{rms} input signal must not clip. The SCART input prescale register has to be set to values of max 19_{hex} (25_{dec}). This is sufficient in terms of clipping.

However, it was found, that by reducing the prescale to a value lower than 25_{dec} more convincing effects are generated in case of very high dynamic signals. A value of 18_{dec} is a good compromise between overall volume and additional headroom.

Test signals: sine sweep with 2 V_{RMS}; L only, R only, L&R equal phase, L&R anti phase.

Listening tests: Dolby Trailers (train trailer, city trailer, canyon trailer...)

2.6.4.3. Loudspeaker Requirements

The loudspeakers used and their positioning inside the TV set will greatly influence the performance of the virtualizer. The algorithm works with the direct sound path. Reflected sound waves reduce the effect. So it's most important to have as much direct sound as possible, compared to indirect sound.

To obtain the approval for a TV set, Dolby Laboratories require mounting the loudspeakers at the front of the set. Loudspeakers radiating to the side of the TV set will not produce convincing effects. Good directionality of the loudspeakers towards the listener is optimal.

The virtualizer was specially developed for implementation in TV sets. Even for rather small stereo TV's, sufficient sound effects can be obtained. For small sets, the loudspeaker placement should be to the side of the CRT; for large screen sets (or 16:9 sets), mounting the loudspeakers below the CRT is acceptable (large separation is preferred, low frequency speakers should be outmost to avoid cancellation effects). Using external loudspeakers with a large stereo base will not create optimal effects.

The loudspeakers should be able to reproduce a wide frequency range. The most important frequency range starts from 160 Hz and ranges up to 5 kHz.

Great care has to be taken with systems that use one common subwoofer: A single loudspeaker cannot reproduce virtual sound locations. The crossover frequency must be lower than 120 Hz.

2.6.4.4. Cabinet Requirements

During listening tests at Dolby Laboratories, no resonances in the cabinet should occur.

Good material to check for resonances are the Dolby Trailers or other dynamic sound tracks.

2.6.5. Input and Output Levels in Dolby Surround Pro Logic Mode

The analog inputs are able to accept 2 V_{rms} input level without overloading any stage before the volume control. The nominal input level (input sensitivity) is 350 mV. This gives 15 dB headroom. The scart prescale value should be set to max 0 dB (max 25_{dec}).

I²S-Inputs should have the same headroom (15 dB) when entering the MSP 34x2G. The highest possible input level of 0 dBFS is accepted without internal overflow. The I²S-prescale value should be set to 0 dB (16_{dec}).

With higher prescale values lower input sensitivities can be accommodated. A higher input sensitivity is not possible, because at least 15 dB headroom is required for every input according to the Dolby specifications.

A full-scale left only input (2 V_{rms}) will produce a full-scale left only output (at 0 dB volume). The typical output level is 1.37 V_{rms} for DACM_L. The same holds true for right only signals (1.37 V_{rms} for DACM_R). A full-scale input level on both inputs (Lin=Rin=2 V_{rms}) will give a center only output with maximum level. The typical output level is 1.37 V_{rms} for DACM_C. A full-scale input level on both inputs (but Lin and Rin with inverted phases) will give a surround-only signal with maximum level (1.37 V_{rms} for DACM_S).

For reproducing Dolby Pro Logic according to its specifications, the center and surround outputs must be amplified by 3 dB with respect to the L and R output signals. This can be done in two ways:

1. By implementing 3 dB more amplification for center and surround loudspeaker outputs.
2. By always selecting volume for L and R 3 dB lower than center and surround. Method 1 is preferable, as method 2 lowers the achievable SNR for left and right signals by 3 dB.

2.6.6. Subwoofer in Surround Mode

If the channel configuration is set to STEREO or TWO_CHANNEL, the subwoofer signal is created by combining the left and right channels directly behind the loudness block using the formula $(L+R)/2$.

Note: This is identical to the MSP 34x0G.

If the channel configuration is MULTI_CHANNEL, the subwoofer signal is created by combining the left and right channels of the loudspeaker channel and the center signal (= headphone left) directly behind the loudness block using the formula $(L+R+C)/2$. Due to the fact, that the subwoofer is formed behind all bass/treble/loudness filters, it is strongly recommended to have exactly the same setting for these filters in both, the loudspeaker and center/surround channels when using the subwoofer output. Any mismatch in these settings will result in an unbalanced mix of L, C and R for the subwoofer signal.

2.6.7. Equalizer in Surround Mode

In the MULTI_CHANNEL Surround mode, the equalizer can be used with one common setting for the left, right, and center channels, but the equalizer cannot be used for the surround channel (see Fig. 2–3 on page 11).

2.7. SCART Signal Routing

2.7.1. SCART DSP In and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with four pairs of SCART-inputs and two pairs of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 48).

2.7.2. Stand-by Mode

If the MSP 34x2G is switched off by first pulling STANDBYQ low and then (after $>1\ \mu\text{s}$ delay) switching off DVSUP and AVSUP, but keeping AHVSUP ('Stand-by-mode'), the SCART switches maintain their position and function. This allows the copying from SCART-input to SCART-output in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (see page 48) are reset to the default configuration (see Table 3–5 on page 26). The reset position of the ACB register becomes active after the first I²C transmission into the Baseband Processing part. By trans-

mitting the ACB register first, the reset state can be redefined.

2.8. I²S Bus Interface

The MSP 34x2G has a synchronous master/slave input/output interface running on 32 kHz.

The interface accepts two formats:

1. I²S_WS changes at the word boundary
2. I²S_WS changes one I²S-clock period before the word boundaries.

All I²S options are set by means of the MODUS and the I2S_CONFIG registers.

The I²S bus interface consists of five pins:

- I2S_DA_IN1, I2S_DA_IN2:
I²S serial data input: 16, 18...32 bits per sample
- I2S_DA_OUT:
I²S serial data output: 16, 18...32 bits per sample
- I2S_CL:
I²S serial clock
- I2S_WS:
I²S word strobe signal defines the left and right sample

If the MSP 34x2G serves as the master on the I²S interface, the clock and word strobe lines are driven by the IC. In this mode, only 16 or 32 bits per sample can be selected. In slave mode, these lines are input to the IC and the MSP clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in slave mode.

An I²S timing diagram is shown in Fig. 4–24 on page 81.

2.9. ADR Bus Interface

For the ASTRA Digital Radio System (ADR), the MSP 3402G, MSP 3412G, and MSP 3452G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x2G should be provided on a feature connector:

- AUD_CL_OUT
- I2S_DA_IN1 or I2S_DA_IN2
- I2S_DA_OUT
- I2S_WS
- I2S_CL
- ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.10. Digital Control I/O Pins and Status Change Indication

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I²C-bus by means of the ACB register (see page 48). This enables the controlling of external hardware switches or other devices via I²C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 32). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 34).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary, I²C bus interactions are reduced to a minimum (see STATUS register on page 34 and MODUS register on page 32).

2.11. Clock PLL Oscillator and Crystal Specifications

The MSP 34x2G derives all internal system clocks from the 18.432 MHz oscillator. In NICAM or in I²S-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I²S-Slave mode at the same time.

For proper performance, the on-chip clock oscillator requires a 18.432 MHz crystal. Note that for the phase-locked modes (NICAM, I²S-Slave), crystals with tighter tolerance are required.

3. Control Interface

3.1. Device and Subaddresses

The MSP 34x2G is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the MSP 34x2G device addresses. In order to allow up to three MSP ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the MSP 34x2G responds to different device addresses. A device address pair is defined as a write address and a read address (see Table 3–1).

Writing is done by sending the write device address, followed by the subaddress byte, two address bytes, and two data bytes.

Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Refer to Section 3.1.3. for the I²C bus protocol and to Section 3.4. “Programming Tips” on page 53 for proposals of MSP 34x2G I²C telegrams. See Table 3–2 for a list of available subaddresses.

Besides the possibility of hardware reset, the MSP can also be reset by means of the RESET bit in the CONTROL register by the controller via I²C bus.

Due to the architecture of the MSP 34x2G, the IC cannot react immediately to an I²C request. The typical

response time is about 0.3 ms. If the MSP cannot accept another byte of data (e.g. while servicing an internal interrupt), it holds the clock line I2C_CL low to force the transmitter into a wait state. The I²C Bus Master must read back the clock line to detect when the MSP is ready to receive the next I²C transmission. The positions within a transmission where this may happen are indicated by “Wait” in Section 3.1.3. The maximum wait period of the MSP during normal operation mode is less than 1 ms.

3.1.1. Internal Hardware Error Handling

In case of any hardware problems (e.g. interruption of the power supply of the MSP), the MSP’s wait period is extended to 1.8 ms. After this time period elapses, the MSP releases data and clock lines.

Indicating and solving the error status:

To indicate the error status, the remaining acknowledge bits of the actual I²C-protocol will be left high. Additionally, bit[14] of CONTROL is set to one. The MSP can then be reset via the I²C bus by transmitting the reset condition to CONTROL.

Indication of reset:

Any reset, even caused by an unstable reset line etc., is indicated in bit[15] of CONTROL.

A general timing diagram of the I²C bus is shown in Fig. 4–23 on page 79.

Table 3–1: I²C Bus Device Addresses

| ADR_SEL | Low (connected to DVSS) | | High (connected to DVSUP) | | Left Open | |
|--------------------|----------------------------|-------------------|------------------------------|-------------------|-------------------|-------------------|
| Mode | Write | Read | Write | Read | Write | Read |
| MSP device address | 80 _{hex} | 81 _{hex} | 84 _{hex} | 85 _{hex} | 88 _{hex} | 89 _{hex} |

Table 3–2: I²C Bus Subaddresses

| Name | Binary Value | Hex Value | Mode | Function |
|---------|--------------|-----------|------------|--|
| CONTROL | 0000 0000 | 00 | Read/Write | Write: Software reset of MSP (see Table 3–3) Read: Hardware error status of MSP |
| WR_DEM | 0001 0000 | 10 | Write | write address demodulator |
| RD_DEM | 0001 0001 | 11 | Write | read address demodulator |
| WR_DSP | 0001 0010 | 12 | Write | write address DSP |
| RD_DSP | 0001 0011 | 13 | Write | read address DSP |

3.1.2. Description of CONTROL Register

Table 3–3: CONTROL as a Write Register

| Name | Subaddress | Bit[15] (MSB) | Bits[14:0] |
|---------|------------|-------------------------|------------|
| CONTROL | 00 hex | 1 : RESET 0 : normal | 0 |

Table 3–4: CONTROL as a Read Register (only MSP 34x2G-versions from A2 on)

| Name | Subaddress | Bit[15] (MSB) | Bit[14] | Bits[13:0] |
|---|------------|--|---|-----------------|
| CONTROL | 00 hex | Reset status after last reading of CONTROL: 0 : no reset occurred 1 : reset occurred | Internal hardware status: 0 : no error occurred 1 : internal error occurred | not of interest |
| Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be reset. | | | | |

3.1.3. Protocol Description

Write to DSP or Demodulator

| | | | | | | | | | | | | | | |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|----------------|-----|---------------|-----|---|
| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | data-byte high | ACK | data-byte low | ACK | P |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|----------------|-----|---------------|-----|---|

Read from DSP or Demodulator

| | | | | | | | | | | | | | | | | | | |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|---|---------------------|------|-----|----------------|-----|---------------|-----|---|
| S | write device address | Wait | ACK | sub-addr | ACK | addr-byte high | ACK | addr-byte low | ACK | S | read device address | Wait | ACK | data-byte high | ACK | data-byte low | NAK | P |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|---|---------------------|------|-----|----------------|-----|---------------|-----|---|

Write to Control Registers

| | | | | | | | | | | |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|---|
| S | write device address | Wait | ACK | sub-addr | ACK | data-byte high | ACK | data-byte low | ACK | P |
|---|----------------------|------|-----|----------|-----|----------------|-----|---------------|-----|---|

Read from Control Register

| | | | | | | | | | | | | | | |
|---|----------------------|------|-----|-------|-----|---|---------------------|------|-----|----------------|-----|---------------|-----|---|
| S | write device address | Wait | ACK | 00hex | ACK | S | read device address | Wait | ACK | data-byte high | ACK | data-byte low | NAK | P |
|---|----------------------|------|-----|-------|-----|---|---------------------|------|-----|----------------|-----|---------------|-----|---|

Note: S = I²C-Bus Start Condition from master
P = I²C-Bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= MSP, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate 'End of Read' or from MSP indicating internal error state
Wait = I²C-Clock line is held low, while the MSP is processing the I²C command.
This waiting time is max. 1 ms

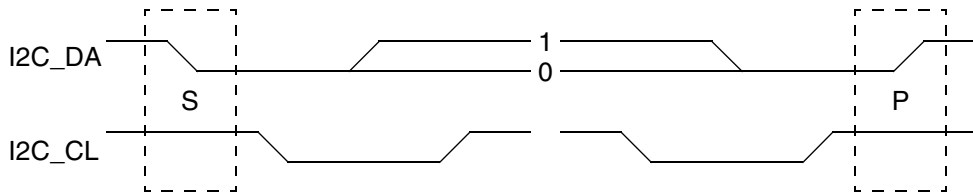


Fig. 3–1: I²C bus protocol (MSB first; data must be stable while clock is high)

3.1.4. Proposals for General MSP 34x2G I²C Telegrams

3.1.4.1. Symbols

| | |
|-----|--|
| daw | write device address (80 _{hex} , 84 _{hex} or 88 _{hex}) |
| dar | read device address (81 _{hex} , 85 _{hex} or 89 _{hex}) |
| < | Start Condition |
| > | Stop Condition |
| aa | Address Byte |
| dd | Data Byte |

3.1.4.2. Write Telegrams

| | |
|----------------------|-----------------------------|
| <daw 00 d0 00> | write to CONTROL register |
| <daw 10 aa aa dd dd> | write data into demodulator |
| <daw 12 aa aa dd dd> | write data into DSP |

3.1.4.3. Read Telegrams

| | |
|---------------------------|------------------------------------|
| <daw 00 <dar dd dd> | read data from CONTROL register |
| <daw 11 aa aa <dar dd dd> | read data from demodulator |
| <daw 13 aa aa <dar dd dd> | read data from DSP |

3.1.4.4. Examples

| | |
|-------------------------|--|
| <80 00 80 00> | RESET MSP statically |
| <80 00 00 00> | Clear RESET |
| <80 10 00 30 00 01> | Automatic Sound Select = ON |
| <80 10 00 20 00 03> | Set demodulator to stand. 03 _{hex} |
| <80 11 02 00 <81 dd dd> | Read STATUS |
| <80 12 00 08 01 20> | Set loudspeaker channel source to Stereo or A/B and Matrix to Stereo (transparent mode) |

More examples of typical application protocols are listed in Section 3.4. “Programming Tips” on page 53.

3.2. Start-Up Sequence: Power-Up and I²C Controlling

After POWER ON or RESET (see Fig. 4–22), the IC is in an inactive state. All registers are in the Reset position (see Table 3–5 and Table 3–6), the analog outputs are muted. The controller has to initialize all registers for which a non-default setting is necessary.

3.3. MSP 34x2G Programming Interface

3.3.1. User Registers Overview

The MSP 34x2G is controlled by means of user registers. The complete list of all user registers is given in Table 3–5 and Table 3–6. The registers are partitioned into the Demodulator section (Subaddress 10_{hex} for writing, 11_{hex} for reading) and the Baseband Processing sections (Subaddress 12_{hex} for writing, 13_{hex} for reading).

Write and read registers are 16-bit wide, whereby the MSB is denoted bit[15]. Transmissions via I²C bus have to take place in 16-bit words (two byte transfers, with the most significant byte transferred first). All write registers, except the demodulator write registers, are readable.

Unused parts of the 16-bit write registers must be zero.
Addresses not given in this table must not be accessed.

For reasons of software compatibility to the MSP 34xxD, a Manual/Compatibility Mode is available. More read and write registers together with a detailed description can be found in the “Appendix B: Manual/Compatibility Mode” on page 95.

Table 3–5: List of MSP 34x2G Write Registers

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|---|---------------|--------|---|-------------------|----------|
| I²C Subaddress = 10_{hex} ; Registers are <i>not</i> readable | | | | | |
| STANDARD SELECT | 00 20 | [15:0] | Initial Programming of complete Demodulator | 00 00 | 30 |
| MODUS | 00 30 | [15:0] | Demodulator, Automatic and I ² S options | 00 00 | 32 |
| I ² S CONFIGURATION | 00 40 | [15:0] | Configuration of I ² S format | 00 00 | 33 |
| I²C Subaddress = 12_{hex} ; Registers are <i>all</i> readable by using I²C Subaddress = 13_{hex} | | | | | |
| Volume loudspeaker channel | 00 00 | [15:8] | [+12 dB ... –114 dB, MUTE] | MUTE | 38 |
| Volume / Mode loudspeaker channel | | [7:0] | 1/8 dB Steps, Reduce Volume / Tone Control / Compromise/ Dynamic | 00 _{hex} | |
| Balance loudspeaker channel [L/R] | 00 01 | [15:8] | [0...100 / 100% and 100 / 0...100%] [–127...0 / 0 dB and 0 / –128...0 dB] | 100%/100% | 39 |
| Balance mode loudspeaker | | [7:0] | [Linear / logarithmic mode] | linear mode | |
| Bass loudspeaker channel | 00 02 | [15:8] | [+20 dB ... –12 dB] | 0 dB | 40 |
| Treble loudspeaker channel | 00 03 | [15:8] | [+15 dB ... –12 dB] | 0 dB | 41 |
| Loudness loudspeaker channel | 00 04 | [15:8] | [0 dB ... +17 dB] | 0 dB | 42 |
| Loudness filter characteristic | | [7:0] | [NORMAL, SUPER_BASS] | NORMAL | |
| Spatial effect strength loudspeaker ch. | 00 05 | [15:8] | [–100%...OFF...+100%] | OFF | 43 |
| Spatial effect mode/customize | | [7:0] | [SBE, SBE+PSE] | SBE+PSE | |
| Volume headphone channel ¹⁾ | 00 06 | [15:8] | [+12 dB ... –114 dB, MUTE] | MUTE | 38 |
| Volume / Mode headphone channel ¹⁾ | | [7:0] | 1/8 dB Steps, Reduce Volume / Tone Control / Compromise/ Dynamic | 00 _{hex} | |
| Volume SCART1 output channel | 00 07 | [15:8] | [+12 dB ... –114 dB, MUTE] | MUTE | 47 |
| Loudspeaker source select | 00 08 | [15:8] | [FM/AM, NICAM, SCART, I ² S1, I ² S2] | FM/AM | 37 |
| Loudspeaker channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| Headphone source select ¹⁾ | 00 09 | [15:8] | [FM/AM, NICAM, SCART, I ² S1, I ² S2] | FM/AM | 37 |
| Headphone channel matrix ¹⁾ | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| SCART1 source select | 00 0a | [15:8] | [FM/AM, NICAM, SCART, I ² S1, I ² S2] | FM/AM | 37 |
| SCART1 channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| I ² S source select | 00 0b | [15:8] | [FM/AM, NICAM, SCART, I ² S1, I ² S2] | FM/AM | 37 |
| I ² S channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| Quasi-peak detector source select | 00 0c | [15:8] | [FM/AM, NICAM, SCART, I ² S1, I ² S2] | FM/AM | 37 |
| Quasi-peak detector matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| Prescale SCART input | 00 0d | [15:8] | [00 _{hex} ... 7F _{hex}] | 00 _{hex} | 36 |
| Prescale FM/AM | 00 0e | [15:8] | [00 _{hex} ... 7F _{hex}] | 00 _{hex} | 35 |
| FM matrix | | [7:0] | [NO_MAT, GSTERERO, KSTEREO] | NO_MAT | 36 |
| Prescale NICAM | 00 10 | [15:8] | [00 _{hex} ... 7F _{hex}] (MSP 3412G, MSP 3452G only) | 00 _{hex} | 36 |
| Prescale I ² S2 | 00 12 | [15:8] | [00 _{hex} ... 7F _{hex}] | 10 _{hex} | 36 |
| ACB : SCART Switches a. D_CTR_I/O | 00 13 | [15:0] | Bits [15..0] | 00 _{hex} | 48 |
| Beeper | 00 14 | [15:0] | [00 _{hex} ... 7F _{hex}]/[00 _{hex} ... 7F _{hex}] | 0/0 | 48 |

Table 3–5: List of MSP 34x2G Write Registers, continued

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|---|---------------|---------|--|-------------------|----------|
| Prescale I ² S1 | 00 16 | [15:8] | [00 _{hex} ... 7F _{hex}] | 10 _{hex} | 36 |
| Tone control mode | 00 20 | [15:8] | [Bass/Treble, Equalizer] | Bass/Treble | 40 |
| Equalizer loudspeaker ch. band 1 | 00 21 | [15:8] | [+12 dB ... –12 dB] | 0 dB | 41 |
| Equalizer loudspeaker ch. band 2 | 00 22 | [15:8] | [+12 dB ... –12 dB] | 0 dB | 41 |
| Equalizer loudspeaker ch. band 3 | 00 23 | [15:8] | [+12 dB ... –12 dB] | 0 dB | 41 |
| Equalizer loudspeaker ch. band 4 | 00 24 | [15:8] | [+12 dB ... –12 dB] | 0 dB | 41 |
| Equalizer loudspeaker ch. band 5 | 00 25 | [15:8] | [+12 dB ... –12 dB] | 0 dB | 41 |
| Acoustical Compensation loudspeaker | 00 26 | [15:0] | C0_Main | 0 | 44 |
| Acoustical Compensation loudspeaker | 00 27 | [15:0] | C1_Main | 0 | 44 |
| Acoustical Compensation loudspeaker | 00 28 | [15:0] | C2_Main | 0 | 44 |
| Automatic Volume Correction | 00 29 | [15:12] | [off, on] | off | 39 |
| | | [11:8] | [decay time] | 00 _{hex} | 39 |
| | | [7:4] | [output level] | –18 dBFS | 39 |
| | | [3:2] | [max attenuation] | 24 dB | 39 |
| | | [1:0] | [max gain] | 6 dB | 39 |
| loudspeaker channel mute and invert | 00 2B | [7:0] | [on, invert, mute] | on | 45 |
| Subwoofer level adjust | 00 2C | [15:8] | [+12 dB ... –30 dB, mute] | 0 dB | 45 |
| Subwoofer corner frequency | 00 2D | [15:8] | [50 Hz ... 400 Hz] | 00 _{hex} | 45 |
| Subwoofer complementary high-pass | | [7:0] | [off, on, Micronas BASS to Main] | off | 45 |
| Balance headphone channel [L/R] ¹⁾ | 00 30 | [15:8] | [0...100 / 100% and 100 / 0...100%] [–127...0 / 0 dB and 0 / –128...0 dB] | 100%/100% | 39 |
| Balance mode headphone ¹⁾ | | [7:0] | [Linear mode / logarithmic mode] | linear mode | |
| Bass headphone channel ¹⁾ | 00 31 | [15:8] | [+20 dB ... –12 dB] | 0 dB | 40 |
| Treble headphone channel ¹⁾ | 00 32 | [15:8] | [+15 dB ... –12 dB] | 0 dB | 41 |
| Loudness headphone channel ¹⁾ | 00 33 | [15:8] | [0 dB ... +17 dB] | 0 dB | 42 |
| Loudness filter characteristic ¹⁾ | | [7:0] | [NORMAL, SUPER_BASS] | NORMAL | |
| Acoustical Compensation center | 00 34 | [15:0] | C0_Center | 0 | 44 |
| Acoustical Compensation center | 00 35 | [15:0] | C1_Center | 0 | 44 |
| Acoustical Compensation center | 00 36 | [15:0] | C2_Center | 0 | 44 |
| Volume SCART2 output channel | 00 40 | [15:8] | [+12 dB ... –114 dB, MUTE] | 00 _{hex} | 47 |
| SCART2 source select | 00 41 | [15:8] | [FM, NICAM, SCART, I ² S1, I ² S2] | FM | 37 |
| SCART2 channel matrix | | [7:0] | [SOUNDA, SOUNDB, STEREO, MONO...] | SOUNDA | 37 |
| AUX/CS switch | 00 48 | [15] | [AUX, CS] | 0 _{hex} | 49 |
| Channel configuration | | [14:8] | [STEREO, TWO_CHANNEL, MULTI_CHANNEL, MULTI_CHANNEL_CENTER] | 00 _{hex} | 49 |
| Tone control mode center channel | | [7:0] | [Bass/Treble, Equalizer] | Bass/Treble | 49 |
| Spatial effect for surround processing | 00 49 | [15:8] | [0% - 100%] | 00 _{hex} | 50 |
| Virtual surround effect strength | 00 4A | [15:8] | [0% - 100%] | 00 _{hex} | 50 |

Table 3–5: List of MSP 34x2G Write Registers, continued

| Write Register | Address (hex) | Bits | Description and Adjustable Range | Reset | See Page |
|--|---------------|--------|---|-------------------|----------|
| Decoder matrix | 00 4B | [15:8] | [ADAPTIVE/PASSIVE/EFFECT] | 00 _{hex} | 51 |
| Surround reproduction | | [7:4] | [REAR_SPEAKER/FRONT_SPEAKER/PANORAMA/3D_PANORAMA] | 0 _{hex} | 51 |
| Center mode | | [3:0] | [PHANTOM/NORMAL/WIDE/OFF] | 0 _{hex} | 51 |
| Surround delay | 00 4C | [15:0] | [5..31ms] | 00 _{hex} | 51 |
| Noise Generator | 00 4D | [15:0] | [NOISEL, NOISEC, NOISER, NOISES] | 00 _{hex} | 51 |
| Micronas BASS Effect Strength | 00 68 | [15:8] | [0 dB ... 127 dB, off] | off | 45 |
| Micronas BASS Amplitude Limit | 00 69 | [15:8] | [0 dB FS... -32 dB FS] | 0 dB FS | 46 |
| Micronas BASS Harmonic Content | 00 6A | [15:8] | [0% ... 100%] | 0% | 46 |
| Micronas BASS Low Pass Corner Frequency | 00 6B | [15:8] | [50 Hz ... 300 Hz] | 0 Hz | 46 |
| Micronas BASS High Pass Corner Frequency | 00 6C | [15:8] | [20 Hz ... 300 Hz] | 0 Hz | 46 |

¹⁾ In Multi Channel Mode, these registers are used for controlling baseband functions of the center and surround channels. Following relationship applies: Center corresponds to the left headphone channel, Surround corresponds to the right headphone channel.

Table 3–6: List of MSP 34x2G Read Registers

| Read Register | Address (hex) | Bits | Description and Adjustable Range | See Page |
|---|---------------|--------|--|----------|
| I²C Subaddress = 11_{hex} ; Registers are <i>not</i> writable | | | | |
| STANDARD RESULT | 00 7E | [15:0] | Result of Automatic Standard Detection | 34 |
| STATUS | 02 00 | [15:0] | Monitoring of internal settings e.g. Stereo, Mono, Mute etc. . | 34 |
| I²C Subaddress = 13_{hex} ; Registers are <i>not</i> writable | | | | |
| Quasi peak readout left | 00 19 | [15:0] | [00 _{hex} ... 7FFF _{hex}] 16 bit two's complement | 52 |
| Quasi peak readout right | 00 1A | [15:0] | [00 _{hex} ... 7FFF _{hex}] 16 bit two's complement | 52 |
| MSP hardware version code | 00 1E | [15:8] | [00 _{hex} ... FF _{hex}] | 52 |
| MSP major revision code | | [7:0] | [00 _{hex} ... FF _{hex}] | 52 |
| MSP product code | 00 1F | [15:8] | [00 _{hex} ... FF _{hex}] | 52 |
| MSP ROM version code | | [7:0] | [00 _{hex} ... FF _{hex}] | 52 |

3.3.2. Description of User Registers

Table 3–7: Standard Codes for STANDARD SELECT register

| MSP Standard Code (Data in hex) | TV Sound Standard | Sound Carrier Frequencies in MHz | MSP 34x2G Version |
|---|--|-------------------------------------|--------------------------|
| Automatic Standard Detection | | | |
| 00 01 | Start Automatic Standard Detection and set to detected standard | | all |
| Standard Selection | | | |
| 00 02 | M-Dual FM-Stereo | 4.5/4.724212 | 3402, -12, -22, -42, -52 |
| 00 03 | B/G -Dual FM-Stereo ¹⁾ | 5.5/5.7421875 | 3402, -12, -52 |
| 00 04 | D/K1-Dual FM-Stereo ²⁾ | 6.5/6.2578125 | |
| 00 05 | D/K2-Dual FM-Stereo ²⁾ | 6.5/6.7421875 | |
| 00 06 | D/K -FM-Mono with HDEV3 ³⁾ , not detectable by Automatic Standard Detection, HDEV3 ³⁾ SAT-Mono (i.e. Eutelsat, see Table 6–18) | 6.5 | |
| 00 07 | D/K3-Dual FM-Stereo | 6.5/5.7421875 | |
| 00 08 | B/G -NICAM-FM ¹⁾ | 5.5/5.85 | 3412, -52 |
| 00 09 | L -NICAM-AM | 6.5/5.85 | |
| 00 0A | I -NICAM-FM | 6.0/6.552 | |
| 00 0B | D/K -NICAM-FM ²⁾ | 6.5/5.85 | |
| 00 0C | D/K -NICAM-FM with HDEV2 ⁴⁾ , not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 0D | D/K -NICAM-FM with HDEV3 ³⁾ , not detectable by Automatic Standard Detection, for China | 6.5/5.85 | |
| 00 20 | BTSC-Stereo | 4.5 | 3422, -42, -52 |
| 00 21 | BTSC-Mono + SAP | | |
| 00 30 | M-EIA-J Japan Stereo | 4.5 | 3422, -42, -52 |
| 00 40 | FM-Stereo Radio with 75 μs Deemphasis | 10.7 | 3422, -42, -52 |
| 00 50 | SAT-Mono (see Table 6–18) | 6.5 | 3402, -12, -52 |
| 00 51 | SAT-Stereo (see Table 6–18) | 7.02/7.20 | |
| 00 60 | SAT ADR (Astra Digital Radio) | 6.12 | |
| <div>¹⁾ In case of Automatic Sound Select, the B/G-codes 3_{hex} and 8_{hex} are equivalent. ²⁾ In case of Automatic Sound Select, the D/K-codes 4_{hex}, 5_{hex}, 7_{hex}, and B_{hex} are equivalent. ³⁾ HDEV3: Max. FM deviation must not exceed 540 kHz ⁴⁾ HDEV2: Max. FM deviation must not exceed 360 kHz</div> | | | |

3.3.2.1. STANDARD SELECT Register

The TV sound standard of the MSP 34x2G demodulator is determined by the STANDARD SELECT register. There are two ways to use the STANDARD SELECT register:

- Setting up the demodulator for a TV sound standard by sending the corresponding standard code with a single I²C-Bus transmission.
- Starting the Automatic Standard Detection for terrestrial TV standards. This is the most comfortable way to set up the demodulator. Within 0.5 s, the detection and set-up of the actual TV sound standard is performed. The detected standard can be read out of the STANDARD RESULT register by the control processor. This feature is recommended for the primary set-up of a TV set. Outputs should be muted during Automatic Standard Detection.

The Standard Codes are listed in Table 3–7.

Selecting a TV sound standard via the STANDARD SELECT register initializes the demodulator. This includes: AGC-settings and carrier mute, tuning frequencies, FIR-filter settings, demodulation mode (FM, AM, NICAM), deemphasis and identification mode.

TV stereo sound standards that are unavailable for a specific MSP version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

For a complete setup of the TV sound processing from analog IF input to the source selection, the transmissions as shown in Section 3.5. are necessary.

For reasons of software compatibility to the MSP 34x0D, a Manual/Compatibility mode is available. A detailed description of this mode can be found on page 95.

3.3.2.2. Refresh of STANDARD SELECT Register

A general refresh of the STANDARD SELECT register is not allowed. However, the following method enables watching the MSP 34x2G “alive” status and detection of accidental resets (only versions A2 and later):

- After Power-on, bit[15] of CONTROL will be set; it must be read once to enable the reset-detection feature.
- Reading of the CONTROL register and checking the reset indicator bit[15].
- If bit[15] is “0”, any refresh of the STANDARD SELECT register **is not allowed**.
- If bit[15] is “1”, indicating a reset, a refresh of the STANDARD SELECT register and all other MSPG registers is required.

3.3.2.3. STANDARD RESULT Register

If Automatic Standard Detection is selected in the STANDARD SELECT register, status and result of the Automatic Standard Detection process can be read out of the STANDARD RESULT register. The possible results are based on the mentioned Standard Code and are listed in Table 3–8.

In cases where no sound standard has been detected (no standard present, too much noise, strong interferers, etc.) the STANDARD RESULT register contains 00 00_{hex}. In that case, the controller has to start further actions (for example, set the standard according to a preference list or by manual input).

As long as the STANDARD RESULT register contains a value greater than 07 FF_{hex}, the Automatic Standard Detection is still active. During this period, the MODUS and STANDARD SELECT register must not be written. The STATUS register will be updated when the Automatic Standard Detection has finished.

If a present sound standard is unavailable for a specific MSP version, it detects and switches to the analog mono sound of this standard.

Example:

The MSP 3442G will detect a B/G-NICAM signal as standard 3 and will switch to the analog FM-Mono sound.

Table 3–8: Results of the Automatic Standard Detection

| Broadcasted Sound Standard | STANDARD RESULT Register Read 007E _{hex} |
|--|--|
| Automatic Standard Detection could not find a sound standard | 0000 _{hex} |
| B/G-FM | 0003 _{hex} |
| B/G-NICAM | 0008 _{hex} |
| I | 000A _{hex} |
| FM-Radio | 0040 _{hex} |
| M-Korea M-Japan M-BTSC | 0002 _{hex} (if MODUS[14,13]=00) |
| | 0020 _{hex} (if MODUS[14,13]=01) |
| | 0030 _{hex} (if MODUS[14,13]=10) |
| L-AM D/K1 D/K2 D/K3 | 0009 _{hex} (if MODUS[12]=0) |
| | 0004 _{hex} (if MODUS[12]=1) |
| L-NICAM D/K-NICAM | 0009 _{hex} (if MODUS[12]=0) |
| | 000B _{hex} (if MODUS[12]=1) |
| Automatic Standard Detection still active | >07FF _{hex} |

3.3.2.4. Write Registers on I²C Subaddress 10_{hex}

Table 3–9: Write Registers on I²C Subaddress 10_{hex}

| Register Address | Function | Name |
|----------------------|---|--------------|
| 00 20 _{hex} | STANDARD SELECTION Register Defines TV Sound or FM-Radio Standard bit[15:0] 00 01 _{hex} start Automatic Standard Detection 00 02 _{hex} Standard Codes (see Table 3–7) ... 00 60 _{hex} | STANDARD_SEL |
| 00 30 _{hex} | MODUS Register Preference in Automatic Standard Detection: bit[15] 0 undefined, must be 0 bit[14:13] detected 4.5 MHz carrier is interpreted as: ¹⁾ 0 standard M (Korea) 1 standard M (BTSC) 2 standard M (Japan) 3 chroma carrier (M/N standards are ignored) bit[12] detected 6.5 MHz carrier is interpreted as: ¹⁾ 0 standard L (SECAM) 1 standard D/K1, D/K2, D/K3, or D/K NICAM General MSP 34x2G Options bit[11:9] 0 undefined, must be 0 bit[8] 0/1 ANA_IN1+/ANA_IN2+; select analog sound IF input pin bit[7] 0/1 active/tristate state of audio clock output pin AUD_CL_OUT bit[6] I ² S word strobe alignment 0 WS changes at data word boundary 1 WS changes one clock cycle in advance bit[5] 0/1 master/slave mode of I ² S interface (must be set to 0 (= Master) in case of NICAM mode) bit[4] 0/1 active/tristate state of I ² S output pins bit[3] state of digital output pins D_CTR_I/O_0 and _1 0 active: D_CTR_I/O_0 and _1 are output pins (can be set by means of the ACB register. see also: MODUS[1]) 1 tristate: D_CTR_I/O_0 and _1 are input pins (level can be read out of STATUS[4,3]) bit[2] 0 undefined, must be 0 bit[1] 0/1 disable/enable STATUS change indication by means of the digital I/O pin D_CTR_I/O_1 Necessary condition: MODUS[3] = 0 (active) bit[0] 0/1 off/on: Automatic Sound Select | MODUS |

¹⁾ Valid at the next start of Automatic Standard Detection.

Table 3–9: Write Registers on I²C Subaddress 10_{hex}, continued

| Register Address | Function | Name |
|----------------------|---|------------|
| 00 40 _{hex} | I2S CONFIGURATION Register bit[15:1] 0 not used, must be set to “0” bit[0] I2S_CL frequency and I ² S data sample length for master mode 0 2 x 16 bit (1.024 MHz) 1 2 x 32 bit (2.048 MHz) | I2S_CONFIG |

3.3.2.5. Read Registers on I²C Subaddress 11_{hex}

Table 3–10: Read Registers on I²C Subaddress 11_{hex}

| Register Address | Function | Name |
|----------------------|---|--------------|
| 00 7E _{hex} | STANDARD RESULT Register Readback of the detected TV Sound or FM-Radio Standard bit[15:0] 00 00 _{hex} Automatic Standard Detection could not find a sound standard 00 02 _{hex} MSP Standard Codes (see Table 3–8) ... 00 40 _{hex} >07 FF _{hex} Automatic Standard Detection still active | STANDARD_RES |
| 02 00 _{hex} | STATUS Register Contains all user relevant internal information about the status of the MSP bit[15:10] undefined bit[8] 0/1 “1” indicates bilingual sound mode or SAP present (internally evaluated from received analog or digital identification signal) bit[7] 0/1 “1” indicates independent mono sound (only for NICAM) bit[6] 0/1 mono/stereo indication (internally evaluated from received analog or digital identification signals) bit[5,9] 00 analog sound standard (FM or AM) active 01 this pattern will not occur 10 digital sound (NICAM) available 11 bad reception condition of digital sound (NICAM) due to: a. high error rate b. unimplemented sound code c. data transmission only bit[4] 0/1 low/high level of digital I/O pin D_CTR_I/O_1 bit[3] 0/1 low/high level of digital I/O pin D_CTR_I/O_0 bit[2] 0 detected secondary carrier (2nd A2 or SAP carrier) 1 no secondary carrier detected bit[1] 0 detected primary carrier (Mono or MPX carrier) 1 no primary carrier detected bit[0] undefined If STATUS change indication is activated by means of MODUS[1]: Each change in the STATUS register sets the digital I/O pin D_CTR_I/O_1 to high level. Reading the STATUS register resets D_CTR_I/O_1. | STATUS |

3.3.2.6. Write Registers on I²C Subaddress 12_{hex}

Table 3–11: Write Registers on I²C Subaddress 12_{hex}

| Register Address | Function | Name |
|----------------------|--|--------|
| PREPROCESSING | | |
| 00 0E _{hex} | <p>FM/AM Prescale</p> <p>bit[15:8] 00_{hex} Defines the input prescale gain for the demodulated FM or AM signal</p> <p> ...</p> <p> 7F_{hex}</p> <p> 00_{hex} off (RESET condition)</p> <p>For all FM modes except satellite FM and AM-mode, the combinations of prescale value and FM deviation listed below lead to internal full scale with 1 kHz test signal and 50 μs emphasis.</p> <p>FM mode</p> <p>bit[15:8] 7F_{hex} 28 kHz FM deviation</p> <p> 48_{hex} 50 kHz FM deviation</p> <p> 30_{hex} 75 kHz FM deviation</p> <p> 24_{hex} 100 kHz FM deviation</p> <p> 18_{hex} 150 kHz FM deviation</p> <p> 13_{hex} 180 kHz FM deviation (limit)</p> <p>FM high deviation mode (HDEV2, MSP Standard Code = C_{hex})</p> <p>bit[15:8] 30_{hex} 150 kHz FM deviation</p> <p> 14_{hex} 360 kHz FM deviation (limit)</p> <p>FM very high deviation mode (HDEV3, MSP Standard Code = 6 and D_{hex})</p> <p>bit[15:8] 20_{hex} 450 kHz FM deviation</p> <p> 1A_{hex} 540 kHz FM deviation (limit)</p> <p>Satellite FM with adaptive deemphasis</p> <p>bit[15:8] 10_{hex} recommendation</p> <p>AM mode (MSP Standard Code = 9)</p> <p>bit[15:8] 7C_{hex} recommendation for SIF input levels from 0.1 V_{pp} to 0.8 V_{pp}</p> <p>(Due to the AGC being switched on, the AM-output level remains stable and independent of the actual SIF-level in the mentioned input range)</p> | PRE_FM |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|--|----------------------|
| (continued) 00 0E _{hex} | FM Matrix Modes Defines the dematrix function for the demodulated FM signal bit[7:0] 00 _{hex} no matrix (used for bilingual and unmatrixed stereo sound) 01 _{hex} German stereo (Standard B/G) 02 _{hex} Korean stereo (also used for BTSC, EIA-J and FM Radio) 03 _{hex} sound A mono (left and right channel contain the mono sound of the FM/AM mono carrier) 04 _{hex} sound B mono In case of Automatic Sound Select = on , the FM Matrix Mode is set automatically. Writing to the FM/AM prescale register (00 0E _{hex} high part) is still allowed. In order not to disturb the automatic process, the low part of any I ² C transmission to this register is ignored. Therefore, any FM-Matrix readback values may differ from data written previously. In case of Automatic Sound Select = off , the FM Matrix Mode must be set as shown in Table 6–17 of Appendix B. To enable a Forced Mono Mode set A2 THRESHOLD as described in Section 6.3.2. on page 99 | FM_MATRIX |
| 00 10 _{hex} | NICAM Prescale Defines the input prescale value for the digital NICAM signal bit[15:8] 00 _{hex} ... 7F _{hex} prescale gain examples: 00 _{hex} off 20 _{hex} 0 dB gain 5A _{hex} 9 dB gain (recommendation) 7F _{hex} +12 dB gain (maximum gain) | PRE_NICAM |
| 00 16 _{hex} 00 12 _{hex} | I2S1 Prescale I2S2 Prescale Defines the input prescale value for digital I ² S input signals bit[15:8] 00 _{hex} ... 7F _{hex} prescale gain examples: 00 _{hex} off 10 _{hex} 0 dB gain (recommendation) 7F _{hex} +18 dB gain (maximum gain) | PRE_I2S1 PRE_I2S2 |
| 00 0D _{hex} | SCART Input Prescale Defines the input prescale value for the analog SCART input signal bit[15:8] 00 _{hex} ... 7F _{hex} prescale gain examples: 00 _{hex} off 19 _{hex} 0 dB gain (2 V _{RMS} input leads to digital full scale) Due to the Dolby requirements, this is the maximum value allowed to prohibit clipping of a 2 V _{RMS} input signal. 7F _{hex} +14 dB gain (400 mV _{RMS} input leads to digital full scale) | PRE_SCART |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|--|---|
| SOURCE SELECT AND OUTPUT CHANNEL MATRIX | | |
| 00 08 _{hex} 00 09 _{hex} 00 0A _{hex} 00 41 _{hex} 00 0B _{hex} 00 0C _{hex} | <p>Source for:</p> <p>Loudspeaker Output</p> <p>Headphone Output</p> <p>SCART1 DA Output</p> <p>SCART2 DA Output</p> <p>I²S Output</p> <p>Quasi-Peak Detector</p> <p>bit[15:8] 00_{hex} “FM/AM”: demodulated FM or AM mono signal</p> <p>01_{hex} “Stereo or A/B”: demodulator Stereo or A/B signal (in manual mode, this source is identical to the NICAM source in the MSP 3410D)</p> <p>03_{hex} “Stereo or A”: demodulator Stereo Sound or Language A (only defined for Automatic Sound Select)</p> <p>04_{hex} “Stereo or B”: demodulator Stereo Sound or Language B (only defined for Automatic Sound Select)</p> <p>02_{hex} SCART input</p> <p>05_{hex} I²S1 input</p> <p>06_{hex} I²S2 input</p> <p>0C_{hex} Main channel: AVC processed signal</p> <p>0D_{hex} Main channel: baseband processed signal with volume</p> <p>0E_{hex} Aux channel: baseband processed signal with volume</p> <p>For demodulator sources, see Table 2–2.</p> | SRC_MAIN SRC_AUX SRC_SCART1 SRC_SCART2 SRC_I2S SRC_QPEAK |
| 00 08 _{hex} 00 09 _{hex} 00 0A _{hex} 00 41 _{hex} 00 0B _{hex} 00 0C _{hex} | <p>Matrix Mode for:</p> <p>Loudspeaker Output</p> <p>Headphone Output</p> <p>SCART1 DA Output</p> <p>SCART2 DA Output</p> <p>I²S Output</p> <p>Quasi-Peak Detector</p> <p>bit[7:0] 00_{hex} Sound A Mono (or Left Mono)</p> <p>10_{hex} Sound B Mono (or Right Mono)</p> <p>20_{hex} Stereo (transparent mode)</p> <p>30_{hex} Mono (sum of left and right inputs divided by 2)</p> <p>special modes are available (see Section 6.5.1. on page 107)</p> <p>In Automatic Sound Select mode, the demodulator source channels are set according to Table 2–2. Therefore, the matrix modes of the corresponding output channels should be set to “Stereo” (transparent).</p> | MAT_MAIN MAT_AUX MAT_SCART1 MAT_SCART2 MAT_I2S MAT_QPEAK |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|---------------------|
| LOUDSPEAKER AND HEADPHONE PROCESSING | | |
| 00 00 _{hex} 00 06 _{hex} | <p>Volume Loudspeaker Volume Headphone</p> <p>bit[15:8] volume table with 1 dB step size</p> <p>7F_{hex} +12 dB (maximum volume)</p> <p>7E_{hex} +11 dB</p> <p>...</p> <p>74_{hex} +1 dB</p> <p>73_{hex} 0 dB</p> <p>72_{hex} –1 dB</p> <p>...</p> <p>02_{hex} –113 dB</p> <p>01_{hex} –114 dB</p> <p>00_{hex} Mute (reset condition)</p> <p>FF_{hex} Fast Mute (needs about 75 ms until the signal is completely ramped down)</p> <p>bit[7:5] higher resolution volume table</p> <p>0 +0 dB</p> <p>1 +0.125 dB increase in addition to the volume table</p> <p>...</p> <p>7 +0.875 dB increase in addition to the volume table</p> <p>bit[4] 0 must be set to 0</p> <p>bit[3:0] clipping mode</p> <p>0 reduce volume</p> <p>1 reduce tone control</p> <p>2 compromise</p> <p>3 dynamic</p> <p>With large scale input signals, positive volume settings may lead to signal clipping.</p> <p>The MSP 34x2G loudspeaker and headphone volume function is divided into a digital and an analog section. With Fast Mute, volume is reduced to mute position by digital volume only. Analog volume is not changed. This reduces any audible DC plops. To turn volume on again, the volume step that has been used before Fast Mute was activated must be transmitted.</p> <p>If the clipping mode is set to “reduce volume”, the following rule is used: To prevent severe clipping effects with bass, treble, or equalizer boosts, the internal volume is automatically limited to a level where, in combination with either bass, treble, or equalizer setting, the amplification does not exceed 12 dB.</p> <p>If the clipping mode is “reduce tone control”, the bass or treble value is reduced if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced, where amplification together with volume exceeds 12 dB.</p> <p>If the clipping mode is “compromise mode”, the bass or treble value and volume are reduced half and half if amplification exceeds 12 dB. If the equalizer is switched on, the gain of those bands is reduced half and half, where amplification together with volume exceeds 12 dB.</p> <p>If the clipping mode is “dynamic”, volume is reduced automatically if the signal amplitudes would exceed –2 dBFS within the IC. For operation of Micronas BASS, dynamic mode must be switched on.</p> | VOL_MAIN VOL_AUX |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|---|
| 00 29 _{hex} | Automatic Volume Correction (AVC) Loudspeaker Channel bit[15:12] 00 _{hex} AVC off (and reset internal variables) 08 _{hex} AVC on bit[11:8] decay time 08 _{hex} 8 s decay time 04 _{hex} 4 s decay time 02 _{hex} 2 s decay time 01 _{hex} 20 ms decay time (should be used for approx. 100 ms after channel change) bit[7:4] output level 0 _{hex} –18 dBFS 1 _{hex} –17 dBFS ... f _{hex} –3 dBFS bit[3:2] maximum attenuation 0 _{hex} 24 dB 1 _{hex} 18 dB 2 _{hex} 12 dB bit[1:0] maximum gain 0 _{hex} 6 dB 1 _{hex} 12 dB 3 _{hex} 0 dB | AVC AVC_DECAY AVC_LEVEL AVC_MIN AVC_MAX |
| 00 01 _{hex} 00 30 _{hex} | Balance Loudspeaker Channel Balance Headphone Channel bit[15:8] Linear Mode 7F _{hex} Left muted, Right 100% 7E _{hex} Left 0.8%, Right 100% ... 01 _{hex} Left 99.2%, Right 100% 00 _{hex} Left 100%, Right 100% FF _{hex} Left 100%, Right 99.2% ... 82 _{hex} Left 100%, Right 0.8% 81 _{hex} Left 100%, Right muted bit[15:8] Logarithmic Mode 7F _{hex} Left –127 dB, Right 0 dB 7E _{hex} Left –126 dB, Right 0 dB ... 01 _{hex} Left –1 dB, Right 0 dB 00 _{hex} Left 0 dB, Right 0 dB FF _{hex} Left 0 dB, Right –1 dB ... 81 _{hex} Left 0 dB, Right –127 dB 80 _{hex} Left 0 dB, Right –128 dB bit[7:0] Balance Mode 00 _{hex} linear 01 _{hex} logarithmic Positive balance settings reduce the left channel without affecting the right channel; negative settings reduce the right channel leaving the left channel unaffected. | BAL_MAIN BAL_AUX |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|-----------------------|
| 00 20 _{hex} | Tone Control Mode Loudspeaker Channel bit[15:8] 00 _{hex} bass and treble is active FF _{hex} equalizer is active Defines whether Bass/Treble or Equalizer is activated for the loudspeaker channel. Bass and Equalizer cannot work simultaneously. If Equalizer is used, Bass, and Treble coefficients must be set to zero and vice versa. | TONE_MODE |
| 00 02 _{hex} 00 31 _{hex} | Bass Loudspeaker Channel Bass Headphone Channel bit[15:8] extended range 7F _{hex} +20 dB 78 _{hex} +18 dB 70 _{hex} +16 dB 68 _{hex} +14 dB normal range 60 _{hex} +12 dB 58 _{hex} +11 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB Higher resolution is possible: an LSB step in the normal range results in a gain step of about 1/8 dB, in the extended range about 1/4 dB. With positive bass settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set bass to a value that, in conjunction with volume, would result in an overall positive gain. | BASS_MAIN BASS_AUX |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|--|---|
| 00 03 _{hex} 00 32 _{hex} | Treble Loudspeaker Channel Treble Headphone Channel bit[15:8] 78 _{hex} +15 dB 70 _{hex} +14 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive treble settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set treble to a value that, in conjunction with volume, would result in an overall positive gain. | TREB_MAIN TREB_AUX |
| 00 21 _{hex} 00 22 _{hex} 00 23 _{hex} 00 24 _{hex} 00 25 _{hex} | Equalizer Loudspeaker Channel Band 1 (below 120 Hz) Equalizer Loudspeaker Channel Band 2 (center: 500 Hz) Equalizer Loudspeaker Channel Band 3 (center: 1.5 kHz) Equalizer Loudspeaker Channel Band 4 (center: 5 kHz) Equalizer Loudspeaker Channel Band 5 (above: 10 kHz) bit[15:8] 60 _{hex} +12 dB 58 _{hex} +11 dB ... 08 _{hex} +1 dB 00 _{hex} 0 dB F8 _{hex} –1 dB ... A8 _{hex} –11 dB A0 _{hex} –12 dB Higher resolution is possible: an LSB step results in a gain step of about 1/8 dB. With positive equalizer settings, internal clipping may occur even with overall volume less than 0 dB. This will lead to a clipped output signal. Therefore, it is not recommended to set equalizer bands to a value that, in conjunction with volume, would result in an overall positive gain. | EQUAL_BAND1 EQUAL_BAND2 EQUAL_BAND3 EQUAL_BAND4 EQUAL_BAND5 |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|--|-----------------------|
| 00 04 _{hex} 00 33 _{hex} | Loudness Loudspeaker Channel Loudness Headphone Channel bit[15:8] Loudness Gain 44 _{hex} +17 dB 40 _{hex} +16 dB ... 04 _{hex} +1 dB 03 _{hex} +0.75 dB 02 _{hex} +0.5 dB 01 _{hex} +0.25 dB 00 _{hex} 0 dB bit[7:0] Loudness Mode 00 _{hex} normal (constant volume at 1 kHz) 04 _{hex} Super Bass (constant volume at 2 kHz) Higher resolution of Loudness Gain is possible: An LSB step results in a gain step of about 1/4 dB. Loudness increases the volume of low- and high-frequency signals, while keeping the amplitude of the 1-kHz reference frequency constant. The intended loudness has to be set according to the actual volume setting. Because loudness introduces gain, it is not recommended to set loudness to a value that, in conjunction with volume, would result in an overall positive gain. The corner frequency for bass amplification can be set to two different values. In Super Bass mode, the corner frequency is shifted up. The point of constant volume is shifted from 1 kHz to 2 kHz. | LOUD_MAIN LOUD_AUX |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|----------------------|---|-----------|
| 00 05 _{hex} | <p>Spatial Effects Loudspeaker Channel</p> <p>bit[15:8] Effect Strength</p> <p>7F_{hex} Enlargement 100%</p> <p>3F_{hex} Enlargement 50%</p> <p>...</p> <p>01_{hex} Enlargement 0.78%</p> <p>00_{hex} Effect off</p> <p>FF_{hex} reduction 0.78%</p> <p>...</p> <p>C0_{hex} reduction 50%</p> <p>80_{hex} reduction 100%</p> <p>bit[7:4] Spatial Effect Mode</p> <p>0_{hex} Stereo Basewidth Enlargement (SBE) and Pseudo Stereo Effect (PSE). (Mode A)</p> <p>2_{hex} Stereo Basewidth Enlargement (SBE) only. (Mode B)</p> <p>bit[3:0] Spatial Effect High-Pass Gain</p> <p>0_{hex} max. high-pass gain</p> <p>2_{hex} 2/3 high-pass gain</p> <p>4_{hex} 1/3 high-pass gain</p> <p>6_{hex} min. high-pass gain</p> <p>8_{hex} automatic</p> <p>Spatial effects should not be used together with 3D-PANORAMA or PANORAMA.</p> <p>There are several spatial effect modes available:</p> <p>In mode A (low byte = 00_{hex}), the spatial effect depends on the source mode. If the incoming signal is mono, Pseudo Stereo Effect is active; for stereo signals, Pseudo Stereo Effect and Stereo Basewidth Enlargement is effective. The strength of the effect is controllable by the upper byte. A negative value reduces the stereo image. A strong spatial effect is recommended for small TV sets where loudspeaker spacing is rather close. For large screen TV sets, a more moderate spatial effect is recommended.</p> <p>In mode B, only Stereo Basewidth Enlargement is effective. For mono input signals, the Pseudo Stereo Effect has to be switched on.</p> <p>It is worth mentioning, that all spatial effects affect amplitude and phase response. With the lower 4 bits, the frequency response can be customized. A value of 0_{hex} yields a flat response for center signals (L = R), but a high-pass function for L or R only signals. A value of 6_{hex} has a flat response for L or R only signals, but a low-pass function for center signals. By using 8_{hex}, the frequency response is automatically adapted to the sound material by choosing an optimal high-pass gain.</p> | SPAT_MAIN |
| 00 2B _{hex} | <p>Mute or Invert Loudspeaker D/A Output</p> <p>bit[15:2] must be zero</p> <p>bit[1:0]</p> <p>0_{hex} no modification</p> <p>1_{hex} invert left channel of D/A output</p> <p>2_{hex} mute D/A output</p> | MUT_INV_M |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|----------------------------|
| 00 26 _{hex} 00 27 _{hex} 00 28 _{hex} | Acoustical Compensation Filter Loudspeaker Channel: C0_Main C1_Main C2_Main | ACF_M0 ACF_M1 ACF_M2 |
| 00 34 _{hex} 00 35 _{hex} 00 36 _{hex} | Acoustical Compensation Filter Headphone Left Channel (Center): C0_Center C1_Center C2_Center | ACF_C0 ACF_C1 ACF_C2 |
| | <p>These cells determine the coefficients of a second order filter for acoustical compensation of loudspeaker responses. The transfer function of this filter is</p> $H(z) = \frac{(1 + a0 + 2 \times a1 \times z^{-1} + a2 \times z^{-2})}{(1 + 2 \times b1 \times z^{-1} + b2 \times z^{-2})}$ <p>The transfer function must not have more than 0 dB gain. Micronas will supply a design tool for these coefficients. This feature is switched off by setting all coefficients to zero (reset state). A mute or fastmute operation should precede any change of these coefficients. The coefficients are two's complement numbers.</p> <p>C0:</p> <p>bit[15:6] 10-bit coefficient a0</p> <p>bit[5:3] 3 LSBs for coefficient b1 (together with 6 bit of c1, this forms a 9-bit coefficient for b1)</p> <p>bit[2:0] 3 LSBs for coefficient b2 (together with 6 bit of c2, this forms a 9-bit coefficient for b2)</p> <p>C1:</p> <p>bit[15:6] 10-bit coefficient a1</p> <p>bit[5:0] 6 MSBs for coefficient b1</p> <p>C2:</p> <p>bit[15:6] 10-bit coefficient a2</p> <p>bit[5:0] 6 MSBs for coefficient b2</p> | |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|---|--|---------------------------------|
| SUBWOOFER OUTPUT CHANNEL | | |
| 00 2C _{hex} | <p>Subwoofer Level Adjustment</p> <p>bit[15:8] 0C_{hex} +12 dB</p> <p> ... </p> <p> 01_{hex} +1 dB</p> <p> 00_{hex} 0 dB (default)</p> <p> FF_{hex} –1 dB</p> <p> ... </p> <p> E3_{hex} –29 dB</p> <p> E2_{hex} –30 dB</p> <p> ... </p> <p> 80_{hex} Mute</p> <p>bit[7:0] 00_{hex} must be zero</p> <p>If Micronas BASS is added onto the main channel, this register should be set to 00_{hex}</p> | SUBW_LEVEL |
| 00 2D _{hex} | <p>Subwoofer Corner Frequency</p> <p>bit[15:8] 5...40_{dec} corner frequency in 10 Hz steps (range: 50...400 Hz)</p> <p>If Micronas BASS is active, SUBW_FREQ must be set to a value higher than the MB Lowpass Frequency (MB_LP). Choosing the corner frequency of the subwoofer closer to MB_LP results in a narrower MB frequency range. Recommended value: 1.5×MB_LP</p> <p>Subwoofer Complementary High-Pass Filter</p> <p>bit[7:0] 0_{hex} loudspeaker channel unfiltered</p> <p> 1_{hex} a complementary high-pass is processed in the loudspeaker output channel</p> <p> 2_{hex} MB added onto main channel</p> | <p>SUBW_FREQ</p> <p>SUBW_HP</p> |
| MICRONAS BASS (MB) CONTROL REGISTERS | | |
| 00 68 _{hex} | <p>Micronas BASS Effect Strength</p> <p>bit[15:8] 00_{hex} Micronas BASS OFF (default)</p> <p> 7F_{hex} maximum Micronas BASS</p> <p>bit[7:0] 00_{hex} must be zero</p> <p>The Micronas BASS effect strength can be adjusted in 1dB steps. A value of 44_{hex} will yield a medium Micronas BASS effect.</p> | MB_STR |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|----------------------|---|--------|
| 00 69 _{hex} | Micronas BASS Amplitude Limit bit[15:8] 00 _{hex} 0 dBFS (default limitation) FF _{hex} –1 dBFS ... E0 _{hex} –32 dBFS bit[7:0] 00 _{hex} must be zero The Micronas BASS Amplitude Limit defines the maximum allowed amplitude at the output of the MB relative to 0 dBFS. If the amplitude exceeds MB_LIM, the gain of the MB is automatically reduced. Note that the Volume Clipping Mode must be set to “dynamic” (see page 38). | MB_LIM |
| 00 6A _{hex} | Micronas BASS Harmonic Content bit[15:8] 00 _{hex} no harmonics are added (default) 3F _{hex} 50% fundamentals + 50% harmonics 7F _{hex} 100% harmonics bit[7:0] 00 _{hex} must be zero Micronas BASS creates harmonics of the frequencies below the MB highpass frequency (MB_HP). The variable MB_HMC describes the ratio of the harmonics towards the original signal. | MB_HMC |
| 00 6B _{hex} | Micronas BASS Low Pass Corner Frequency bit[15:8] 5 _{dec} 50 Hz 6 _{dec} 60 Hz ... 30 _{dec} 300 Hz bit[7:0] 00 _{hex} must be zero The MB lowpass corner frequency (range 50...300 Hz) defines the upper corner frequency of the MB bandpass filter. Recommended values are the same as for the MB highpass corner frequency (MB_HP). | MB_LP |
| 00 6C _{hex} | Micronas BASS High Pass Corner Frequency bit[15:8] 3 _{dec} 30 Hz 4 _{dec} 40 Hz ... 30 _{dec} 300 Hz bit[7:0] 00 _{hex} must be zero The Micronas BASS highpass corner frequency defines the lower corner frequency of the MB bandpass filter. The highpass filter avoids loading the loudspeakers with low frequency components that are below the speakers' cut off frequency. Recommended values for subwoofer systems are around 5 _{dec} (=50 Hz), for regular TV sets around 10 _{dec} (=100 Hz). | MB_HP |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|--------------------------|
| SCART OUTPUT CHANNEL | | |
| 00 07 _{hex} 00 40 _{hex} | Volume SCART1 Output Channel Volume SCART2 Output Channel bit[15:8] volume table with 1 dB step size 7F _{hex} +12 dB (maximum volume) 7E _{hex} +11 dB ... 74 _{hex} +1 dB 73 _{hex} 0 dB 72 _{hex} –1 dB ... 02 _{hex} –113 dB 01 _{hex} –114 dB 00 _{hex} Mute (reset condition) bit[7:5] higher resolution volume table 0 +0 dB 1 +0.125 dB increase in addition to the volume table ... 7 +0.875 dB increase in addition to the volume table bit[4:0] 01 _{hex} this must be 01 _{hex} | VOL_SCART1 VOL_SCART2 |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|--|---|---------|
| SCART SWITCHES AND DIGITAL I/O PINS | | |
| 00 13 _{hex} | <p>ACB Register</p> <p>Defines the level of the digital output pins and the position of the SCART switches</p> <p>bit[15] 0/1 low/high of digital output pin D_CTR_I/O_1 (MODUS[3]=0)</p> <p>bit[14] 0/1 low/high of digital output pin D_CTR_I/O_0 (MODUS[3]=0)</p> <p>bit[13:5] SCART DSP Input Select</p> <p> xxx00xx0 SCART1 to DSP input (RESET position)</p> <p> xxx01xx0 MONO to DSP input (Set Sound A Mono in the channel matrix mode for the corresponding output channels)</p> <p> xxx10xx0 SCART2 to DSP input</p> <p> xxx11xx0 SCART3 to DSP input</p> <p> xxx00xx1 SCART4 to DSP input</p> <p> xxx11xx1 mute DSP input</p> <p>bit[13:5] SCART1 Output Select</p> <p> xx00xxx0x SCART3 input to SCART1 output (RESET position)</p> <p> xx01xxx0x SCART2 input to SCART1 output</p> <p> xx10xxx0x MONO input to SCART1 output</p> <p> xx11xxx0x SCART1 DA to SCART1 output</p> <p> xx00xxx1x SCART2 DA to SCART1 output</p> <p> xx01xxx1x SCART1 input to SCART1 output</p> <p> xx10xxx1x SCART4 input to SCART1 output</p> <p> xx11xxx1x mute SCART1 output</p> <p>bit[13:5] SCART2 Output Select</p> <p> 00xxxx0xx SCART1 DA to SCART2 output (RESET position)</p> <p> 01xxxx0xx SCART1 input to SCART2 output</p> <p> 10xxxx0xx MONO input to SCART2 output</p> <p> 00xxxx1xx SCART2 DA to SCART2 output</p> <p> 01xxxx1xx SCART2 input to SCART2 output</p> <p> 10xxxx1xx SCART3 input to SCART2 output</p> <p> 11xxxx1xx SCART4 input to SCART2 output</p> <p> 11xxxx0xx mute SCART2 output</p> <p>bit[4:0] must be zero</p> <p>The RESET position becomes active at the time of the first write transmission on the control bus to the audio processing part. By writing to the ACB register first, the RESET state can be redefined.</p> | ACB_REG |
| BEEPER | | |
| 00 14 _{hex} | <p>Beeper Volume and Frequency</p> <p>bit[15:8] Beeper Volume</p> <p> 00_{hex} off</p> <p> 7F_{hex} maximum volume</p> <p>bit[7:0] Beeper Frequency</p> <p> 01_{hex} 16 Hz (lowest)</p> <p> 40_{hex} 1 kHz</p> <p> FF_{hex} 4 kHz</p> | BEEPER |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|----------------------------|---|--|
| SURROUND PROCESSING | | |
| 00 48 _{hex} | <p>Output Configuration</p> <p>bit[15] AUX/CS Switch</p> <p> 0 Headphone outputs are active (pin names: DACA_L, DACA_R), CS outputs are muted</p> <p> 1 CS (Center/Surround) outputs are active (pin names: DACM_C, DACM_S), Aux outputs are muted (C corresponds to Aux L, S to Aux R)</p> <p>The AUX/CS switch defines which output pin pair is driven by the D/A converters that are used for headphone or surround processing. The unselected pins are muted. This makes it convenient to connect the center/surround amplifiers or outputs to the MSP 34x2G without external switches. The Headphone/Surround channel should be muted before switching (set register 06_{hex} to: 0000_{hex}). Allow at least 2 s for settling.</p> <p>bit[14:8] Channel Configuration</p> <p> 00_{hex} STEREO: This mode is used in plain stereo mode. Standard processing applies to the loudspeaker and headphone channels. Surround processing is switched off. In this mode, the IC is compatible to the MSP 34x0G (if bit[15] is equal to 0).</p> <p> 01_{hex} TWO_CHANNEL: This mode is used for virtual surround sound. The surround processing block is active and its left and right outputs are distributed to the loudspeaker output channel. The processing on the headphone channel remains standard. In this mode, the IC is comparable to the MSP 34x1G.</p> <p> 02_{hex} MULTI_CHANNEL: This mode is used for surround sound with more than 2 channels. The surround processing block is active and its left and right outputs are distributed to the loudspeaker output channel, its center and surround outputs are distributed to the headphone output channel. No headphone processing is possible. In this mode, it is convenient to select the C/S pins by setting bit[15] to 1.</p> <p> 03_{hex} MULTI_CHANNEL_CENTER: This mode is used for surround sound with more than 2 channels. The surround processing block is active and its left and right outputs are distributed to the loudspeaker output channel, its center and surround outputs are distributed to the headphone output channel. Just after the volume control, the center signal is distributed to the left and right loudspeaker outputs as well as to the center outputs. The left and right signals can be accessed via the feedback path to the source selector. No headphone processing is possible. In this mode, it is convenient to select the C/S pins by setting bit[15] to 1.</p> <p>bit[7:0] Tone control mode center channel</p> <p> 00_{hex} Bass/Treble for center channel (same setting as surround chan.)</p> <p> 01_{hex} The center signal is processed with an equalizer using the same band setting as for the loudspeaker equalizer. The surround channel is processed with bass/treble. This mode is only allowed in channel configurations 2 and 3.</p> | <p>MA_CONF</p> <p>AUX_CS</p> <p>CHAN_CONF</p> <p>C_TONE_MODE</p> |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|----------------------|---|-----------|
| 00 49 _{hex} | Spatial Effects for Surround Processing bit[15:8] Spatial Effect Strength 7F _{hex} Enlargement 100% 3F _{hex} Enlargement 50% ... 01 _{hex} Enlargement 0.78% 00 _{hex} Effect off bit[7:0] 00 _{hex} must be 0 Increases the perceived basewidth of the reproduced left and right front channels. Recommended value: 50% = 3F _{hex} . In contrast to the spatial effect for the loudspeaker channel, the surround spatial effect is optimized for surround sound. Note: If surround sound processing is active, the spatial effect for the loudspeaker channel (Register 05 _{hex}) is switched off. | SUR_SPAT |
| 00 4A _{hex} | Virtual Surround Effect Strength bit[15:8] Virtual Surround Effect Strength 7F _{hex} Effect 100% 54 _{hex} Effect 66% 3F _{hex} Effect 50% ... 01 _{hex} Effect 0.78% 00 _{hex} Effect off bit[7:0] 00 _{hex} must be 0 Strength of the surround effect in PANORAMA or 3D-PANORAMA mode. In other Surround Reproduction Modes, this value must be set to 0. Recommended value: 66% = 54 _{hex} . | SUR_3DEFF |

Table 3–11: Write Registers on I²C Subaddress 12_{hex}, continued

| Register Address | Function | Name |
|----------------------|---|---|
| 00 4B _{hex} | <p>Surround Processing Mode</p> <p>bit[15:8] Decoder Matrix</p> <p>00_{hex} ADAPTIVE (for Dolby Pro Logic and Virtual Dolby Surround)</p> <p>10_{hex} PASSIVE (for Micronas AROUND)</p> <p>20_{hex} EFFECT (used for special effects and monophonic Micronas AROUND)</p> <p>bit[7:4] Surround Reproduction</p> <p>0_{hex} REAR_SPEAKER: The surround signal is reproduced by a rear speaker.</p> <p>3_{hex} FRONT_SPEAKER: The surround signal is redirected to the front channels. There is no physical rear speaker connected.</p> <p>5_{hex} PANORAMA: The surround signal is processed and redirected to the left and right front speakers in order to create the illusion of a virtual rear speaker, although no physical rear speaker is connected.</p> <p>6_{hex} 3D-PANORAMA® (approved by Dolby Laboratories to be compliant with Virtual Dolby Surround technology): The surround signal is processed and redirected to the left and right front speakers in order to create the illusion of a virtual rear speaker, although no physical rear speaker is connected.</p> <p>bit[3:0] Center Mode</p> <p>0_{hex} PHANTOM mode (no Center speaker connected)</p> <p>1_{hex} NORMAL mode (small Center speaker)</p> <p>2_{hex} WIDE mode (large Center speaker)</p> <p>3_{hex} OFF mode (Center output of the Surround Decoder is discarded. Useful only in special effect modes)</p> | <p>SUR_MODE</p> <p>DEC_MAT</p> <p>SUR_REPRO</p> <p>C_MODE</p> |
| 00 4C _{hex} | <p>Surround Delay</p> <p>bit[15:8] 05_{hex} 5 ms delay in surround path (lowest)</p> <p>06_{hex} 6 ms delay in surround path</p> <p>...</p> <p>1F_{hex} 31 ms delay in surround path (highest)</p> <p>bit[7:0] 00_{hex} must be 0</p> <p>For Dolby Surround Pro Logic designs, only 20 ms fixed or 15-30 ms variable delay must be used. This register has no effect in 3D-PANORAMA and PANORAMA mode.</p> | SUR_DELAY |
| 00 4D _{hex} | <p>Noise Generator</p> <p>bit[15:8] 00_{hex} Noise generator off</p> <p>80_{hex} Noise generator on</p> <p>bit[7:0] A0_{hex} Noise on left channel</p> <p>B0_{hex} Noise on center channel</p> <p>C0_{hex} Noise on right channel</p> <p>D0_{hex} Noise on surround channel</p> <p>Determines the active channel for the noise generator.</p> | SUR_NOISE |

3.3.2.7. Read Registers on I²C Subaddress 13_{hex}Table 3–12: Read Registers on I²C Subaddress 13_{hex}

| Register Address | Function | Name |
|--|---|--|
| QUASI-PEAK DETECTOR READOUT | | |
| 00 19 _{hex} 00 1A _{hex} | Quasi-Peak Detector Readout Left Quasi-Peak Detector Readout Right bit[15:0] 0 _{hex} ... 7FFF _{hex} Values are 16 bit two's complement (only positive). A value of 4000 _{hex} corresponds to internal full scale. | QPEAK_L QPEAK_R |
| MSP 34x2G VERSION READOUT Registers | | |
| 00 1E _{hex} | MSP Hardware Version Code bit[15:8] 02 _{hex} MSP 3452G - B3 A change in the hardware version code defines hardware optimizations that may have influence on the chip's behavior. The readout of this register is identical to the hardware version code in the chip's imprint. MSP Major Revision Code bit[7:0] 07 _{hex} MSP 3452G - B3 The major revision code of the MSP 3452G is 7. | MSP_HARD MSP_REVISION |
| 00 1F _{hex} | MSP Product Code bit[15:8] 02 _{hex} MSP 3402G - B3 0C _{hex} MSP 3412G - B3 16 _{hex} MSP 3422G - B3 2A _{hex} MSP 3442G - B3 34 _{hex} MSP 3452G - B3 3E _{hex} MSP 3462G - B3 By means of the MSP-Product Code, the control processor is able to decide which TV sound standards and audio baseband features have to be considered. MSP ROM Version Code bit[7:0] 43 _{hex} MSP 3452G - B3 A change in the ROM version code defines internal software optimizations, that may have influence on the chip's behavior, e.g. new features may have been included. While a software change is intended to create no compatibility problems, customers that want to use the new functions can identify new MSP 34x2G versions according to this number. To avoid compatibility problems with MSP 3410B and MSP 34x0D, an offset of 40 _{hex} is added to the ROM version code of the chip's imprint. | MSP_PRODUCT MSP_ROM |

3.4. Programming Tips

This section describes the preferred method for initializing the MSP 34x2G. The initialization is grouped into four sections:

- SCART Signal Path (analog signal path)
- Demodulator Input
- SCART and I²S Inputs
- Output Channels

See Fig. 2–1 on page 10 for a complete signal flow.

SCART Signal Path

1. Select analog input for the SCART baseband processing (SCART DSP Input Select) by means of the ACB register.
2. Select the source for each analog SCART output (SCART Output Select) by means of the ACB register.

Demodulator Input

For a complete setup of the TV sound processing from analog IF input to the source selection, the following steps must be performed:

1. Set MODUS register to the preferred mode and Sound IF input.
2. Choose preferred prescale (FM and NICAM) values.
3. Write STANDARD SELECT register.
4. If Automatic Sound Select is not active: Choose FM matrix repeatedly according to the sound mode indicated in the STATUS register.

SCART and I²S Inputs

1. Select preferred prescale for SCART.
2. Select preferred prescale for I²S inputs (set to 0 dB after RESET).

Output Channels

1. Select the source channel and matrix for each output channel.
2. Set audio baseband processing.
3. Select volume for each output channel.

3.5. Examples of Minimum Initialization Codes

Initialization of the MSP 34x2G according to these listings reproduces sound of the selected standard on the loudspeaker output. All numbers are hexadecimal. The examples have the following structure:

1. Perform an I²C controlled reset of the IC.
2. Write MODUS register (with Automatic Sound Select).
3. Set Source Selection for loudspeaker channel (with matrix set to STEREO).
4. Set Prescale (FM and/or NICAM and dummy FM matrix).
5. Write STANDARD SELECT register.
6. Set Volume loudspeaker channel to 0 dB.

3.5.1. SCART1 Input to Loudspeaker in Stereo Sound

```
<80 00 80 00>      // reset
<80 00 00 00>
<80 12 00 08 02 20> // source loudspeaker = scart, stereo
<80 12 00 0d 19 00> // prescale scart
<80 12 00 00 73 00> // volume main = 0dB
```

3.5.2. B/G-FM (A2 or NICAM)

```
<80 00 80 00>      // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                    // FM-Matrix = MONO/SOUNDA
<80 12 00 10 5A 00> // NICAM-Prescale = 5Ahex
<80 10 00 20 00 03> // Standard Select: A2 B/G or NICAM B/G
                    or
<80 10 00 20 00 08>
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.3. BTSC-Stereo

```
<80 00 80 00>      // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
                    // FM-Matrix = Sound A Mono
<80 10 00 20 00 20> // Standard Select: BTSC-STEREO
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.4. BTSC-SAP with SAP at Loudspeaker Channel

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 12 00 08 04 20> // Source Sel. = (St or B) & Ch. Matr. = St
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
// FM-Matrix = Sound A Mono
<80 10 00 20 00 21> // Standard Select: BTSC-SAP
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.5. FM-Stereo Radio

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
// FM-Matrix = Sound A Mono
<80 10 00 20 00 40> // Standard Select: FM-STEREO-RADIO
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.6. Automatic Standard Detection

A detailed software flow diagram is shown in Fig. 3–2 on page 55.

```
<80 00 80 00> // Softreset
<80 00 00 00>
<80 10 00 30 20 03> // MODUS-Register: Automatic = on
<80 12 00 08 03 20> // Source Sel. = (St or A) & Ch. Matr. = St
<80 12 00 0E 24 03> // FM/AM-Prescale = 24hex,
// FM-Matrix = Sound A Mono
<80 12 00 10 5A 00> // NICAM-Prescale = 5Ahex
<80 10 00 20 00 01> // Standard Select:
// Automatic Standard Detection

// Wait till STANDARD RESULT contains a value ≤ 07FF
// IF STANDARD RESULT contains 0000
// do some error handling

// ELSE
<80 12 00 00 73 00> // Loudspeaker Volume 0 dB
```

3.5.7. Dolby Surround Pro Logic Example

SCART1 Input to Loudspeaker and Center/Surround Output Pins in Dolby Surround Pro Logic (Normal mode).

```
<80 00 80 00> // reset
<80 00 00 00>
<80 12 00 08 02 20> // source loudspeaker = scart, stereo
<80 12 00 0d 19 00> // prescale scart
<80 12 00 00 70 00> // volume main = –3 dB
<80 12 00 06 73 00> // volume center/surround = 0 dB
<80 12 00 48 82 00> // multi channel mode with C/S outputs
// used
<80 12 00 49 00 00> // Surround spatial effect = 0%
```

```
<80 12 00 4a 00 00> // panorama sound effect = off
<80 12 00 4b 00 01> // Dolby Surround Pro Logic Normal mode
<80 12 00 4c 14 00> // 20 ms Delay
<80 12 00 4d 00 00> // Noise Sequencer = off
```

3.5.8. Virtual Dolby Surround Example

SCART1 Input to Loudspeaker in 3D-PANORAMA Sound

```
<80 00 80 00> // reset
<80 00 00 00>
<80 12 00 08 02 20> // source loudspeaker = scart, stereo
<80 12 00 0d 12 00> // prescale scart with some loss
<80 12 00 00 73 00> // volume main = 0 dB
<80 12 00 48 01 00> // two channel virtual surround mode
<80 12 00 49 3F 00> // Surround spatial effect = 50%
<80 12 00 4a 54 00> // panorama sound effect = 66%
<80 12 00 4b 00 60> // adaptive, 3d_panorama, phantom
<80 12 00 4d 00 00> // Noise Sequencer = off
```

3.5.9. Noise Sequencer for Dolby Pro Logic

// switch into Dolby Pro Logic sound (s.a.). Then:

```
<80 12 00 4d 80 a0> // noise L
[wait for 2 seconds]
<80 12 00 4d 80 b0> // noise C
[wait for 2 seconds]
<80 12 00 4d 80 c0> // noise R
[wait for 2 seconds]
<80 12 00 4d 80 d0> // noise S
[wait for 2 seconds]
// switch back to normal operation
<80 12 00 4d 00 00> // Noise Sequencer = off
```

3.5.10. Software Flow for Interrupt driven STATUS Check

A detailed software flow diagram is shown in Fig. 3–2 on page 55.

If the D_CTR_I/O_1 pin of the MSP 34x2G is connected to an interrupt input pin of the controller, the following interrupt handler can be applied to be automatically called with each status change of the MSP 34x2G. The interrupt handler may adjust the TV display according to the new status information.

Interrupt Handler:

```
<80 11 02 00 <81 dd dd> // Read STATUS
// adjust TV display with given status information
// Return from Interrupt
```

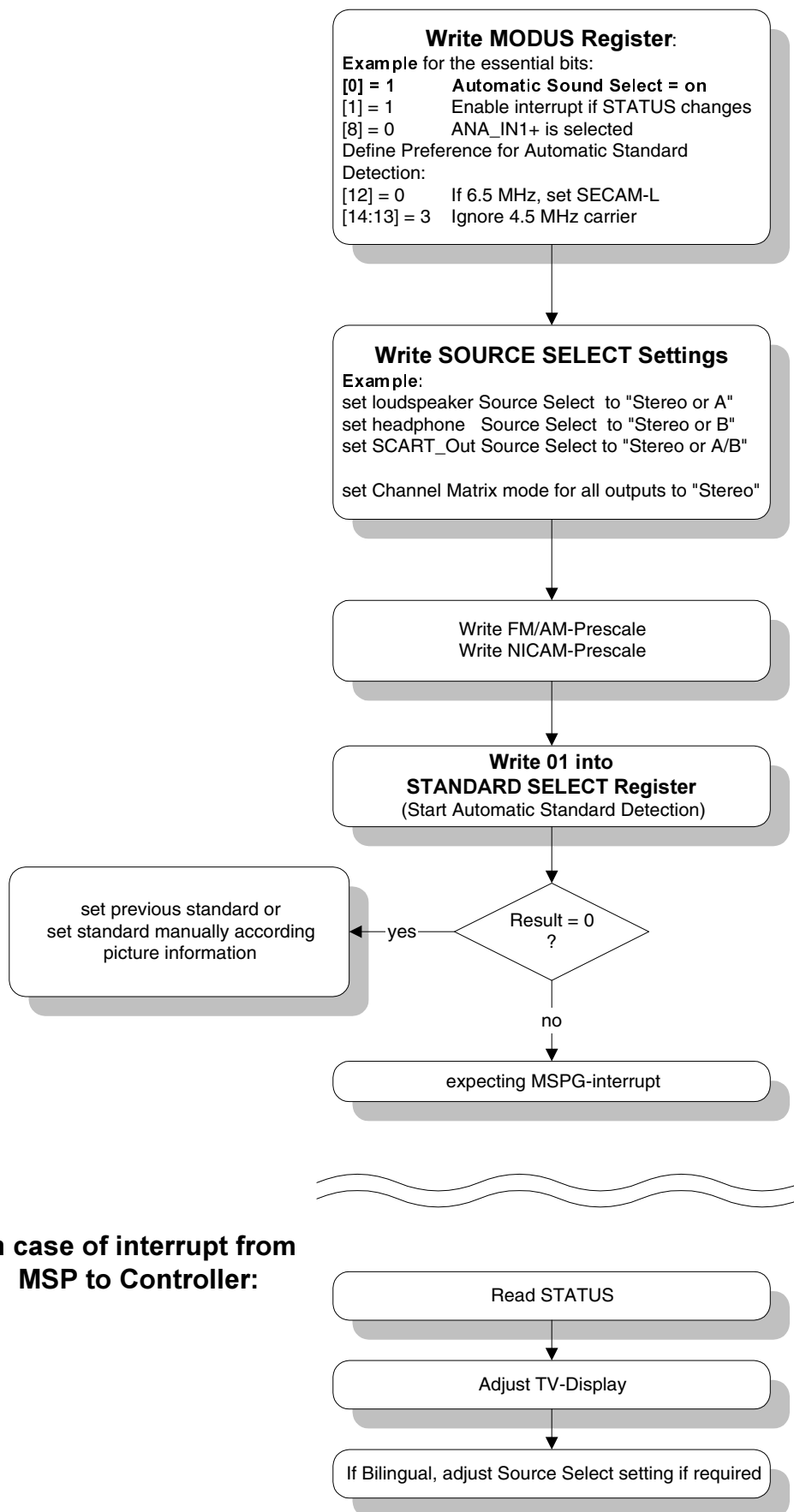


Fig. 3–2: Software flow diagram for a Minimum demodulator setup for a European Multistandard TV set applying the Automatic Sound Select feature

4. Specifications

4.1. Outline Dimensions

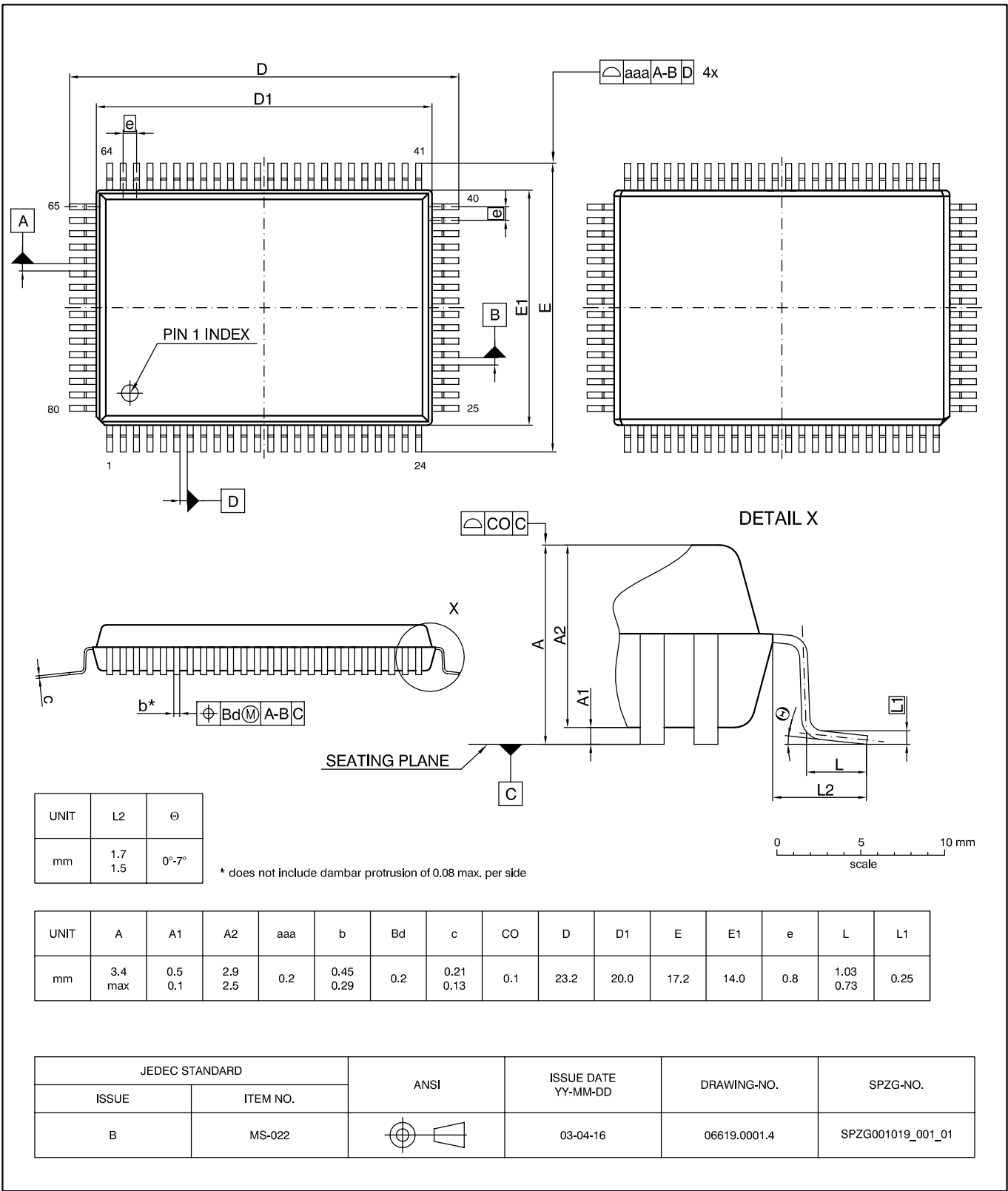


Fig. 4-1:
PMQFP80-11: Plastic Metric Quad Flat Package, 80 leads, 14 × 20 × 2.7 mm³, high standoff
Ordering code: QA
Weight approximately 1.68 g

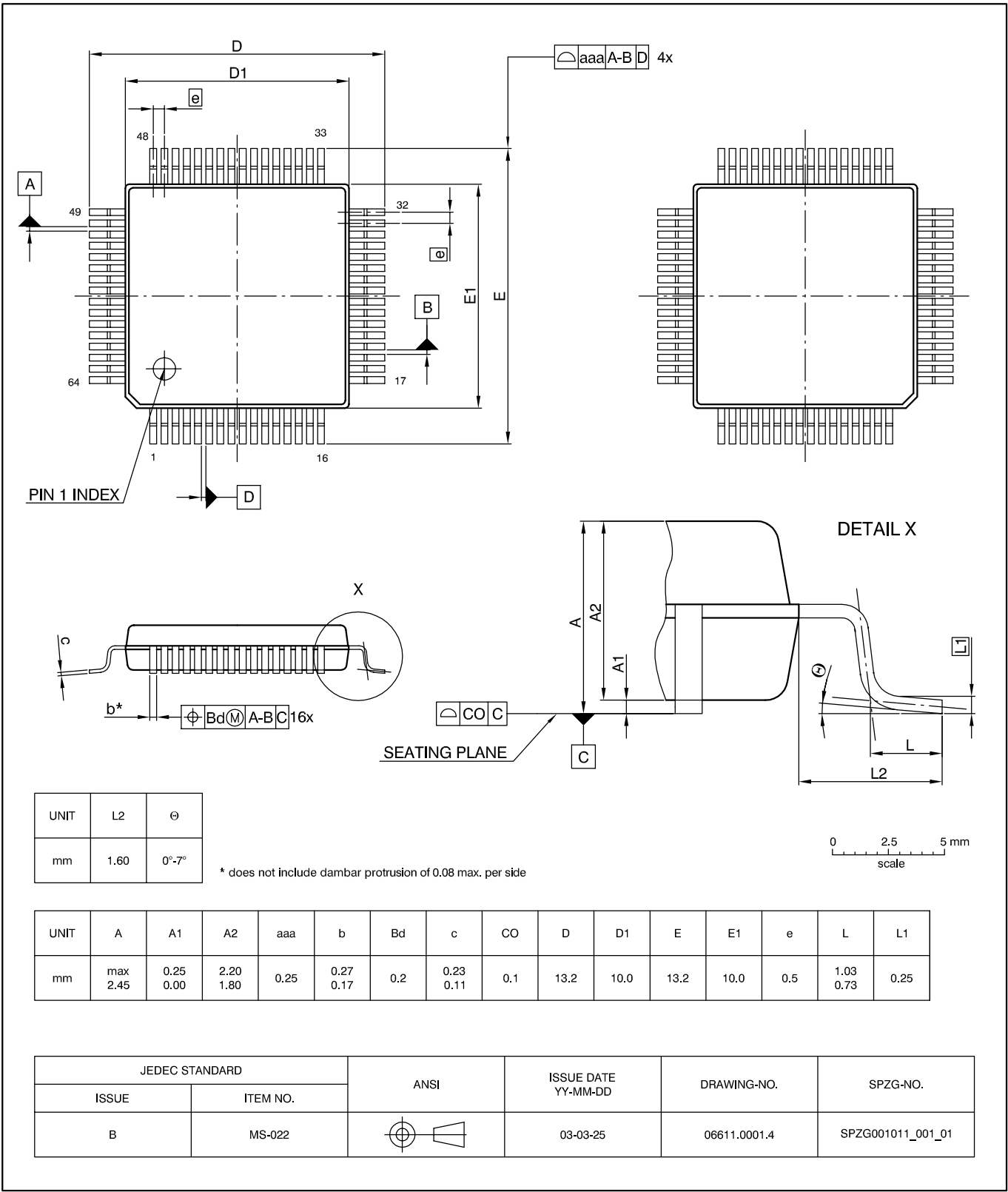


Fig. 4-2:
PMQFP64-2: Plastic Metric Quad Flat Package, 64 leads, 10 × 10 × 2 mm³
Ordering code: QI
Weight approximately 0.5 g

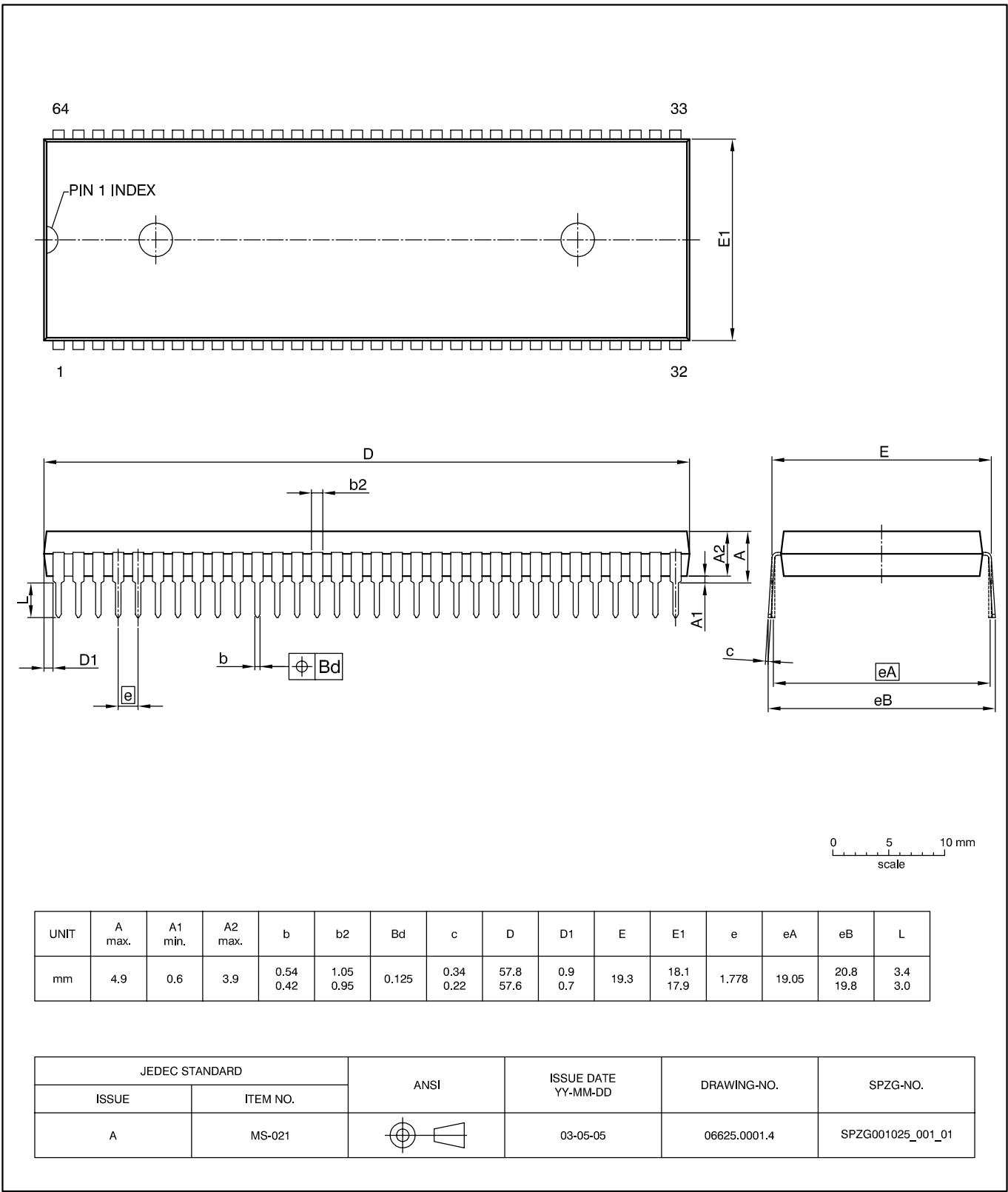


Fig. 4-3:
PSDIP64-1: Plastic Shrink Dual In-line Package, 64 leads, 750 mil
Ordering code: PP
Weight approximately 8.77 g

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant

LV = if not used, leave vacant

OBL = obligatory; connect as described in circuit diagram

DVSS: if not used, connect to DVSS

AHVSS: connect to AHVSS

| Pin No. PMQFP 80-11 | Pin No. PMQFP 64-2 | Pin No. PSDIP 64-1 | Pin Name | Type | Connection (if not used) | Short Description |
|---------------------------|--------------------------|--------------------------|------------|--------|-----------------------------|------------------------------|
| | | | | | | |
| 1 | 64 | 8 | NC | | LV | Not connected |
| 2 | 1 | 9 | I2C_CL | IN/OUT | OBL | I ² C clock |
| 3 | 2 | 10 | I2C_DA | IN/OUT | OBL | I ² C data |
| 4 | 3 | 11 | I2S_CL | IN/OUT | LV | I ² S clock |
| 5 | 4 | 12 | I2S_WS | IN/OUT | LV | I ² S word strobe |
| 6 | 5 | 13 | I2S_DA_OUT | OUT | LV | I ² S data output |
| 7 | 6 | 14 | I2S_DA_IN1 | IN | LV | I ² S1 data input |
| 8 | 7 | 15 | ADR_DA | OUT | LV | ADR data output |
| 9 | 8 | 16 | ADR_WS | OUT | LV | ADR word strobe |
| 10 | 9 | 17 | ADR_CL | OUT | LV | ADR clock |
| 11 | – | – | DVSUP | | OBL | Digital power supply 5 V |
| 12 | – | – | DVSUP | | OBL | Digital power supply 5 V |
| 13 | 10 | 18 | DVSUP | | OBL | Digital power supply 5 V |
| 14 | – | – | DVSS | | OBL | Digital ground |
| 15 | – | – | DVSS | | OBL | Digital ground |
| 16 | 11 | 19 | DVSS | | OBL | Digital ground |
| 17 | 12 | 20 | I2S_DA_IN2 | IN | LV | I ² S2-data input |
| 18 | 13 | 21 | NC | | LV | Not connected |
| 19 | 14 | 22 | NC | | LV | Not connected |
| 20 | 15 | 23 | NC | | LV | Not connected |
| 21 | 16 | 24 | RESETQ | IN | OBL | Power-on-reset |
| 22 | – | – | NC | | LV | Not connected |
| 23 | – | – | NC | | LV | Not connected |
| 24 | 17 | 25 | DACA_R | OUT | LV | Headphone out, right |
| 25 | 18 | 26 | DACA_L | OUT | LV | Headphone out, left |
| 26 | 19 | 27 | VREF2 | | OBL | Reference ground 2 |
| 27 | 20 | 28 | DACM_R | OUT | LV | Loudspeaker out, right |

| PMQFP 80-11 | Pin No. | | Pin Name | Type | Connection (if not used) | Short Description |
|----------------|---------------|---------------|-----------|------|-----------------------------|--------------------------|
| | PMQFP 64-2 | PSDIP 64-1 | | | | |
| 28 | 21 | 29 | DACM_L | OUT | LV | Loudspeaker out, left |
| 29 | 22 | 30 | DACM_C | OUT | LV | Center output |
| 30 | 23 | 31 | DACM_SUB | OUT | LV | Subwoofer output |
| 31 | 24 | 32 | DACM_S | OUT | LV | Surround output |
| 32 | – | – | NC | | LV | Not connected |
| 33 | 25 | 33 | SC2_OUT_R | OUT | LV | SCART output 2, right |
| 34 | 26 | 34 | SC2_OUT_L | OUT | LV | SCART output 2, left |
| 35 | 27 | 35 | VREF1 | | OBL | Reference ground 1 |
| 36 | 28 | 36 | SC1_OUT_R | OUT | LV | SCART output 1, right |
| 37 | 29 | 37 | SC1_OUT_L | OUT | LV | SCART output 1, left |
| 38 | 30 | 38 | CAPL_A | | OBL | Volume capacitor AUX |
| 39 | 31 | 39 | AHVSUP | | OBL | Analog power supply 8 V |
| 40 | 32 | 40 | CAPL_M | | OBL | Volume capacitor MAIN |
| 41 | – | – | NC | | LV | Not connected |
| 42 | – | – | NC | | LV | Not connected |
| 43 | – | – | AHVSS | | OBL | Analog ground |
| 44 | 33 | 41 | AHVSS | | OBL | Analog ground |
| 45 | 34 | 42 | AGNDC | | OBL | Analog reference voltage |
| 46 | – | – | NC | | LV or AHVSS | Not connected |
| 47 | 35 | 43 | SC4_IN_L | IN | LV | SCART 4 input, left |
| 48 | 36 | 44 | SC4_IN_R | IN | LV | SCART 4 input, right |
| 49 | 37 | 45 | ASG | | AHVSS | Analog Shield Ground |
| 50 | 38 | 46 | SC3_IN_L | IN | LV | SCART 3 input, left |
| 51 | 39 | 47 | SC3_IN_R | IN | LV | SCART 3 input, right |
| 52 | 40 | 48 | ASG | | AHVSS | Analog Shield Ground |
| 53 | 41 | 49 | SC2_IN_L | IN | LV | SCART 2 input, left |
| 54 | 42 | 50 | SC2_IN_R | IN | LV | SCART 2 input, right |
| 55 | 43 | 51 | ASG | | AHVSS | Analog Shield Ground |
| 56 | 44 | 52 | SC1_IN_L | IN | LV | SCART 1 input, left |
| 57 | 45 | 53 | SC1_IN_R | IN | LV | SCART 1 input, right |

| PMQFP 80-11 | Pin No. | | Pin Name | Type | Connection (if not used) | Short Description |
|----------------|---------------|---------------|-------------|--------|-----------------------------|--|
| | PMQFP 64-2 | PSDIP 64-1 | | | | |
| 58 | 46 | 54 | VREFTOP | | OBL | Reference voltage IF A/D converter |
| 59 | – | – | NC | | LV | Not connected |
| 60 | 47 | 55 | MONO_IN | IN | LV | Mono input |
| 61 | – | – | AVSS | | OBL | Analog ground |
| 62 | 48 | 56 | AVSS | | OBL | Analog ground |
| 63 | – | – | NC | | LV | Not connected |
| 64 | – | – | NC | | LV | Not connected |
| 65 | – | – | AVSUP | | OBL | Analog power supply 5 V |
| 66 | 49 | 57 | AVSUP | | OBL | Analog power supply 5 V |
| 67 | 50 | 58 | ANA_IN1+ | IN | LV | IF input 1 |
| 68 | 51 | 59 | ANA_IN– | IN | AVSS via 56 pF / LV | IF common (can be left vacant, only if IF input 1 is also not in use) |
| 69 | 52 | 60 | ANA_IN2+ | IN | AVSS via 56 pF / LV | IF input 2 (can be left vacant, only if IF input 1 is also not in use) |
| 70 | 53 | 61 | TESTEN | IN | OBL | Test pin |
| 71 | 54 | 62 | XTAL_IN | IN | OBL | Crystal oscillator |
| 72 | 55 | 63 | XTAL_OUT | OUT | OBL | Crystal oscillator |
| 73 | 56 | 64 | TP | | LV | Test pin |
| 74 | 57 | 1 | AUD_CL_OUT | OUT | LV | Audio clock output (18.432 MHz) |
| 75 | 58 | 2 | NC | | LV | Not connected |
| 76 | 59 | 3 | NC | | LV | Not connected |
| 77 | 60 | 4 | D_CTR_I/O_1 | IN/OUT | LV | D_CTR_I/O_1 |
| 78 | 61 | 5 | D_CTR_I/O_0 | IN/OUT | LV | D_CTR_I/O_0 |
| 79 | 62 | 6 | ADR_SEL | IN | OBL | I ² C Bus address select |
| 80 | 63 | 7 | STANDBYQ | IN | OBL | Stand-by (low-active) |

4.3. Pin Descriptions

Pin numbers refer to the PMQFP80-11 package.

Pin 1, **NC** – Pin not connected.

Pin 2, **I2C_CL** – I²C Clock Input/Output (Fig. 4–14)
Via this pin, the I²C-bus clock signal has to be supplied. The signal can be pulled down by the MSP in case of wait conditions.

Pin 3, **I2C_DA** – I²C Data Input/Output (Fig. 4–14)
Via this pin, the I²C-bus data is written to or read from the MSP.

Pin 4, **I2S_CL** – I²S Clock Input/Output (Fig. 4–15)
Clock line for the I²S bus. In master mode, this line is driven by the MSP; in slave mode, an external I²S clock has to be supplied.

Pin 5, **I2S_WS** – I²S Word Strobe Input/Output (Fig. 4–15)
Word strobe line for the I²S bus. In master mode, this line is driven by the MSP; in slave mode, an external I²S word strobe has to be supplied.

Pin 6, **I2S_DA_OUT** – I²S Data Output (Fig. 4–19)
Output of digital serial sound data of the MSP on the I²S bus.

Pin 7, **I2S_DA_IN1** – I²S Data Input 1 (Fig. 4–11)
First input of digital serial sound data to the MSP via the I²S bus.

Pin 8, **ADR_DA** – ADR Bus Data Output (Fig. 4–19)
Output of digital serial data to the DRP 3510A via the ADR bus.

Pin 9, **ADR_WS** – ADR Bus Word Strobe Output (Fig. 4–19)
Word strobe output for the ADR bus.

Pin 10, **ADR_CL** – ADR Bus Clock Output (Fig. 4–19)
Clock line for the ADR bus.

Pins 11, 12, 13, **DVSUP*** – Digital Supply Voltage
Power supply for the digital circuitry of the MSP. Must be connected to a +5 V power supply.

Pins 14, 15, 16, **DVSS*** – Digital Ground
Ground connection for the digital circuitry of the MSP.

Pin 17, **I2S_DA_IN2** – I²S Data Input 2 (Fig. 4–11)
Second input of digital serial sound data to the MSP via the I²S bus.

Pins 18, 19, 20, **NC** – Pins not connected.

Pin 21, **RESETQ** – Reset Input (Fig. 4–11)
In the steady state, high level is required. A low level resets the MSP 34x2G.

Pins 22, 23, **NC** – Pins not connected.

Pins 24, 25, **DACA_R/L** – Headphone Outputs (Fig. 4–17)
Output of the headphone signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected headphone volume.

Pin 26, **VREF2** – Reference Ground 2
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF2 serves as a clean ground and should be used as the reference for analog connections to the loudspeaker and headphone outputs.

Pins 27, 28, **DACM_R/L** – Loudspeaker Outputs (Fig. 4–17)
Output of the loudspeaker signal. A 1-nF capacitor to AHVSS must be connected to these pins. The DC offset on these pins depends on the selected loudspeaker volume.

Pin 29, **DACM_C** – Center Output (Fig. 4–17)
Output of the center loudspeaker signal. A 1-nF capacitor to AHVSS must be connected to these pins. If active (HP/CS = 1), the DC offset on these pins depends on the selected headphone volume.

Pin 30, **DACM_SUB** – Subwoofer Output (Fig. 4–17)
Output of the subwoofer signal. A 1-nF capacitor to AHVSS must be connected to this pin. Due to the low frequency content of the subwoofer output, the value of the capacitor may be increased for better suppression of high-frequency noise. The DC offset on this pin depends on the selected loudspeaker volume.

Pins 31, **DACM_S** – Surround Output (Fig. 4–17)
Output of the surround loudspeaker signal. A 1-nF capacitor to AHVSS must be connected to these pins. If active (HP/CS = 1), the DC offset on these pins depends on the selected headphone volume.

Pin 32 **NC** – Pin not connected.

Pins 33, 34, **SC2_OUT_R/L** – SCART2 Outputs (Fig. 4–18)
Output of the SCART2 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 35, **VREF1** – Reference Ground 1
Reference analog ground. This pin must be connected separately to the single ground point (AHVSS). VREF1 serves as a clean ground and should be used as the reference for analog connections to the SCART outputs.

Pins 36, 37, **SC1_OUT_R/L** – SCART1 Outputs (Fig. 4–18)

Output of the SCART1 signal. Connections to these pins must use a 100-Ω series resistor and are intended to be AC-coupled.

Pin 38, **CAPL_A** – Volume Capacitor Headphone (Fig. 4–20)

A 10-μF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for headphone volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1-μF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pin 39, **AHVSUP*** – Analog Power Supply High Voltage

Power is supplied via this pin for the analog circuitry of the MSP (except IF input). This pin must be connected to the +8 V supply.

Pin 40, **CAPL_M** – Volume Capacitor Loudspeaker (Fig. 4–20)

A 10-μF capacitor to AHVSUP must be connected to this pin. It serves as a smoothing filter for loudspeaker volume changes in order to suppress audible plops. The value of the capacitor can be lowered to 1 μF if faster response is required. The area encircled by the trace lines should be minimized; keep traces as short as possible. This input is sensitive for magnetic induction.

Pins 41, 42, **NC** – Pins not connected.

Pins 43, 44, **AHVSS*** – Ground for Analog Power Supply High Voltage

Ground connection for the analog circuitry of the MSP (except IF input).

Pin 45, **AGNDC** – Internal Analog Reference Voltage
This pin serves as the internal ground connection for the analog circuitry (except IF input). It must be connected to the VREF pins with a 3.3-μF and a 100-nF capacitor in parallel. This pins shows a DC level of typically 3.73 V.

Pin 46, **NC** – Pin not connected.

Pins 47, 48, **SC4_IN_L/R** – SCART4 Inputs (Fig. 4–10)

The analog input signal for SCART4 is fed to this pin. Analog input connection must be AC-coupled.

Pin 49, **ASG** – Analog Shield Ground

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 50, 51, **SC3_IN_L/R** – SCART3 Inputs (Fig. 4–10)

The analog input signal for SCART3 is fed to this pin. Analog input connection must be AC-coupled.

Pin 52, **ASG** – Analog Shield Ground

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 53, 54 **SC2_IN_L/R** – SCART2 Inputs (Fig. 4–10)

The analog input signal for SCART2 is fed to this pin. Analog input connection must be AC-coupled.

Pin 55, **ASG** – Analog Shield Ground

Analog ground (AHVSS) should be connected to this pin to reduce cross-coupling between SCART inputs.

Pins 56, 57 **SC1_IN_L/R** – SCART1 Inputs (Fig. 4–10)

The analog input signal for SCART1 is fed to this pin. Analog input connection must be AC-coupled.

Pin 58, **VREFTOP** – Reference Voltage IF A/D Converter (Fig. 4–12)

Via this pin, the reference voltage for the IF A/D converter is decoupled. It must be connected to AVSS pins with a 10-μF and a 100-nF capacitor in parallel. Traces must be kept short.

Pin 59, **NC** – Pin not connected.

Pin 60 **MONO_IN** – Mono Input (Fig. 4–9)

The analog mono input signal is fed to this pin. Analog input connection must be AC-coupled.

Pins 61, 62, **AVSS*** – Ground for Analog Power Supply Voltage

Ground connection for the analog IF input circuitry of the MSP.

Pins 63, 64, **NC** – Pins not connected.

Pins 65, 66, **AVSUP*** – Analog Power Supply Voltage
Power is supplied via this pin for the analog IF input circuitry of the MSP. This pin must be connected to the +5 V supply.

Pin 67, **ANA_IN1+** – IF Input 1 (Fig. 4–12)

The analog sound IF signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN1+ is internally connected to one input of a symmetrical op amp, ANA_IN- to the other.

Pin 68, **ANA_IN–** – IF Common (Fig. 4–12)

This pins serves as a common reference for ANA_IN1/2+ inputs.

Pin 69, ANA_IN2+ – IF Input 2 (Fig. 4–12)

The analog sound if signal is supplied to this pin. Inputs must be AC-coupled. This pin is designed as symmetrical input: ANA_IN2+ is internally connected to one input of a symmetrical op amp, ANA_IN– to the other.

Pin 70, TESTEN – Test Enable Pin (Fig. 4–11)

This pin enables factory test modes. For normal operation, it must be connected to ground.

Pins 71, 72 XTAL_IN, XTAL_OUT – Crystal Input and Output Pins (Fig. 4–16)

These pins are connected to an 18.432 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL_IN. The audio clock output signal AUD_CL_OUT is derived from the oscillator. External capacitors at each crystal pin to ground (AVSS) are required. It should be verified by layout, that no supply current for the digital circuitry is flowing through the ground connection point.

Pin 73, **TP** – This pin enables factory test modes. For normal operation, it must be left vacant.

Pin 74, AUD_CL_OUT – Audio Clock Output (Fig. 4–16)

This is the 18.432 MHz main clock output.

Pins 75, 76, **NC** – Pins not connected.

Pins 77, 78, D_CTR_I/O_1/0 – Digital Control Input/Output Pins (Fig. 4–15)

These pins serve as general purpose input/output pins. Pin D_CTR_I/O_1 can be used as an interrupt request pin to the controller.

Pin 79, ADR_SEL – I²C Bus Address Select (Fig. 4–13)

By means of this pin, one of three device addresses for the MSP can be selected. The pin can be connected to ground (I²C device addresses 80/81_{hex}), to +5 V supply (84/85_{hex}), or left open (88/89_{hex}).

Pin 80, STANDBYQ – Stand-by

In normal operation, this pin must be High. If the MSP 34x2G is switched off by first pulling STANDBYQ low and then (after >1 μs delay) switching off the 5 V, but keeping the 8-V power supply ('Stand-by'-mode), the SCART switches maintain their position and function.

*** Application Note:**

All ground pins should be connected to one low-resistive ground plane. All supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from DVSUP to DVSS, AVSUP to AVSS, and AHVSUP to AHVSS are recommended as closely as possible to these pins. Decoupling of DVSUP and DVSS is most important. We recommend using more than one capacitor. By choosing different values, the frequency range of active decoupling can be extended. In our application boards we use: 220 pF, 470 pF, 1.5 nF, and 10 μF. The capacitor with the lowest value should be placed nearest to the DVSUP and DVSS pins.

The ASG pins should be connected as closely as possible to the MSP ground. If they are lead with the SCART-inputs as shielding lines, they should not be connected to ground at the SCART connector.

4.4. Pin Configurations

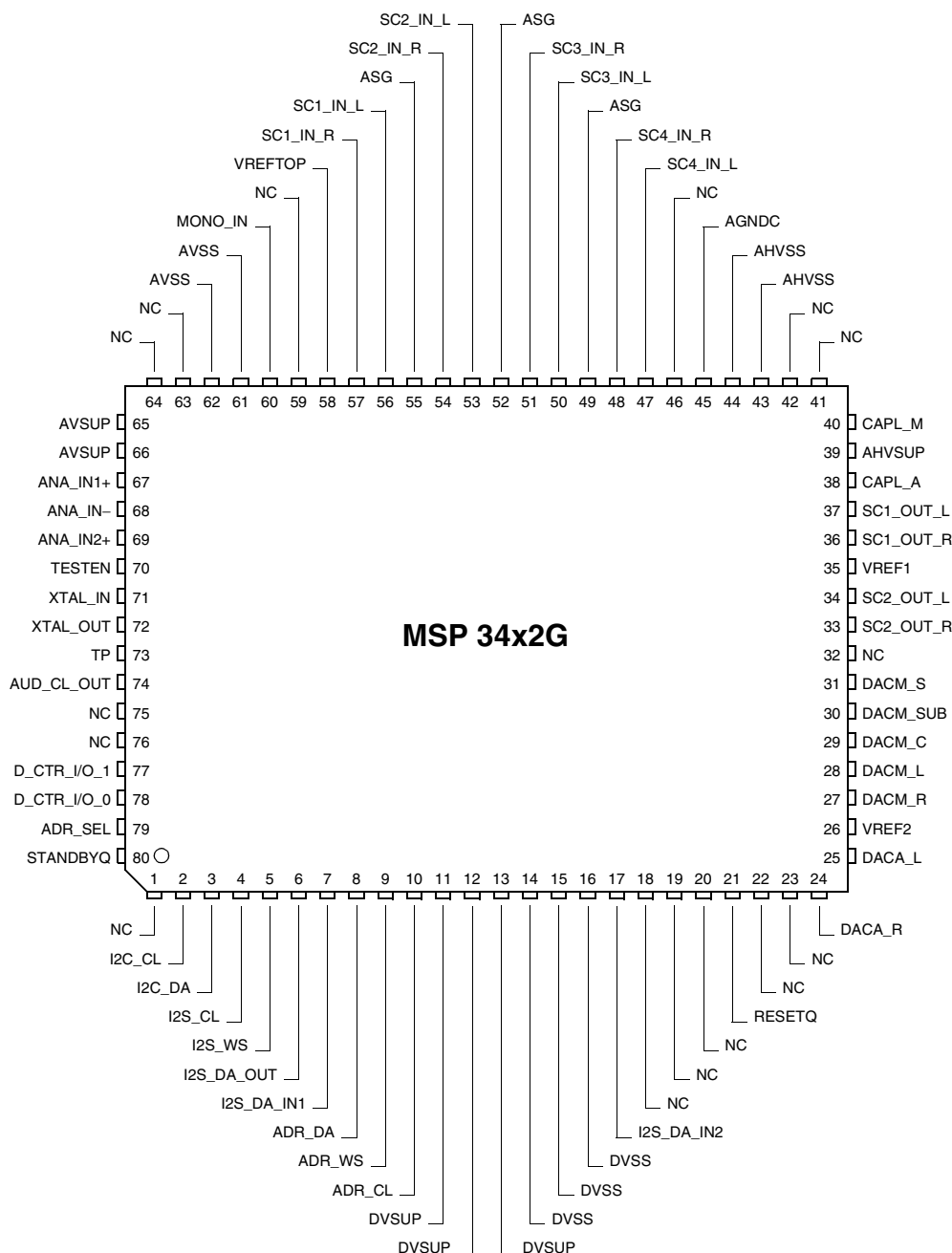


Fig. 4-4: PMQFP80-11 package

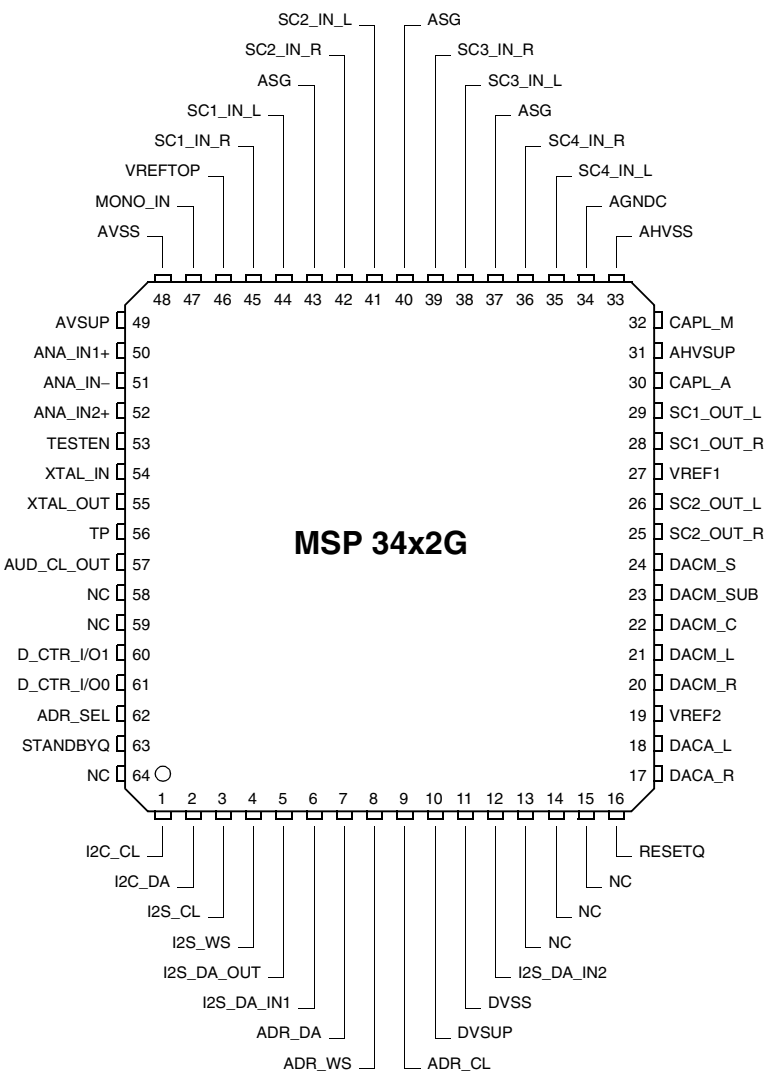


Fig. 4-5: PMQFP64-2 package

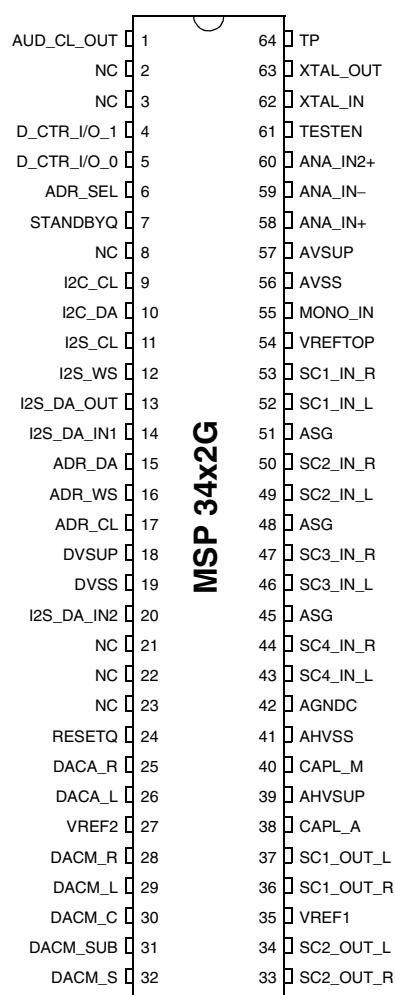
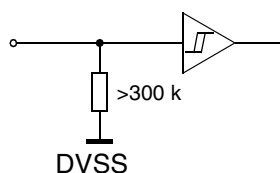
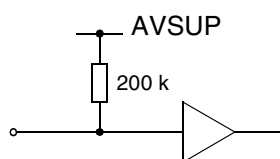
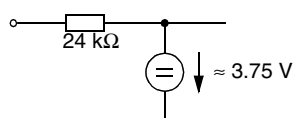
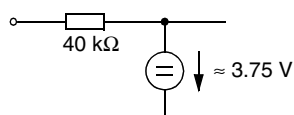
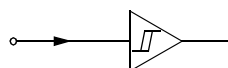
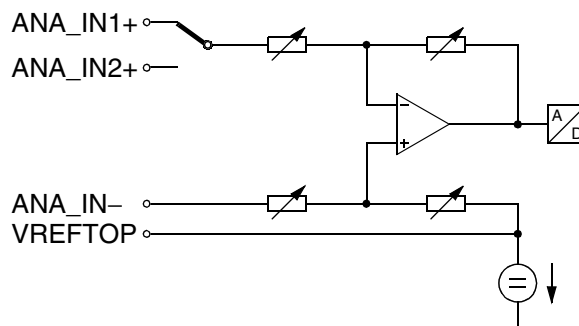
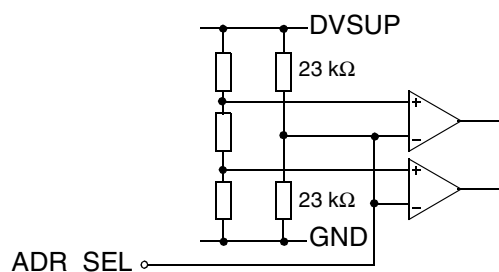
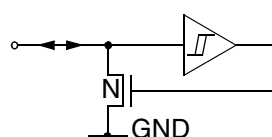
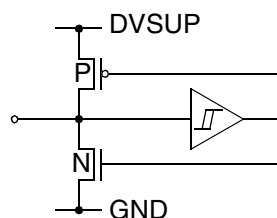


Fig. 4-6: PSDIP64-1 package

4.5. Pin Circuits

Fig. 4-7: Input Pin: **RESETQ**Fig. 4-8: Input Pin: **TESTEN**Fig. 4-9: Input Pin: **MONO_IN**Fig. 4-10: Input Pins: **SC4-1_IN_L/R**Fig. 4-11: Input Pins:
I2S_DA_IN1, I2S_DA_IN2, STANDBYQFig. 4-12: Input Pins 58, 67, 68, and 69:
VREFTOP, ANA_IN1+, ANA_IN-, ANA_IN2+Fig. 4-13: Input Pin: **ADR_SEL**Fig. 4-14: Input/Output Pins: **I2C_CL, I2C_DA**Fig. 4-15: Input/Output Pins:
I2S_CL, I2S_WS, D_CTR_I/O_1, D_CTR_I/O_0

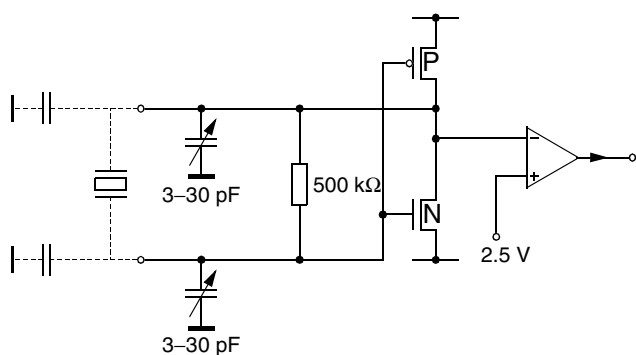


Fig. 4-16: Input/Output Pins:
XTAL_IN, XTAL_OUT, AUD_CL_OUT

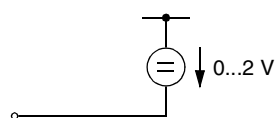


Fig. 4-20: Capacitor Pins: CAPL_A, CAPL_M

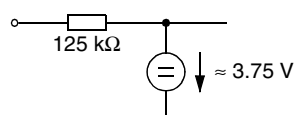


Fig. 4-21: Pin: AGNDC

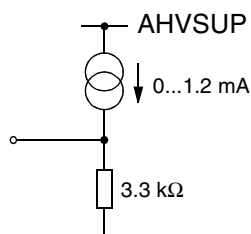


Fig. 4-17: Output Pins:
DACA_R/L, DACM_R/L, DACM_SUB, DACM_C/S

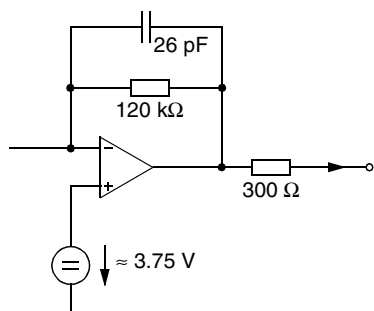


Fig. 4-18: Output Pins:
SC_2_OUT_R/L, SC_1_OUT_R/L

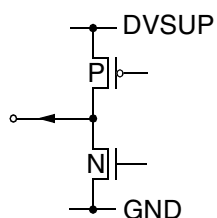


Fig. 4-19: Output Pins:
I2S_DA_OUT, ADR_DA, ADR_WS, ADR_CL

4.6. Electrical Characteristics

Abbreviations:

tbd = to be defined

vacant = not applicable

positive current values mean current flowing into the chip

4.6.1. Absolute Maximum Ratings

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods will affect device reliability.

All voltages listed are referenced to ground (0 V, V_{SS}), except where noted.

All grounds must be externally connected low ohmic.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

Table 4–1: Absolute Maximum Ratings

| Symbol | Parameter | Pin Name | Limit Values | | Unit |
|---|---|----------|--------------|---------------------|----------------|
| | | | Min. | Max. | |
| $T_A^{1)}$ | Ambient Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2 | – | 0 | 70 70 65 | °C |
| T_C | Case Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2 | – | 0 | 85 95 100 | °C |
| T_S | Storage Temperature | – | –40 | 125 | °C |
| P_{MAX} | Maximum Power Dissipation PSDIP64-1 PMQFP80-11 PMQFP64-2 | | | 1300 1000 930 | mW mW mW |
| V_{SUP1} | Supply Voltage 1 | AHVSUP | –0.3 | 9.0 | V |
| V_{SUP2} | Supply Voltage 2 | DVSUP | –0.3 | 6.0 | V |
| V_{SUP3} | Supply Voltage 3 | AVSUP | –0.3 | 6.0 | V |
| V_{Idig} | Input Voltage, all Digital Inputs | | –0.3 | $V_{SUP2}+0.3$ | V |
| I_{Idig} | Input Current, all Digital Pins | – | –20 | +20 | mA |
| ¹⁾ Measured on standard board according to JESD 51 Standard with maximum power consumption allowed for this package. | | | | | |

Table 4–1: Absolute Maximum Ratings, continued

| Symbol | Parameter | Pin Name | Limit Values | | Unit |
|------------|---|------------------------------------|--------------|----------------|------|
| | | | Min. | Max. | |
| V_{Iana} | Input Voltage, all Analog Inputs | SCn_IN_s, ¹⁾ MONO_IN | –0.3 | $V_{SUP1}+0.3$ | V |
| I_{Iana} | Input Current, all Analog Inputs | SCn_IN_s, ¹⁾ MONO_IN | –5 | +5 | mA |
| I_{Oana} | Output Current, all SCART Outputs | SCn_OUT_s ¹⁾ | 2) | 2) | |
| I_{Oana} | Output Current, all Analog Outputs except SCART Outputs | DACM_r, ¹⁾ DACA_s | 2) | 2) | |
| I_{Cana} | Output Current, other pins connected to capacitors | CAPL_A, CAPL_M, AGNDC | 2) | 2) | |

¹⁾ “n” means “1”, “2”, “3”, or “4”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R”

²⁾ The analog outputs are short-circuit proof with respect to Supply Voltage 1 and ground.

4.6.2. Recommended Operating Conditions

Functional operation of the device beyond those indicated in the "Recommended Operating Conditions/Characteristics" is not implied and will result in unpredictable behavior of the device and may result in device destruction.

All voltages listed are referenced to ground ($V_{SS} = 0$ V) except where noted.

All grounds must be externally connected low ohmic.

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply. For power-up/-down sequences, see the instructions in Section 4.6.3.3. of this document.

4.6.2.1. General Recommended Operating Conditions

| Symbol | Parameter | Pin Name | Limit Values | | | Unit |
|--|---|--------------------|--------------|------|----------------------|------|
| | | | Min. | Typ. | Max. | |
| T_A | Ambient Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2 | – | | | 1) 70 70 65 | °C |
| T_C | Case Operating Temperature PSDIP64-1 PMQFP80-11 PMQFP64-2 | – | | | 85 95 100 | °C |
| V_{SUP1} | Supply Voltage 1 (AHVSUP = 8 V) | AHVSUP | 7.6 | 8.0 | 8.7 | V |
| | Supply Voltage 1 (AHVSUP = 5 V) | | 4.75 | 5.0 | 5.25 | V |
| V_{SUP2} | Supply Voltage 2 | DVSUP | 4.75 | 5.0 | 5.25 | V |
| V_{SUP3} | Supply Voltage 3 | AVSUP | 4.75 | 5.0 | 5.25 | V |
| t_{STBYQ1} | STANDBYQ Setup Time before Turn-off of Second Supply Voltage | STANDBYQ, DVSUP | 1 | | | μs |
| 1) A power-optimized board layout is recommended. The Case Operating Temperature mentioned in the Recommended Operating Conditions must not be exceeded at worst case conditions of the application. | | | | | | |

4.6.2.2. Analog Input and Output Recommendations

| Symbol | Parameter | Pin Name | Limit Values | | | Unit |
|---------------------|--|---------------------------------|--------------|------|------|------------------|
| | | | Min. | Typ. | Max. | |
| C _{AGNDC} | AGNDC-Filter-Capacitor | AGNDC | −20% | 3.3 | | μF |
| | Ceramic Capacitor in Parallel | | −20% | 100 | | nF |
| C _{inSC} | DC-Decoupling Capacitor in front of SCART Inputs | SCn_IN_s ¹⁾ | −20% | 330 | | nF |
| V _{inSC} | SCART Input Level | | | | 2.0 | V _{RMS} |
| V _{inMONO} | Input Level, Mono Input | MONO_IN | | | 2.0 | V _{RMS} |
| R _{LSC} | SCART Load Resistance | SCn_OUT_s ¹⁾ | 10 | | | kΩ |
| C _{LSC} | SCART Load Capacitance | | | | 6.0 | nF |
| C _{VMA} | Main/AUX Volume Capacitor | CAPL_M, CAPL_A | | 10 | | μF |
| C _{FMA} | Main/AUX Filter Capacitor | DACM_r, ¹⁾ DACA_s | −10% | 1 | +10% | nF |

¹⁾ “n” means “1”, “2”, “3”, or “4”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R”

4.6.2.3. Recommendations for Analog Sound IF Input Signal

| Symbol | Parameter | Pin Name | Limit Values | | | Unit |
|-------------------------|--|-----------------------------------|--------------|-----------|--------|---|
| | | | Min. | Typ. | Max. | |
| C _{VREFTOP} | VREFTOP-Filter-Capacitor | VREFTOP | −20% | 10 | | μF |
| | Ceramic Capacitor in Parallel | | −20% | 100 | | nF |
| F _{IF_FMTV} | Analog Input Frequency Range for TV Applications | ANA_IN1+, ANA_IN2+, ANA_IN− | 0 | | 9 | MHz |
| F _{IF_FMRADIO} | Analog Input Frequency for FM-Radio Applications | | | 10.7 | | MHz |
| V _{IF_FM} | Analog Input Range FM/NICAM | | 0.1 | 0.8 | 3 | V _{pp} |
| V _{IF_AM} | Analog Input Range AM/NICAM | | 0.1 | 0.45 | 0.8 | V _{pp} |
| R _{FMNI} | Ratio: NICAM Carrier/FM Carrier (unmodulated carriers) BG: I: | | −20 −23 | −7 −10 | 0 0 | dB dB |
| R _{AMNI} | Ratio: NICAM Carrier/AM Carrier (unmodulated carriers) | | −25 | −11 | 0 | dB |
| R _{FM} | Ratio: FM-Main/FM-Sub Satellite | | | 7 | | dB |
| R _{FM1/FM2} | Ratio: FM1/FM2 German FM-System | | | 7 | | dB |
| R _{FC} | Ratio: Main FM Carrier/ Color Carrier | | 15 | − | − | dB |
| R _{FV} | Ratio: Main FM Carrier/ Luma Components | | 15 | − | − | dB |
| PR _{IF} | Passband Ripple | | − | − | ±2 | dB |
| SUP _{HF} | Suppression of Spectrum above 9.0 MHz (not for FM Radio) | | 15 | | − | dB |
| FM _{MAX} | Maximum FM-Deviation (approx.) normal mode HDEV2: high deviation mode HDEV3: very high deviation mode | | | | | ±180 ±360 ±540 kHz kHz kHz |

4.6.2.4. Crystal Recommendations

| Symbol | Parameter | Pin Name | Min. | Typ. | Max. | Unit |
|--|---|----------------------|----------------|----------------------------|---------|----------|
| General Crystal Recommendations | | | | | | |
| f_P | Crystal Parallel Resonance Frequency at 12 pF Load Capacitance | | | 18.432 | | MHz |
| R_R | Crystal Series Resistance | | | 8 | 25 | Ω |
| C_0 | Crystal Shunt (Parallel) Capacitance | | | 6.2 | 7.0 | pF |
| C_L | External Load Capacitance ¹⁾ | XTAL_IN, XTAL_OUT | PSDIP PMQFP | approx. 1.5 approx. 3.3 | | pF pF |
| Crystal Recommendations for Master-Slave Applications (MSP-clock must perform synchronization to I ² S clock) | | | | | | |
| f_{TOL} | Accuracy of Adjustment | | -20 | | +20 | ppm |
| D_{TEM} | Frequency Variation versus Temperature | | -20 | | +20 | ppm |
| C_1 | Motional (Dynamic) Capacitance | | 19 | 24 | | fF |
| f_{CL} | Required Open Loop Clock Frequency ($T_{amb} = 25\text{ }^\circ\text{C}$) | AUD_CL_OUT | 18.431 | | 18.433 | MHz |
| Crystal Recommendations for FM / NICAM Applications (No MSP-clock synchronization to I ² S clock possible) | | | | | | |
| f_{TOL} | Accuracy of Adjustment | | -30 | | +30 | ppm |
| D_{TEM} | Frequency Variation versus Temperature | | -30 | | +30 | ppm |
| C_1 | Motional (Dynamic) Capacitance | | 15 | | | fF |
| f_{CL} | Required Open Loop Clock Frequency ($T_{amb} = 25\text{ }^\circ\text{C}$) | AUD_CL_OUT | 18.4305 | | 18.4335 | MHz |
| Crystal Recommendations for all analog FM/AM Applications (No MSP-clock synchronization to I ² S clock possible) | | | | | | |
| f_{TOL} | Accuracy of Adjustment | | -100 | | +100 | ppm |
| D_{TEM} | Frequency Variation versus Temperature | | -50 | | +50 | ppm |
| f_{CL} | Required Open Loop Clock Frequency ($T_{amb} = 25\text{ }^\circ\text{C}$) | AUD_CL_OUT | 18.429 | | 18.435 | MHz |
| Amplitude Recommendation for Operation with External Clock Input (C_{load} after reset typ. 22 pF) | | | | | | |
| V_{XCA} | External Clock Amplitude | XTAL_IN | 0.7 | | | V_{pp} |
| <p>¹⁾ External capacitors at each crystal pin to ground are required. They are necessary to tune the open-loop frequency of the internal PLL and to stabilize the frequency in closed-loop operation. Due to different layouts, <u>the accurate capacitor value should be determined with the customer PCB</u>. The suggested values (1.5...3.3 pF) are figures based on experience and should serve as "start value".</p> <p>To adjust the capacitor value, reset the MSP. After the reset, no I²C telegrams should be transmitted. Measure the frequency at AUD_CL_OUT-pin. Change the capacitor value until the free running frequency matches 18.432 MHz as closely as possible. The higher the capacity, the lower the resulting clock frequency.</p> <p>Note: To minimize adjustment tolerances for all MSP-generations, it is strongly recommended to use the so-called MSP-XTAL-REF ICs (available in all packages) for the capacitor adjustment.</p> | | | | | | |

4.6.3. Characteristics

at $T_A = 0$ to $70\text{ }^{\circ}\text{C}$, $f_{\text{CLOCK}} = 18.432\text{ MHz}$, $V_{\text{SUP1}} = 7.6$ to 8.7 V , $V_{\text{SUP2}} = 4.75$ to 5.25 V for min./max. values
 at $T_A = 60\text{ }^{\circ}\text{C}$, $f_{\text{CLOCK}} = 18.432\text{ MHz}$, $V_{\text{SUP1}} = 8\text{ V}$, $V_{\text{SUP2}} = 5\text{ V}$ for typical values,

T_J = Junction Temperature

MAIN (M) = Loudspeaker Channel, AUX (A) = Headphone Channel

4.6.3.1. General Characteristics

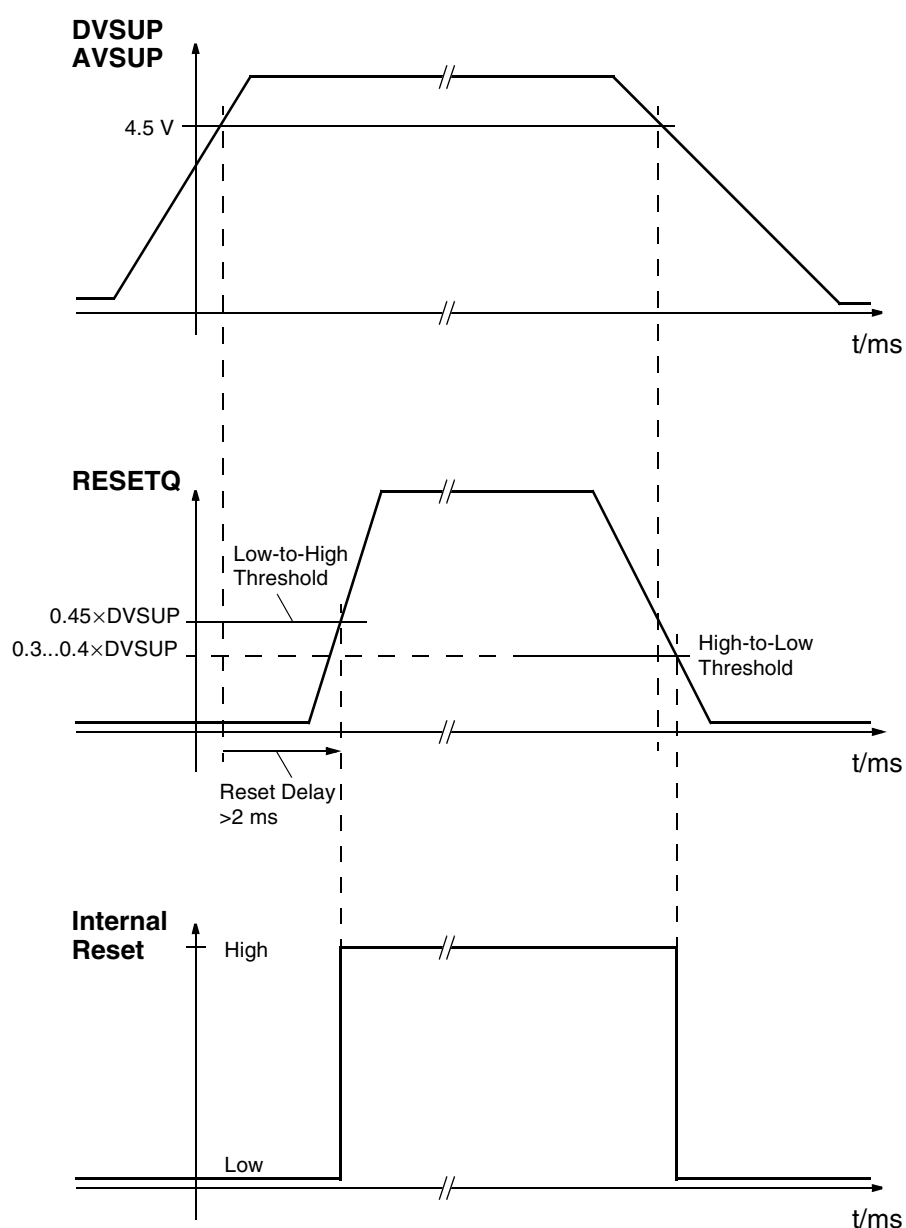
| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|------------------------|--|----------------------|--------------|----------|----------|-------------------|--|
| | | | Min. | Typ. | Max. | | |
| Supply | | | | | | | |
| I _{SUP1A} | First Supply Current (active) (AHVSUP = 8 V) | AHVSUP | | 17 11 | 25 16 | mA mA | Vol. Main and Aux = 0 dB Vol. Main and Aux = -30dB |
| | First Supply Current (active) (AHVSUP = 5 V) | | | 11 8 | 17 11 | mA mA | Vol. Main and Aux = 0 dB Vol. Main and Aux = -30 dB |
| I _{SUP2A} | Second Supply Current (active) | DVSUP | | 75 | 100 | mA | |
| I _{SUP3A} | Third Supply Current (active) | AVSUP | | 35 | 45 | mA | |
| I _{SUP1S} | First Supply Current (AHVSUP = 8 V) | AHVSUP | | 5.6 | 7.7 | mA | STANDBYQ = low |
| | First Supply Current (AHVSUP = 5 V) | | | 3.7 | 5.1 | mA | |
| Clock | | | | | | | |
| f _{CLOCK} | Clock Input Frequency | XTAL_IN | | 18.432 | | MHz | |
| D _{CLOCK} | Clock High to Low Ratio | | 45 | | 55 | % | |
| t _{JITTER} | Clock Jitter (Verification not provided in Production Test) | | | | 50 | ps | |
| V _{xtalDC} | DC-Voltage Oscillator | | | 2.5 | | V | |
| t _{Startup} | Oscillator Startup Time at VDD Slew-rate of 1 V/1 μs | XTAL_IN, XTAL_OUT | | 0.4 | 2 | ms | |
| V _{ACLKAC} | Audio Clock Output AC Voltage | AUD_CL_OUT | 1.2 | 1.8 | | V _{pp} | load = 40 pF |
| V _{ACLKDC} | Audio Clock Output DC Voltage | | 0.4 | | 0.6 | V _{SUP3} | I _{max} = 0.2 mA |
| r _{outHF_ACL} | HF Output Resistance | | | 140 | | Ω | |

4.6.3.2. Digital Inputs, Digital Outputs

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|-----------------------|----------------------------------|----------------------------|---------------------------|------|------|-------------------|--|
| | | | Min. | Typ. | Max. | | |
| Digital Input Levels | | | | | | | |
| V _{DIGIL} | Digital Input Low Voltage | STANDBYQ D_CTR_I/O_0/1 | | | 0.2 | V _{SUP2} | |
| V _{DIGIH} | Digital Input High Voltage | | 0.5 | | | V _{SUP2} | |
| Z _{DIGI} | Input Impedance | | | | 5 | pF | |
| I _{DLEAK} | Digital Input Leakage Current | | −1 | | 1 | μA | 0 V < U _{INPUT} < DVSUP D_CTR_I/O_0/1: tri-state |
| V _{DIGIL} | Digital Input Low Voltage | ADR_SEL | | | 0.2 | V _{SUP2} | |
| V _{DIGIH} | Digital Input High Voltage | | 0.8 | | | V _{SUP2} | |
| I _{ADRSEL} | Input Current Address Select Pin | | −500 | −220 | | μA | U _{ADR_SEL} = DVSS |
| | | | | 220 | 500 | μA | U _{ADR_SEL} = DVSUP |
| Digital Output Levels | | | | | | | |
| V _{DCTROL} | Digital Output Low Voltage | D_CTR_I/O_0 D_CTR_I/O_1 | | | 0.4 | V | IDDCTR = 1 mA |
| V _{DCTROH} | Digital Output High Voltage | | V _{SUP2} −0.3 | | | V | IDDCTR = −1 mA |

4.6.3.3. Reset Input and Power-Up

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---------------------|-----------------------------------|----------|--------------|------|------|-------------------|----------------------------------|
| | | | Min. | Typ. | Max. | | |
| RESETQ Input Levels | | | | | | | |
| V _{RHL} | Reset High-Low Transition Voltage | RESETQ | 0.3 | | 0.4 | V _{SUP2} | |
| V _{RLH} | Reset Low-High Transition Voltage | | | 0.45 | | V _{SUP2} | |
| Z _{RES} | Input Impedance | | | | 5 | pF | |
| I _{RES} | Input Pin Leakage Current | | | | 20 | μA | 0 V < U _{INPUT} < DVSUP |



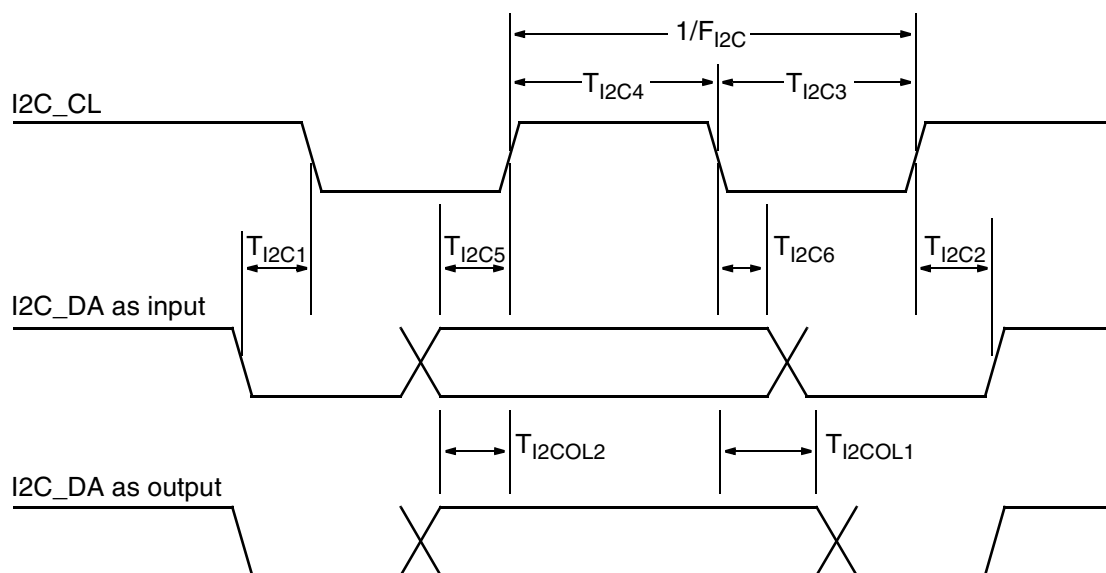
Note: The reset should not reach high level before the oscillator has started. This requires a reset delay of >2 ms

0.45 x DVSUP means
2.25 Volt with
DVSUP = 5.0 V

Fig. 4-22: Power-up sequence

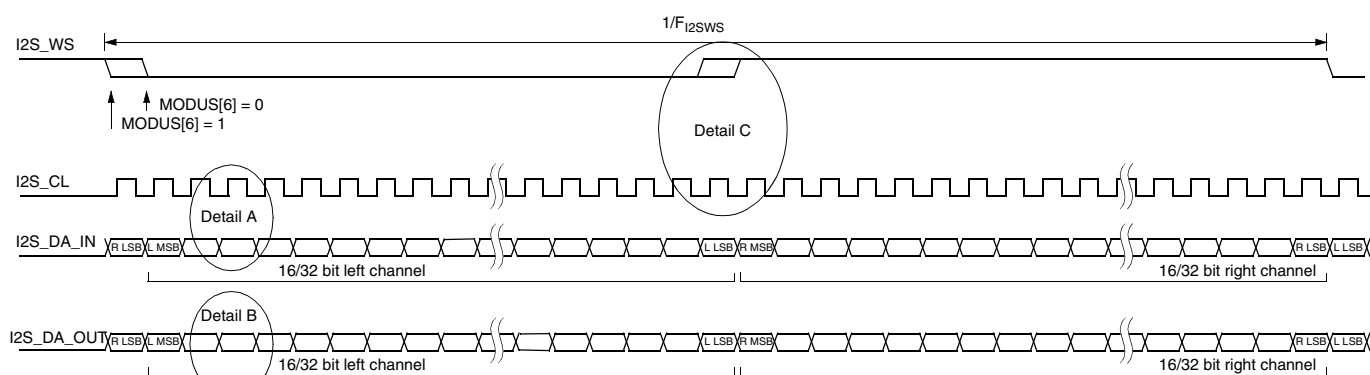
4.6.3.4. I²C-Bus Characteristics

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---------------------|---|-------------------|--------------|------|------|-------------------|---------------------------|
| | | | Min. | Typ. | Max. | | |
| V _{I2CIL} | I ² C-Bus Input Low Voltage | I2C_CL, I2C_DA | | | 0.3 | V _{SUP2} | |
| V _{I2CIH} | I ² C-Bus Input High Voltage | | 0.6 | | | V _{SUP2} | |
| t _{I2C1} | I ² C Start Condition Setup Time | | 120 | | | ns | |
| t _{I2C2} | I ² C Stop Condition Setup Time | | 120 | | | ns | |
| t _{I2C5} | I ² C-Data Setup Time before Rising Edge of Clock | | 55 | | | ns | |
| t _{I2C6} | I ² C-Data Hold Time after Falling Edge of Clock | | 55 | | | ns | |
| t _{I2C3} | I ² C-Clock Low Pulse Time | I2C_CL | 500 | | | ns | |
| t _{I2C4} | I ² C-Clock High Pulse Time | | 500 | | | ns | |
| f _{I2C} | I ² C-BUS Frequency | | | | 1.0 | MHz | |
| V _{I2COL} | I ² C-Data Output Low Voltage | I2C_CL, I2C_DA | | | 0.4 | V | I _{I2COL} = 3 mA |
| I _{I2COH} | I ² C-Data Output High Leakage Current | | | | 1.0 | μA | V _{I2COH} = 5 V |
| t _{I2COL1} | I ² C-Data Output Hold Time after Falling Edge of Clock | | 15 | | | ns | |
| t _{I2COL2} | I ² C-Data Output Setup Time before Rising Edge of Clock | | 100 | | | ns | f _{I2C} = 1 MHz |

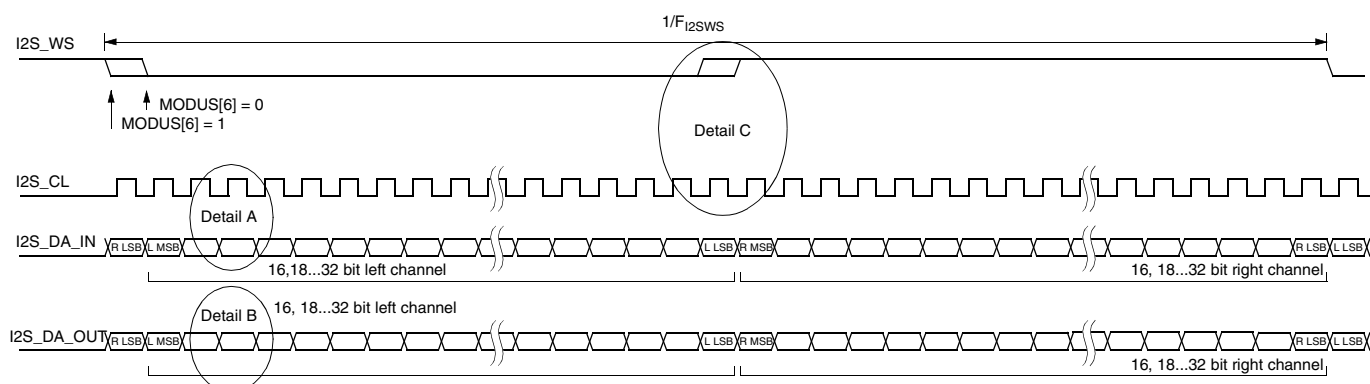
Fig. 4-23: I²C bus timing diagram

4.6.3.5. I²S-Bus Characteristics

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--------------------------|---|----------------------------------|-------------------------|----------------|-------|-------------------|--|
| | | | Min. | Typ. | Max. | | |
| V _{I2SIL} | Input Low Voltage | I2S_CL I2S_WS I2S_DA_IN1/2 | | | 0.2 | V _{SUP2} | |
| V _{I2SIH} | Input High Voltage | | 0.5 | | | V _{SUP2} | |
| Z _{I2SI} | Input Impedance | | | | 5 | pF | |
| I _{LEAKI2S} | Input Leakage Current | | −1 | | 1 | μA | 0 V < U _{INPUT} < DVSUP |
| V _{I2SOL} | I ² S Output Low Voltage | I2S_CL I2S_WS I2S_DA_OUT | | | 0.4 | V | I _{I2SOL} = 1 mA |
| V _{I2SOH} | I ² S Output High Voltage | | V _{SUP2} − 0.3 | | | V | I _{I2SOH} = −1 mA |
| f _{I2SOWS} | I ² S-Word Strobe Output Frequency | I2S_WS | | 32.0 | | kHz | |
| f _{I2SOCL} | I ² S-Clock Output Frequency | I2S_CL | | 1.024 2.048 | | MHz MHz | I2S_CONFIG[0] = 0 I2S_CONFIG[0] = 1 |
| R _{I2S10/I2S20} | I ² S-Clock Output High/Low-Ratio | | 0.9 | 1.0 | 1.1 | | |
| t _{s_I2S} | I ² S Input Setup Time before Rising Edge of Clock | I2S_CL I2S_DA_IN1/2 | 12 | | | ns | for details see Fig. 4–24 “I ² S bus timing diagram” |
| t _{h_I2S} | I ² S Input Hold Time after Rising Edge of Clock | | 40 | | | ns | |
| t _{d_I2S} | I ² S Output Delay Time after Falling Edge of Clock | I2S_CL I2S_WS I2S_DA_OUT | | | 28 | ns | C _L = 30 pF |
| f _{I2SWS} | I ² S-Word Strobe Input Frequency | I2S_WS | | 32.0 | | kHz | |
| f _{I2SCL} | I ² S-Clock Input Frequency | I2S_CL | | 1.024 | 2.048 | MHz | |
| R _{I2SCL} | I ² S-Clock Input Ratio | | 0.9 | | 1.1 | | |

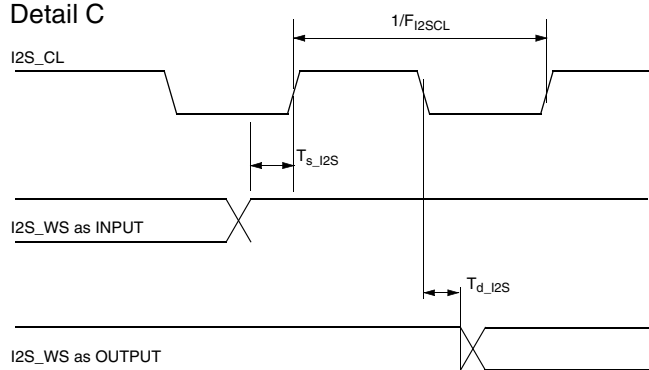


Data: MSB first, I²S master



Data: MSB first, I²S slave

Detail C



Detail A,B

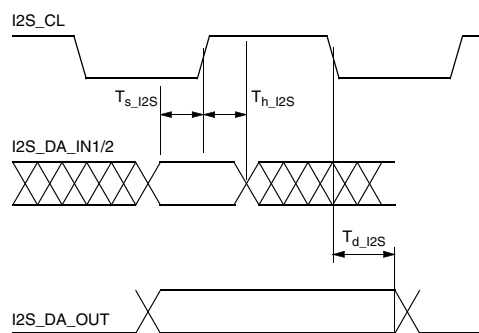


Fig. 4-24: I²S bus timing diagram

4.6.3.6. Analog Baseband Inputs and Outputs, AGNDC

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--|---|--|--------------|------|------------|------------------|--|
| | | | Min. | Typ. | Max. | | |
| Analog Ground | | | | | | | |
| V _{AGNDC0} | AGNDC Open Circuit Voltage (AHVSUP = 8 V) | AGNDC | | 3.77 | | V | R _{load} ≥ 10 MΩ |
| | AGNDC Open Circuit Voltage (AHVSUP = 5 V) | | | 2.51 | | V | |
| R _{outAGN} | AGNDC Output Resistance (AHVSUP = 8 V) | | 70 | 125 | 180 | kΩ | 3 V ≤ V _{AGNDC} ≤ 4 V |
| | AGNDC Output Resistance (AHVSUP = 5 V) | | 47 | 83 | 120 | kΩ | |
| Analog Input Resistance | | | | | | | |
| R _{inSC} | SCART Input Resistance from T _A = 0 to 70 °C | SCn_IN_s ¹⁾ | 25 | 40 | 58 | kΩ | f _{signal} = 1 kHz, I = 0.05 mA |
| R _{inMONO} | MONO Input Resistance from T _A = 0 to 70 °C | MONO_IN | 15 | 24 | 35 | kΩ | f _{signal} = 1 kHz, I = 0.1 mA |
| Audio Analog-to-Digital-Converter | | | | | | | |
| V _{AICL} | Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 8 V) | SCn_IN_s, ¹⁾ MONO_IN | 2.00 | | 2.25 | V _{RMS} | f _{signal} = 1 kHz |
| | Analog Input Clipping Level for Analog-to-Digital-Conversion (AHVSUP = 5 V) | | 1.13 | | 1.51 | V _{RMS} | |
| SCART Outputs | | | | | | | |
| R _{outSC} | SCART Output Resistance | SCn_OUT_s ¹⁾ | 200 200 | 330 | 460 500 | Ω Ω | f _{signal} = 1 kHz, I = 0.1 mA T _j = 27 °C T _A = 0 to 70 °C |
| dV _{OUTSC} | Deviation of DC-Level at SCART Output from AGNDC Voltage | | −70 | | +70 | mV | |
| A _{SCtoSC} | Gain from Analog Input to SCART Output | SCn_IN_s, ¹⁾ MONO_IN → SCn_OUT_s ¹⁾ | −1.0 | | +0.5 | dB | f _{signal} = 1 kHz |
| f _{rSCtoSC} | Frequency Response from Analog Input to SCART Output | | −0.5 | | +0.5 | dB | with resp. to 1 kHz Bandwidth: 0 to 20000 Hz |
| V _{outSC} | Signal Level at SCART Output (AHVSUP = 8 V) | SCn_OUT_s ¹⁾ | 1.8 | 1.9 | 2.0 | V _{RMS} | f _{signal} = 1 kHz Volume 0 dB Full Scale input from I ² S |
| | Signal Level at SCART Output (AHVSUP = 5 V) | | 1.17 | 1.27 | 1.37 | V _{RMS} | |
| 1) “n” means “1”, “2”, “3”, or “4”; “s” means “L” or “R” | | | | | | | |

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--|--|---------------------------------|--------------|-----------------|------------------|--|--|
| | | | Min. | Typ. | Max. | | |
| Main, AUX, and CS Outputs | | | | | | | |
| R _{outMA} | Main/AUX Output Resistance | DACM_r, ¹⁾ DACA_s | 2.1 2.1 | 3.3 | 4.6 5.0 | kΩ kΩ | f _{signal} = 1 kHz, I = 0.1 mA T _j = 27 °C T _A = 0 to 70 °C |
| V _{outDCMA} | DC-Level at Main/AUX-Output | | 1.80 | 2.04 61 0 | 2.28 | V mV V | Volume 0 dB Volume –30 dB |
| | DC-Level, not selected CS-Output (AHVSUP = 8 V) | | | | | | |
| V _{outDCMA} | DC-Level at Main/AUX-Output | | 1.12 | 1.36 40 0 | 1.60 | V mV V | Volume 0 dB Volume –30 dB |
| | DC-Level, not selected CS-Output (AHVSUP = 5 V) | | | | | | |
| V _{outMACS} | Signal Level at Main/AUX-Output (AHVSUP = 8 V) | 1.23 | 1.37 | 1.51 | V _{RMS} | f _{signal} = 1 kHz Volume = 0 dB Full Scale input from I ² S | |
| | Signal Level at Main/AUX-Output (AHVSUP = 5 V) | 0.76 | 0.90 | 1.04 | V _{RMS} | | |
| 1) “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

4.6.3.7. Sound IF Inputs

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|-----------------------|-------------------------|-----------------------------------|--------------|----------|-------------|----------|---|
| | | | Min. | Typ. | Max. | | |
| R _{IFIN} | Input Impedance | ANA_IN1+, ANA_IN2+, ANA_IN- | 1.5 6.8 | 2 9.1 | 2.5 11.4 | kΩ kΩ | Gain AGC = 20 dB Gain AGC = 3 dB |
| DC _{VREFTOP} | DC Voltage at VREFTOP | VREFTOP | 2.45 | 2.65 | 2.75 | V | |
| DC _{ANA_IN} | DC Voltage on IF Inputs | ANA_IN1+, ANA_IN2+, ANA_IN- | 1.3 | 1.5 | 1.7 | V | |
| XTALK _{IF} | Crosstalk Attenuation | ANA_IN1+, ANA_IN2+, ANA_IN- | 40 | | | dB | f _{signal} = 1 MHz Input Level = -2 dBr |
| BW _{IF} | 3 dB Bandwidth | | 10 | | | MHz | |
| AGC | AGC Step Width | | | 0.85 | | dB | |

4.6.3.8. Power Supply Rejection

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---|---|---|--------------|------|------|------|-----------------|
| | | | Min. | Typ. | Max. | | |
| PSRR: Rejection of Noise on AHVSUP at 1 kHz | | | | | | | |
| PSRR | AGNDC | AGNDC | | 80 | | dB | |
| | From Analog Input to I ² S Output | MONO_IN, SCn_IN_s ¹⁾ | | 70 | | dB | |
| | From Analog Input to SCART Output | MONO_IN, SCn_IN_s ¹⁾ SCn_OUT_s ¹⁾ | | 70 | | dB | |
| | From I ² S Input to SCART Output | SCn_OUT_s ¹⁾ | | 60 | | dB | |
| | From I ² S Input to Main or AUX Output | DACM_r, ¹⁾ DACA_s | | 80 | | dB | |
| 1) “n” means “1”, “2”, “3”, or “4”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

4.6.3.9. Analog Performance

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---|--|--|--------------|----------|------|----------|---|
| | | | Min. | Typ. | Max. | | |
| Specifications for AHVSUP = 8 V | | | | | | | |
| SNR | Dynamic Range and Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to I ² S Output | MONO_IN, SCn_IN_s ¹⁾ | 88 | 93 | | dB | Input Level = −20 dB with resp. to V _{AICL} , f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s ¹⁾ → SCn_OUT_s ¹⁾ | 93 | 96 | | dB | Input Level = −20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz... 20 kHz |
| | from I ² S Input to SCART Output | SCn_OUT_s ¹⁾ | 88 | 93 | | dB | Input Level = −20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| | from I ² S Input to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at −30 dB | DACM_r, ¹⁾ DACA_s | 88 81 | 93 86 | | dB dB | Input Level = −20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to I ² S Output | MONO_IN, SCn_IN_s ¹⁾ | | 0.008 | 0.03 | % | Input Level = −3 dBr with resp. to V _{AICL} , f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s → SCn_OUT_s ¹⁾ | | 0.008 | 0.03 | % | Input Level = −3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz... 20 kHz |
| | from I ² S Input to SCART Output | SCn_OUT_s ¹⁾ | | 0.008 | 0.03 | % | Input Level = −3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| | from I ² S Input to Main or AUX Output | DACM_r, ¹⁾ DACA_s | | 0.008 | 0.03 | % | Input Level = −3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| 1) “n” means “1”, “2”, “3”, or “4”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---|---|--|--------------|----------|------|----------|--|
| | | | Min. | Typ. | Max. | | |
| Specifications for AHVSUP = 5 V | | | | | | | |
| SNR | Dynamic Range and Signal-to-Noise Ratio | | | | | | |
| | from Analog Input to I ² S Output | MONO_IN, SCn_IN_s ¹⁾ | 85 | 90 | | dB | Input Level = –20 dB with resp. to V _{AICL} , f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s ¹⁾ → SCn_OUT_s ¹⁾ | 90 | 93 | | dB | Input Level = –20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz...20 kHz |
| | from I ² S Input to SCART Output | SCn_OUT_s ¹⁾ | 85 | 90 | | dB | Input Level = –20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| | from I ² S Input to Main/AUX-Output for Analog Volume at 0 dB for Analog Volume at –30 dB | DACM_r, ¹⁾ DACA_s | 85 78 | 90 83 | | dB dB | Input Level = –20 dB, f _{sig} = 1 kHz, A-weighted 20 Hz... 16 kHz |
| THD | Total Harmonic Distortion | | | | | | |
| | from Analog Input to I ² S Output | MONO_IN, SCn_IN_s ¹⁾ | | 0.03 | 0.1 | % | Input Level = –3 dBr with resp. to V _{AICL} , f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| | from Analog Input to SCART Output | MONO_IN, SCn_IN_s → SCn_OUT_s ¹⁾ | | | 0.1 | % | Input Level = –3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz...20 kHz |
| | from I ² S Input to SCART Output | SCn_OUT_s ¹⁾ | | | 0.1 | % | Input Level = –3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| | from I ² S Input to Main or AUX Output | DACA_s, DACM_s ¹⁾ | | | 0.1 | % | Input Level = –3 dBr, f _{sig} = 1 kHz, unweighted 20 Hz... 16 kHz |
| 1) “n” means “1”, “2”, “3”, or “4”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--------------------------|---|---|----------------------|------|----------------------|--|---|
| | | | Min. | Typ. | Max. | | |
| CROSSTALK Specifications | | | | | | | |
| XTALK | Crosstalk Attenuation | | | | | | Input Level = −3 dB, f _{sig} = 1 kHz, unused analog inputs connected to ground by Z < 1 kΩ |
| | between left and right channel within SCART Input/Output pair (L→R, R→L) SCn_IN → SCn_OUT ¹⁾ SC1_IN or SC2_IN → I ² S Output SC3_IN → I ² S Output I ² S Input → SCn_OUT ¹⁾ | 80 80 80 80 | | | dB dB dB dB | unweighted 20 Hz...20 kHz | |
| | between left and right channel within Main or AUX Output pair I ² S Input → DACM I ² S Input → DACA | 75 | | | dB | unweighted 20 Hz... 16 kHz | |
| | between SCART Input/Output pairs D = disturbing program O = observed program D: MONO/SCn_IN → SCn_OUT O: MONO/SCn_IN → SCn_OUT ¹⁾ D: MONO/SCn_IN → SCn_OUT or unsel. O: MONO/SCn_IN → I ² S Output D: MONO/SCn_IN → SCn_OUT O: I ² S Input → SCn_OUT ¹⁾ D: MONO/SCn_IN → unselected O: I ² S Input → SC1_OUT ¹⁾ | 100 95 100 100 | | | dB dB dB dB | unweighted 20 Hz...20 kHz same signal source on left and right disturbing channel, effect on each observed output channel | |
| | Crosstalk between Main and AUX Output pairs I ² S Input → DACM I ² S Input → DACA | 90 | | | dB | unweighted 20 Hz... 16 kHz same signal source on left and right disturbing channel, effect on each observed output channel | |
| | XTALK | Crosstalk from Main or AUX Output to SCART Output and vice versa D = disturbing program O = observed program D: MONO/SCn_IN/DSP → SCn_OUT O: I ² S Input → DACM O: I ² S Input → DACA D: MONO/SCn_IN/DSP → SCn_OUT O: I ² S Input → DACM O: I ² S Input → DACA D: I ² S Input → DACM D: I ² S Input → DACA O: MONO/SCn_IN → SCn_OUT ¹⁾ D: I ² S Input → DACM D: I ² S Input → DACA O: I ² S Input → SCn_OUT ¹⁾ | 80 85 95 95 | | | dB dB dB dB | unweighted 20 Hz...20 kHz same signal source on left and right disturbing channel, effect on each observed output channel SCART output load resistance 10 kΩ SCART output load resistance 30 kΩ |

1) “n” means “1”, “2”, “3”, or “4”

4.6.3.10. Sound Standard Dependent Characteristics

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--|--|--|--------------|------|------|------------------|--|
| | | | Min. | Typ. | Max. | | |
| NICAM Characteristics (MSP Standard Code = 8) | | | | | | | |
| dV _{NICAMOUT} | Tolerance of Output Voltage of NICAM Baseband Signal | DACM _r ¹⁾ DACA _s , SCn_OUT _s | −1.5 | | +1.5 | dB | 2.12 kHz, Modulator input level = 0 dBref |
| S/N _{NICAM} | S/N of NICAM Baseband Signal | | 72 | | | dB | NICAM: −6 dB, 1 kHz, RMS unweighted 0 to 16 kHz, Vol = 9 dB NIC_Presc = 7F _{hex} Output level 1 V _{RMS} |
| THD _{NICAM} | Total Harmonic Distortion + Noise of NICAM Baseband Signal | | | | 0.1 | % | 2.12 kHz, Modulator input level = 0 dBref |
| BER _{NICAM} | NICAM: Bit Error Rate | | | | 1 | 10 ^{−7} | FM+NICAM, norm conditions |
| fR _{NICAM} | NICAM Frequency Response , 20...15000 Hz | | −1.0 | | +1.0 | dB | Modulator input level = −12 dB dBref; RMS |
| XTALK _{NICAM} | NICAM Crosstalk Attenuation (Dual) | | 80 | | | dB | |
| SEP _{NICAM} | NICAM Channel Separation (Stereo) | 80 | | | | dB | |
| FM Characteristics (MSP Standard Code = 3) | | | | | | | |
| dV _{FMOUT} | Tolerance of Output Voltage of FM Demodulated Signal | DACM _r ¹⁾ DACA _s , SCn_OUT _s ¹⁾ | −1.5 | | +1.5 | dB | 1 FM-carrier, 50 μs, 1 kHz, 40 kHz deviation; RMS |
| S/N _{FM} | S/N of FM Demodulated Signal | | 73 | | | dB | 1 FM-carrier 5.5 MHz, 50 μs, 1 kHz, 40 kHz deviation; RMS, unweighted 0 to 15 kHz (for S/N); full input range, FM-Prescale = 46 _{hex} , Vol = 0 dB → Output Level 1 V _{RMS} |
| THD _{FM} | Total Harmonic Distortion + Noise of FM Demodulated Signal | | | | 0.1 | % | |
| fR _{FM} | FM Frequency Response 20...15000 Hz | | −1.0 | | +1.0 | dB | 1 FM-carrier 5.5 MHz, 50 μs, Modulator input level = −14.6 dBref; RMS |
| XTALK _{FM} | FM Crosstalk Attenuation (Dual) | | 80 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 μs, 1 kHz, 40 kHz deviation; Bandpass 1 kHz |
| SEP _{FM} | FM Channel Separation (Stereo) | DACM _r ¹⁾ DACA _s , SCn_OUT _s | 50 | | | dB | 2 FM-carriers 5.5/5.74 MHz, 50 μs, 1 kHz, 40 kHz deviation; RMS |
| AM Characteristics (MSP Standard Code = 9) | | | | | | | |
| S/N _{AM(1)} | S/N of AM Demodulated Signal measurement condition: RMS/Flat | DACM _r ¹⁾ DACA _s , SCn_OUT _s | 55 | | | dB | SIF level: 0.1–0.8 V _{pp} AM-carrier 54% at 6.5 MHz Vol = 0 dB, FM/AM prescaler set for output = 0.5 V _{RMS} at Loudspeaker out; Standard Code = 09 _{hex} no video/chroma components |
| S/N _{AM(2)} | S/N of AM Demodulated Signal measurement condition: QP/CCIR | | 45 | | | dB | |
| THD _{AM} | Total Harmonic Distortion + Noise of AM Demodulated Signal | | | | 0.6 | % | |
| fR _{AM} | AM Frequency Response 50...12000 Hz | | −2.5 | | +1.0 | dB | |
| 1) “n” means “1” or “2”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|---|---|---|--------------|------|--------|------|--|
| | | | Min. | Typ. | Max. | | |
| BTSC Characteristics (MSP Standard Code = 20 _{hex} , 21 _{hex}) | | | | | | | |
| S/N _{BTSC} | S/N of BTSC Stereo Signal | DACM_r, ¹⁾ DACA_s, SCn_OUT_s | 68 | | | dB | 1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz |
| | S/N of BTSC-SAP Signal | | 57 | | | dB | |
| THD _{BTSC} | THD+N of BTSC Stereo Signal | | | | 0.1 | % | 1 kHz L or R or SAP, 100% modulation, 75 μs EIM ²⁾ , DBX NR, RMS unweighted 0 to 15 kHz |
| | THD+N of BTSC SAP Signal | | | | 0.5 | % | |
| f _R _{DBX} | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | -1.0 | | 1.0 | dB | L or R or SAP, 1%...66% EIM ²⁾ , DBX NR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | -1.0 | | 1.0 | dB | |
| f _R _{MNR} | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | -2.0 | | 2.0 | dB | L or R 5%...66% EIM ²⁾ , MNR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | -2.0 | | 2.0 | dB | |
| XTALK _{BTSC} | Stereo → SAP | | 76 | | | dB | 1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, Bandpass 1 kHz |
| | SAP → Stereo | | 80 | | | dB | |
| SEP _{DBX} | Stereo Separation DBX NR 50 Hz...10 kHz | | 35 | | | dB | L or R 1%...66% EIM ²⁾ , DBX NR |
| | 50 Hz...12 kHz | | 30 | | | dB | |
| SEP _{MNR} | Stereo Separation MNR | | 30 | | | dB | L = 300 Hz, R = 3.1 kHz 14% modulation, MNR |
| FM _{pil} | Pilot deviation threshold | ANA_IN1+, ANA_IN2+ | 3.2 | | 3.5 | kHz | 4.5 MHz carrier modulated with f _h = 15.743 kHz SIF level = 100 mV _{op} indication: STATUS Bit[6] |
| | Stereo off → on Stereo on → off | | 1.2 | | 1.5 | kHz | |
| f _{Pilot} | Pilot Frequency Range | | 15.563 | | 15.843 | kHz | standard BTSC stereo signal, sound carrier only |

1) “n” means “1” or “2”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R”

2) EIM refers to 75-μs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-μs preemphasis network.

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--|---|--|--------------|------|------|------|---|
| | | | Min. | Typ. | Max. | | |
| BTSC Characteristics (MSP Standard Code = 20 _{hex} , 21 _{hex}) with a minimum IF input signal level of 70 mVpp (measured without any video/chroma signal components) | | | | | | | |
| S/N _{BTSC} | S/N of BTSC Stereo Signal | DACM _r , ¹⁾ DACA _s , SCn_OUT _s | 64 | | | dB | 1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 |
| | S/N of BTSC-SAP Signal | | 55 | | | dB | |
| THD _{BTSC} | THD+N of BTSC Stereo Signal | | | | 0.15 | % | 1 kHz L or R or SAP, 100% modulation, 75 μs EIM ²⁾ , DBX NR, RMS unweighted 0 to 15 kHz |
| | THD+N of BTSC SAP Signal | | | | 0.8 | % | |
| f _R _{DBX} | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | -1.0 | | 1.0 | dB | L or R or SAP, 1%...66% EIM ²⁾ , DBX NR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | -1.0 | | 1.0 | dB | |
| f _R _{MNR} | Frequency Response of BTSC Stereo, 50 Hz...12 kHz | | -2.0 | | 2.0 | dB | L or R 5%...66% EIM ²⁾ , MNR |
| | Frequency Response of BTSC-SAP, 50 Hz...9 kHz | | -2.0 | | 2.0 | dB | SAP, white noise, 10% Modulation, MNR |
| XTALK _{BTSC} | Stereo → SAP | | 75 | | | dB | 1 kHz L or R or SAP, 100% modulation, 75 μs deemphasis, Bandpass 1 kHz |
| | SAP → Stereo | | 75 | | | dB | |
| SEP _{DBX} | Stereo Separation DBX NR 50 Hz...10 kHz | | 35 | | | dB | L or R 1%...66% EIM ²⁾ , DBX NR |
| | 50 Hz...12 kHz | | 30 | | | dB | |
| SEP _{MNR} | Stereo Separation MNR | | 30 | | | dB | L = 300 Hz, R = 3.1 kHz 14% modulation, MNR |

1) "n" means "1" or "2"; "r" means "L", "R", "C", or "S"; "s" means "L" or "R"

2) EIM refers to 75-μs Equivalent Input Modulation. It is defined as the audio-signal level which results in a stated percentage modulation, when the DBX encoding process is replaced by a 75-μs preemphasis network.

| Symbol | Parameter | Pin Name | Limit Values | | | Unit | Test Conditions |
|--|--|--|--|----------|------------|----------|---|
| | | | Min. | Typ. | Max. | | |
| EIA-J Characteristics (MSP Standard Code = 30 _{hex}) | | | | | | | |
| S/N _{EIAJ} | S/N of EIA-J Stereo Signal S/N of EIA-J Sub-Channel | DACM _r , ¹⁾ DACA _s , SCn_OUT _s | 60 60 | | | dB dB | 1 kHz L or R, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz |
| THD _{EIAJ} | THD+N of EIA-J Stereo Signal THD+N of EIA-J Sub-Channel | | | | 0.2 0.3 | % % | |
| f _R _{EIAJ} | Frequency Response of EIA-J Stereo, 50 Hz...12 kHz | | −1.0 | | 1.0 | dB | 100% modulation, 75 μs deemphasis |
| | Frequency Response of EIA-J Sub-Channel, 50 Hz...12 kHz | | −1.0 | | 1.0 | dB | |
| XTALK _{EIAJ} | Main → SUB Sub → MAIN | | 66 80 | | | dB dB | 1 kHz L or R, 100% modulation, 75 μs deemphasis, Bandpass 1 kHz |
| | SEP _{EIAJ} | | Stereo Separation 50 Hz...5 kHz 50 Hz...10 kHz | 35 28 | | | |
| FM-Radio Characteristics (MSP Standard Code = 40 _{hex}) | | | | | | | |
| S/N _{UKW} | S/N of FM-Radio Stereo Signal | DACM _r , ¹⁾ DACA _s , SCn_OUT _s | 68 | | | dB | 1 kHz L or R, 100% modulation, 75 μs deemphasis, RMS unweighted 0 to 15 kHz |
| THD _{UKW} | THD+N of FM-Radio Stereo Signal | | | | 0.1 | % | |
| f _R _{UKW} | Frequency Response of FM-Radio Stereo 50 Hz...15 kHz | | −1.0 | | 1.0 | dB | L or R, 1%...100% modulation, 75 μs deemphasis |
| SEP _{UKW} | Stereo Separation 50 Hz...15 kHz | | 45 | | | dB | |
| f _{Pilot} | Pilot Frequency Range | ANA_IN1+ ANA_IN2+ | 18.844 | | 19.125 | kHz | standard FM radio stereo signal |
| 1) “n” means “1” or “2”; “r” means “L”, “R”, “C”, or “S”; “s” means “L” or “R” | | | | | | | |

5. Appendix A: Overview of TV-Sound Standards

5.1. NICAM 728

Table 5–1: Summary of NICAM 728 sound modulation parameters

| Specification | I | B/G | L | | D/K | |
|--|--|--------------------|---|-------|--------------------|--------|
| Carrier frequency of digital sound | 6.552 MHz | 5.85 MHz | 5.85 MHz | | 5.85 MHz | |
| Transmission rate | 728 kbit/s | | | | | |
| Type of modulation | Differentially encoded quadrature phase shift keying (DQPSK) | | | | | |
| Spectrum shaping Roll-off factor | by means of Roll-off filters | | | | | |
| | 1.0 | 0.4 | 0.4 | | 0.4 | |
| Carrier frequency of analog sound component | 6.0 MHz FM mono | 5.5 MHz FM mono | 6.5 MHz AM mono terrestrial cable | | 6.5 MHz FM mono | |
| Power ratio between vision carrier and analog sound carrier | 10 dB | 13 dB | 10 dB | 16 dB | 13 dB | |
| Power ratio between analog and modulated digital sound carrier | 10 dB | 7 dB | 17 dB | 11 dB | China/ Hungary | Poland |
| | | | | | 12 dB | 7 dB |

Table 5–2: Summary of NICAM 728 sound coding characteristics

| Characteristics | Values |
|-------------------------------|--|
| Audio sampling frequency | 32 kHz |
| Number of channels | 2 |
| Initial resolution | 14 bit/sample |
| Companding characteristics | near instantaneous, with compression to 10 bits/sample in 32-samples (1 ms) blocks |
| Coding for compressed samples | 2's complement |
| Preemphasis | CCITT Recommendation J.17 (6.5 dB attenuation at 800 Hz) |
| Audio overload level | +12 dBm measured at the unity gain frequency of the preemphasis network (2 kHz) |

5.2. A2-Systems

Table 5–3: Key parameters for A2 Systems of Standards B/G, D/K, and M

| Characteristics | Sound Carrier FM1 | | | Sound Carrier FM2 | | |
|---------------------------------------|-------------------|-----|-------------|---|-------------------------------------|----------------------|
| TV-Sound Standard | B/G | D/K | M | B/G | D/K | M |
| Carrier frequency in MHz | 5.5 | 6.5 | 4.5 | 5.7421875 | 6.2578125 6.7421875 5.7421875 | 4.724212 |
| Vision/sound power difference | 13 dB | | | 20 dB | | |
| Sound bandwidth | 40 Hz to 15 kHz | | | | | |
| Preemphasis | 50 μs | | 75 μs | 50 μs | | 75 μs |
| Frequency deviation (nom/max) | ±27/±50 kHz | | ±17/±25 kHz | ±27/±50 kHz | | ±15/±25 kHz |
| Transmission Modes | | | | | | |
| Mono transmission | mono | | | mono | | |
| Stereo transmission | (L+R)/2 | | (L+R)/2 | R | | (L–R)/2 |
| Dual sound transmission | language A | | | language B | | |
| Identification of Transmission Mode | | | | | | |
| Pilot carrier frequency | | | | 54.6875 kHz | | 55.0699 kHz |
| Max. deviation portion | | | | ±2.5 kHz | | |
| Type of modulation / modulation depth | | | | AM / 50% | | |
| Modulation frequency | | | | mono: unmodulated stereo: 117.5 Hz dual: 274.1 Hz | | 149.9 Hz 276.0 Hz |

5.3. BTSC-Sound System

Table 5–4: Key parameters for BTSC-Sound Systems

| | Aural Carrier | BTSC-MPX-Components | | | | |
|--|-------------------|----------------------|-------|----------------------|--------------|-------------------|
| | | (L+R) | Pilot | (L–R) | SAP | Prof. Ch. |
| Carrier frequency ($f_{hNTSC} = 15.734 \text{ kHz}$) ($f_{hPAL} = 15.625 \text{ kHz}$) | 4.5 MHz | Baseband | f_h | $2 f_h$ | $5 f_h$ | $6.5 f_h$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | 0.05 - 10 | 0.05 - 3.4 |
| Preemphasis | | 75 μs | | DBX | DBX | 150 μs |
| Max. deviation to Aural Carrier | 73 kHz (total) | 25 kHz ¹⁾ | 5 kHz | 50 kHz ¹⁾ | 15 kHz | 3 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | | AM | 10 kHz FM | 3 kHz FM |
| ¹⁾ Sum does not exceed 50 kHz due to interleaving effects | | | | | | |

5.4. Japanese FM Stereo System (EIA-J)

Table 5–5: Key parameters for Japanese FM-Stereo Sound System EIA-J

| | Aural Carrier FM | EIA-J-MPX-Components | | |
|---|---------------------|----------------------|------------------|-----------------|
| | | (L+R) | (L–R) | Identification |
| Carrier frequency ($f_h = 15.734 \text{ kHz}$) | 4.5 MHz | Baseband | $2 f_h$ | $3.5 f_h$ |
| Sound bandwidth | | 0.05 - 15 kHz | 0.05 - 15 kHz | – |
| Preemphasis | | 75 μs | 75 μs | none |
| Max. deviation portion to Aural Carrier | 47 kHz | 25 kHz | 20 kHz | 2 kHz |
| Max. Freq. Deviation of Subcarrier Modulation Type | | | 10 kHz FM | 60% AM |
| Transmitter-sided delay | | 20 μs | 0 μs | 0 μs |
| Mono transmission | | L+R | – | unmodulated |
| Stereo transmission | | L+R | L–R | 982.5 Hz |
| Bilingual transmission | | Language A | Language B | 922.5 Hz |

5.5. FM Satellite Sound

Table 5–6: Key parameters for FM Satellite Sound

| Carrier Frequency | Maximum FM Deviation | Sound Mode | Bandwidth | Deemphasis |
|-------------------|----------------------|-----------------------|-----------|------------|
| 6.5 MHz | 85 kHz | Mono | 15 kHz | 50 μ s |
| 7.02/7.20 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.38/7.56 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |
| 7.74/7.92 MHz | 50 kHz | Mono/Stereo/Bilingual | 15 kHz | adaptive |

5.6. FM-Stereo Radio

Table 5–7: Key parameters for FM-Stereo Radio Systems

| | Aural Carrier | FM-Radio-MPX-Components | | | |
|--|------------------|--------------------------|-------|--------------------------|---------|
| | | (L+R) | Pilot | (L–R) | RDS/ARI |
| Carrier frequency ($f_p = 19$ kHz) | 10.7 MHz | Baseband | f_p | $2 f_p$ | $3 f_p$ |
| Sound bandwidth in kHz | | 0.05 - 15 | | 0.05 - 15 | |
| Preemphasis: – USA – Europe | | 75 μ s 50 μ s | | 75 μ s 50 μ s | |
| Max. deviation to Aural Carrier | 75 kHz (100%) | 90% ¹⁾ | 10% | 90% ¹⁾ | 5% |
| ¹⁾ Sum does not exceed 90% due to interleaving effects. | | | | | |

6. Appendix B: Manual/Compatibility Mode

To adapt the modes of the STANDARD SELECT register to individual requirements and for reasons of **compatibility to the MSP 34x0D**, the MSP 34x2G offers an Manual/Compatibility Mode, which provides sophisticated programming of the MSP 34x2G.

Using the STANDARD SELECT register generally provides a more economic way to program the MSP 34x2G and will result in optimal behavior. **Therefore, it is not recommended to use the Manual/Compatibility mode.** In those cases, where the MSP 34x0D is to be substituted by the MSP 34x2G, the tips given in Section 6.9. on page 109 have to be obeyed by the controller software.

6.1. Demodulator Write and Read Registers for Manual/Compatibility Mode

Table 6–1: Demodulator Write Registers; Subaddress: 10_{hex}; these registers are not readable!

| Demodulator Write Registers | Address (hex) | MSP-Version | Description | Reset Mode | Page |
|---|----------------------------------|-------------|--|----------------------|------|
| AUTO_FM/AM | 00 21 | 3412, 3452 | 1. MODUS[0]=1 (Automatic Sound Select): Switching Level threshold of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception 2. MODUS[0]=0 (Manual Mode): Activation and configuration of Automatic Switching between NICAM and FM/AM in case of bad NICAM reception | 00 00 | 97 |
| A2_Threshold | 00 22 | all | A2 Stereo Identification Threshold | 01 90 _{hex} | 99 |
| CM_Threshold | 00 24 | all | Carrier-Mute Threshold | 00 2A _{hex} | 99 |
| AD_CV | 00 BB | all | SIF-input selection, configuration of AGC, and Carrier-Mute Function | 00 00 | 100 |
| MODE_REG | 00 83 | 3412, 3452 | Controlling of MSP-Demodulator and Interface options. As soon as this register is applied, the MSP 34x2G works in the MSP 34x0D Compatibility Mode . Warning: In this mode, BTSC, EIA-J, and FM-Radio are disabled. Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x2G is reset to the normal mode by first programming the MODUS register followed by transmitting a valid standard code to the STANDARD SELECTION register. | 00 00 | 101 |
| FIR1 FIR2 | 00 01 00 05 | | FIR1-filter coefficients channel 1 (6 · 8 bit) FIR2-filter coefficients channel 2 (6 · 8 bit), + 3 · 8 bit offset (total 72 bit) | 00 00 | 103 |
| DCO1_LO DCO1_HI DCO2_LO DCO2_HI | 00 93 00 9B 00 A3 00 AB | | Increment channel 1 Low Part Increment channel 1 High Part Increment channel 2 Low Part Increment channel 2 High Part | 00 00 | 103 |
| PLL_CAPS | 00 1F | | Not of interest for the customer Switchable PLL capacitors to tune open-loop frequency | 00 56 | 106 |
| Note: All registers except AUTO_FM/AM, A2_Threshold and CM_Threshold are initialised during STANDARD SELECTION and are automatically updated when Automatic Sound Select (MODUS[0]=1) is on. | | | | | |

Table 6–2: Demodulator Read Registers; Subaddress: 11_{hex}; these registers are not writable!

| Demodulator Read Registers | Address (hex) | MSP-Version | Description | Page |
|----------------------------|---------------|-------------|--|------|
| C_AD_BITS | 00 23 | 3412, 3452 | NICAM-Sync bit, NICAM-C-Bits, and three LSBs of additional data bits | 105 |
| ADD_BITS | 00 38 | | NICAM: bit [10:3] of additional data bits | 105 |
| CIB_BITS | 00 3E | | NICAM: CIB1 and CIB2 control bits | 105 |
| ERROR_RATE | 00 57 | | NICAM error rate, updated with 182 ms | 106 |
| PLL_CAPS | 02 1F | | Not for customer use | 106 |
| AGC_GAIN | 02 1E | | Not for customer use | 106 |

6.2. DSP Write and Read Registers for Manual/Compatibility Mode

Table 6–3: DSP-Write Registers; Subaddress: 12_{hex}, all registers are readable as well

| Write Register | Address (hex) | Bits | Operational Modes and Adjustable Range | Reset Mode | Page |
|-----------------------------------|---------------|--------|--|-------------------|------|
| Volume SCART1 channel: Ctrl. mode | 00 07 | [7:0] | [Linear mode / logarithmic mode] | 00 _{hex} | 107 |
| FM Fixed Deemphasis | 00 0F | [15:8] | [50 μs, 75 μs, J17, OFF] | 50 μs | 107 |
| FM Adaptive Deemphasis | | [7:0] | [OFF, WP1] | OFF | 107 |
| Identification Mode | 00 15 | [7:0] | [B/G, M] | B/G | 108 |
| FM DC Notch | 00 17 | [7:0] | [ON, OFF] | ON | 108 |
| Volume SCART2 channel: Ctrl. mode | 00 40 | [7:0] | [Linear mode / logarithmic mode] | 00 _{hex} | 107 |

Table 6–4: DSP Read Registers; Subaddress: 13_{hex}, all registers are not writable

| Additional Read Registers | Address (hex) | Bits | Output Range | Page |
|---|---------------|--------|--|------|
| Stereo detection register for A2 Stereo Systems | 00 18 | [15:8] | [80 _{hex} ... 7F _{hex}] 8 bit two's complement | 108 |
| DC level readout FM1/Ch2-L | 00 1B | [15:0] | [8000 _{hex} ... 7FFF _{hex}] 16 bit two's complement | 108 |
| DC level readout FM2/Ch1-R | 00 1C | [15:0] | [8000 _{hex} ... 7FFF _{hex}] 16 bit two's complement | 108 |

6.3. Manual/Compatibility Mode: Description of Demodulator Write Registers

6.3.1. Automatic Switching between NICAM and Analog Sound

In case of bad NICAM reception or loss of the NICAM-carrier, the MSP 34x2G offers an Automatic Switching (fall back) to the analog sound (FM/AM-Mono), without the necessity of the controller reading and evaluating any parameters. If a proper NICAM signal returns, switching back to this source is performed automatically as well. The feature evaluates the NICAM ERROR_RATE and switches, if necessary, all output channels which are assigned to the NICAM source, to the analog source, and vice versa.

An appropriate hysteresis algorithm avoids oscillating effects (see Fig. 6–1). STATUS[9] and C_AD_BITS[11] (Addr: 0023 hex) provide information about the actual NICAM-FM/AM-status.

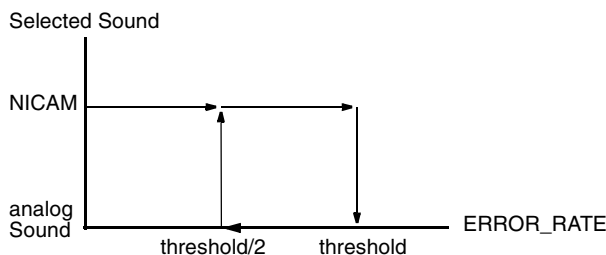


Fig. 6–1: Hysteresis for Automatic Switching

6.3.1.1. Function in Automatic Sound Select Mode

The Automatic Sound Select feature (MODUS[0]=1) includes the procedure mentioned above. By default, the internal ERROR_RATE threshold is set to 700_{dec}, i.e. :

- NICAM → analog Sound if ERROR_RATE > 700
- analog Sound → NICAM if ERROR_RATE < 700/2

The ERROR_RATE value of 700 corresponds to a BER of approximately $5.46 \cdot 10^{-3}/s$.

Individual configuration of the threshold can be done using Table 6–5. It is recommended to use the internal setting used by the standard selection.

The optimum NICAM sound can be assigned to the MSP output channels by selecting one of the “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels.

6.3.1.2. Function in Manual Mode

If the manual mode (MODUS[0]=0) is required, the activation and configuration of the Automatic Switching feature has to be done as described in Table 6–6. Note, that the channel matrix of the corresponding output channels must be set according to the NICAM mode and need not to be changed in the FM/AM-fallback case.

Example:

Required threshold = 500: bits [10:1]=00 1111 1010

Table 6–5: Coding of Automatic NICAM/Analog Sound Switching;
Automatic Sound Select is on (MODUS[0] = 1)

| Mode | Description | AUTO_FM [11:0] Addr. = 00 21 _{hex} | ERROR_RATE- Threshold/dec | Source Select: Input at NICAM Path ¹⁾ |
|--|---|---|---|---|
| 1 Default | Automatic Switching with internal threshold | bit[11:0] = 0 | 700 | NICAM or FM/AM, depending on ERROR_RATE |
| 2 | Automatic Switching with external threshold (Customizing of Automatic Sound Select) | bit[11] = 0 bit[10:1] = 25...1000 = threshold/2 bit[0] = 1 | set by customer; recommended range: 50...2000 | |
| 3 | Forced Analog Mono | bit [11] = 1 bit [10:1] = ignored bit [0] = 1 | | always FM/AM |
| ¹⁾ The NICAM path may be assigned to “Stereo or A/B”, “Stereo or A”, or “Stereo or B” source channels (see Table 2–2 on page 14). | | | | |

Table 6–6: Coding of Automatic NICAM/Analog Sound Switching;
Automatic Sound Select is off (MODUS[0] = 0)

| Mode | Description | AUTO_FM [11:0] Addr. = 00 21 _{hex} | ERROR_RATE- Threshold/dec | Source Select: Input at NICAM Path |
|----------------------|--|---|---|---|
| 0 reset status | Forced NICAM (Automatic Switching disabled) | bit[11] = 0 bit[10:1] = 0 bit[0] = 0 | none | always NICAM; Mute in case of no NICAM available |
| 1 | Automatic Switching with internal threshold (Default, if Automatic Sound Select is on) | bit[11] = 0 bit[10:1] = 0 bit[0] = 1 | 700 | NICAM or FM/AM, depending on ERROR_RATE |
| 2 | Automatic Switching with external threshold (Customizing of Automatic Sound Select) | bit[11] = 0 bit[10:1] = 25...1000 = threshold/2 bit[0] = 1 | set by customer; recommended range: 50...2000 | |
| 3 | Forced Analog Mono (Automatic Switching disabled) | bit[11] = 1 bit[10:1] = 0 bit[0] = 1 | none | always FM/AM |

6.3.2. A2 Threshold

The threshold between Stereo/Bilingual and Mono Identification for the A2 Standard has been made programmable according to the user's preferences. An internal hysteresis ensures robustness and stability.

Table 6–7: Write Register on I²C Subaddress 10_{hex} : A2 Threshold

| Register Address | Function | Name |
|------------------------------|---|-----------|
| THRESHOLDS | | |
| 00 22 _{hex} (write) | A2 THRESHOLD Register Defines threshold of all A2 and EIA_J standards for Stereo and Bilingual detection bit[15:0] 07F0 _{hex} force Mono Identification ... 0190 _{hex} default setting after reset ... 00A0 _{hex} minimum Threshold for stable detection recommended range : 00A0 _{hex} ...03C0 _{hex} | A2_THRESH |

6.3.3. Carrier-Mute Threshold

The Carrier-Mute threshold has been made programmable according to the user's preferences. An internal hysteresis ensures stable behavior.

Table 6–8: Write Register on I²C Subaddress 10_{hex} : Carrier-Mute Threshold

| Register Address | Function | Name |
|------------------------------|--|-----------|
| THRESHOLDS | | |
| 00 24 _{hex} (write) | Carrier-Mute THRESHOLD Register Defines threshold for the carrier mute feature bit[15:0] 0000 _{hex} Carrier-Mute always ON (both channels muted) ... 002A _{hex} default setting after reset ... 07FF _{hex} Carrier-Mute always OFF (both channels forced on) recommended range : 0014 _{hex} ...0050 _{hex} | CM_THRESH |

6.3.4. Register AD_CV

The use of this register is no longer recommended. Use it only in cases where compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x2G.

Table 6–9: AD_CV Register; reset status: all bits are “0”

| AD_CV (00 BB _{hex}) | | | Automatic setting by STANDARD SELECT Register | |
|--|---|---|--|--------|
| Bit | Function | Settings | 2-8, 0A-60 _{hex} | 9 |
| [0] | not used | must be set to 0 | 0 | 0 |
| [1–6] | Reference level in case of Automatic Gain Control = on (see Table 6–10). Constant gain factor when Automatic Gain Control = off (see Table 6–11). | | 101000 | 100011 |
| [7] | Determination of Automatic Gain or Constant Gain | 0 = constant gain 1 = automatic gain | 1 | 1 |
| [8] | Selection of Sound IF source (identical to MODUS[8]) | 0 = ANA_IN1+ 1 = ANA_IN2+ | X | X |
| [9] | MSP-Carrier-Mute Feature | 0 = off: no mute 1 = on: mute as described in section 2.2.2. | 1 | 1 |
| [10–15] | not used | must be set to 0 | 0 | 0 |
| X : not affected while choosing the TV sound standard by means of the STANDARD SELECT Register | | | | |

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Automatic Sound Select (MODUS[0]=1) is on.

Table 6–10: Reference Values for Active AGC (AD_CV[7] = 1)

| Application | Input Signal Contains | AD_CV [6:1] Ref. Value | AD_CV [6:1] in integer | Range of Input Signal at pin ANA_IN1+ and ANA_IN2+ |
|---|--------------------------|---------------------------|---------------------------|--|
| Terrestrial TV | | | | |
| – FM Standards | 1 or 2 FM Carriers | 101000 | 40 | 0.10 – 3 V _{pp} ¹⁾ |
| – NICAM/FM | 1 FM and 1 NICAM Carrier | 101000 | 40 | 0.10 – 3 V _{pp} ¹⁾ |
| – NICAM/AM | 1 AM and 1 NICAM Carrier | 100011 | 35 | 0.10 – 1.4 V _{pp} (recommended: 0.10 – 0.8 V _{pp}) |
| – NICAM only | 1 NICAM Carrier only | 010100 | 20 | 0.05 – 1.0 V _{pp} |
| SAT | 1 or more FM Carriers | 100011 | 35 | 0.10 – 3 V _{pp} ¹⁾ |
| ADR | FM and ADR carriers | see DRP 3510A data sheet | | |
| 1) For signals above 1.4 V _{pp} , the minimum gain of 3 dB is switched, and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 V _{pp} , if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear. | | | | |

Table 6–11: AD_CV parameters for Constant Input Gain (AD_CV[7]=0)

| Step | AD_CV [6:1] Constant Gain | Gain | Input Level at pin ANA_IN1+ and ANA_IN2+ |
|------|------------------------------|----------|--|
| 0 | 000000 | 3.00 dB | maximum input level: 3 V _{pp} (FM) or 1 V _{pp} (NICAM) ¹⁾ |
| 1 | 000001 | 3.85 dB | |
| 2 | 000010 | 4.70 dB | |
| 3 | 000011 | 5.55 dB | |
| 4 | 000100 | 6.40 dB | |
| 5 | 000101 | 7.25 dB | |
| 6 | 000110 | 8.10 dB | |
| 7 | 000111 | 8.95 dB | |
| 8 | 001000 | 9.80 dB | |
| 9 | 001001 | 10.65 dB | |
| 10 | 001010 | 11.50 dB | |
| 11 | 001011 | 12.35 dB | |
| 12 | 001100 | 13.20 dB | |
| 13 | 001101 | 14.05 dB | |
| 14 | 001110 | 14.90 dB | |
| 15 | 001111 | 15.75 dB | |
| 16 | 010000 | 16.60 dB | |
| 17 | 010001 | 17.45 dB | |
| 18 | 010010 | 18.30 dB | |
| 19 | 010011 | 19.15 dB | |
| 20 | 010100 | 20.00 dB | maximum input level: 0.14 V _{pp} |

¹⁾ For signals above 1.4 V_{pp}, the minimum gain of 3 dB is switched and overflow of the A/D converter may result. Due to the robustness of the internal processing, the IC works up to and even more than 3 V_{pp}, if norm conditions of FM/NICAM or FM1/FM2 ratio are supposed. In this overflow case, a loss of FM-S/N ratio of about 10 dB may appear.

6.3.5. Register MODE_REG

Note: The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x2G.

As soon as this register is applied, the MSP 34x2G works in the **MSP 34x0D Manual/Compatibility Mode**. In this mode, **BTSC, EIA-J, and FM-Radio are disabled**. Only MSP 34x0D features are available; the use of MODUS and STATUS register is not allowed. The MSP 34x2G is reset to the normal mode by first programming the MODUS register, followed by transmitting a valid standard code to the STANDARD SELECTION register.

The register 'MODE_REG' contains the control bits determining the operation mode of the MSP 34x2G in the MSP 34x0D Manual/Compatibility Mode; Table 6–12 explains all bit positions.

Table 6–12: Control word 'MODE_REG'; reset status: all bits are "0"

| MODE_REG 00 83 _{hex} | | | | Automatic setting by STANDARD SELECT Register | | |
|--|-------------------------------------|---|--|--|---------|---|
| Bit | Function | Comment | Definition | 2 - 5 | 8, A, B | 9 |
| [0] | not used | | 0 : must be used | 0 | 0 | 0 |
| [1] | DCTR_TRI | Digital control out 0/1 tri-state | 0 : active 1 : tri-state | X | X | X |
| [2] | I2S_TRI | I ² S outputs tri-state (I2S_CL, I2S_WS, I2S_DA_OUT) | 0 : active 1 : tri-state | X | X | X |
| [3] | I ² S Mode ¹⁾ | Master/Slave mode of the I ² S bus | 0 : Master 1 : Slave | X | X | X |
| [4] | I2S_WS Mode | WS due to the Sony or Philips-Format | 0 : Sony 1 : Philips | X | X | X |
| [5] | Audio_CL_OUT | Switch Audio_Clock_Output to tri-state | 0 : on 1 : tri-state | X | X | X |
| [6] | NICAM ¹⁾ | Mode of MSP-Ch1 | 0 : FM 1 : Nicam | 0 | 1 | 1 |
| [7] | not used | | 0 : must be used | 0 | 0 | 0 |
| [8] | FM AM | Mode of MSP-Ch2 | 0 : FM 1 : AM | 0 | 0 | 1 |
| [9] | HDEV | High Deviation Mode (channel matrix must be sound A) | 0 : normal 1 : high deviation mode | 0 | 0 | 0 |
| [11:10] | not used | | 0 : must be used | 0 | 0 | 0 |
| [12] | MSP-Ch1 Gain | see also Table 6–14 | 0 : Gain = 6 dB 1 : Gain = 0 dB | 0 | 0 | 0 |
| [13] | FIR1-Filter Coeff. Set | see also Table 6–14 | 0 : use FIR1 1 : use FIR2 | 1 | 0 | 0 |
| [14] | ADR | Mode of MSP-Ch1/ ADR-Interface | 0 : normal mode/tri-state 1 : ADR-mode/active | 0 | 0 | 0 |
| [15] | AM-Gain | Gain for AM Demodulation | 0 : 0 dB (default. of MSPB) 1 : 12 dB (recommended) | 1 | 1 | 1 |
| ¹⁾ NICAM and I ² S-Slave mode are not allowed simultaneously | | | | X: not affected by STANDARD SELECT Register | | |

Table 6–13: Loading sequence for FIR-coefficients

| FIR1 00 01 _{hex} (MSP-Ch1: NICAM/FM2) | | | |
|--|----------------------|------|-------------------|
| No. | Symbol Name | Bits | Value |
| 1 | NICAM/FM2_Coeff. (5) | 8 | see Table 6–14 |
| 2 | NICAM/FM2_Coeff. (4) | 8 | |
| 3 | NICAM/FM2_Coeff. (3) | 8 | |
| 4 | NICAM/FM2_Coeff. (2) | 8 | |
| 5 | NICAM/FM2_Coeff. (1) | 8 | |
| 6 | NICAM/FM2_Coeff. (0) | 8 | |
| FIR2 00 05 _{hex} (MSP-Ch2: FM1/AM) | | | |
| No. | Symbol Name | Bits | Value |
| 1 | IMREG1 | 8 | 04 _{hex} |
| 2 | IMREG1/IMREG2 | 8 | 40 _{hex} |
| 3 | IMREG2 | 8 | 00 _{hex} |
| 4 | FM/AM_Coef (5) | 8 | see Table 6–14 |
| 5 | FM/AM_Coef (4) | 8 | |
| 6 | FM/AM_Coef (3) | 8 | |
| 7 | FM/AM_Coef (2) | 8 | |
| 8 | FM/AM_Coef (1) | 8 | |
| 9 | FM/AM_Coef (0) | 8 | |

6.3.6. FIR-Parameter, Registers FIR1 and FIR2

Note: The use of this register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x2G.

Data-shaping and/or FM/AM bandwidth limitation is performed by a pair of linear phase Finite Impulse Response filters (FIR-filter). The filter coefficients are programmable and are either configured automatically by the STANDARD SELECT register or written manually by the control processor via the control bus. Two not necessarily different sets of coefficients are required: one for MSP-Ch1 (NICAM or FM2) and one for MSP-Ch2 (FM1 = FM-mono). In Table 6–14 several coefficient sets are proposed.

To load the FIR-filters, the following data values are to be transferred **8 bits at a time embedded LSB-bound in a 16-bit word**.

The loading sequences must be obeyed. To change a coefficient set, the complete block FIR1 or FIR2 must be transmitted.

Note: For compatibility with MSP 3410B, IMREG1 and IMREG2 have to be transmitted. The value for IMREG1 and IMREG2 is 004. Due to the partitioning to 8-bit units, the values 04_{hex}, 40_{hex}, and 00_{hex} arise.

6.3.7. DCO-Registers

Note: The use of this register is no longer recommended. It should be used only in cases where software-compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the MODUS register provides a more economic way to program the MSP 34x2G.

When selecting a TV-sound standard by means of the STANDARD SELECT register, all frequency tuning is performed automatically.

If manual setting of the tuning frequency is required, a set of 24-bit registers determining the mixing frequencies of the quadrature mixers can be written manually into the IC. In Table 6–15, some examples of DCO registers are listed. It is necessary to divide them up into low part and high part. The formula for the calculation of the registers for any chosen IF frequency is as follows:

$$\text{INCR}_{\text{dec}} = \text{int}(f/\text{fs} \cdot 2^{24})$$

with: int = integer function
 f = IF frequency in MHz
 f_s = sampling frequency (18.432 MHz)

Conversion of INCR into hex-format and separation of the 12-bit low and high parts lead to the required register values (DCO1_HI or _LO for MSP-Ch1, DCO2_HI or LO for MSP-Ch2).

Table 6–14: 8-bit FIR-coefficients (decimal integer); reset status: all coefficients are “0”

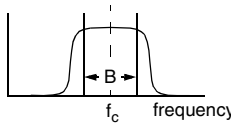
| Coefficients for FIR1 00 01 _{hex} and FIR2 00 05 _{hex} | | | | | | | | | | | | | | |
|---|--------------------------|------|------------|------|------------|------|-----------------------|---|---------|---------|---------|---------|---------|-------------|
| | Terrestrial TV Standards | | | | | | | <div>FM - Satellite</div> <div>FIR filter corresponds to a band-pass with a band-width of B = 130 to 500 kHz</div> <div></div> | | | | | | |
| | B/G-, D/K-NICAM-FM | | I-NICAM-FM | | L-NICAM-AM | | B/G-, D/K-, M-Dual FM | 130 kHz | 180 kHz | 200 kHz | 280 kHz | 380 kHz | 500 kHz | Auto-search |
| Coef(i) | FIR1 | FIR2 | FIR1 | FIR2 | FIR1 | FIR2 | FIR2 | FIR2 | FIR2 | FIR2 | FIR2 | FIR2 | FIR2 | FIR2 |
| 0 | −2 | 3 | 2 | 3 | −2 | −4 | 3 | 73 | 9 | 3 | −8 | −1 | −1 | −1 |
| 1 | −8 | 18 | 4 | 18 | −8 | −12 | 18 | 53 | 18 | 18 | −8 | −9 | −1 | −1 |
| 2 | −10 | 27 | −6 | 27 | −10 | −9 | 27 | 64 | 28 | 27 | 4 | −16 | −8 | −8 |
| 3 | 10 | 48 | −4 | 48 | 10 | 23 | 48 | 119 | 47 | 48 | 36 | 5 | 2 | 2 |
| 4 | 50 | 66 | 40 | 66 | 50 | 79 | 66 | 101 | 55 | 66 | 78 | 65 | 59 | 59 |
| 5 | 86 | 72 | 94 | 72 | 86 | 126 | 72 | 127 | 64 | 72 | 107 | 123 | 126 | 126 |
| Mode-REG[12] | 0 | | 0 | | 0 | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| Mode-REG[13] | 0 | | 0 | | 0 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| For compatibility, except for the FIR2-AM and the Autosearch-sets, the FIR-filter programming as used for the MSP 3410B is also possible. | | | | | | | | | | | | | | |
| ADR coefficients are listed in the DRP data sheet. | | | | | | | | | | | | | | |

Table 6–15: DCO registers for the MSP 34x2G; reset status: DCO_HI/LO = “0000”

| DCO1_LO 00 93 _{hex} , DCO1_HI 00 9B _{hex} ; DCO2_LO 00 A3 _{hex} , DCO2_HI 00 AB _{hex} | | | | | |
|---|------------|------------|-----------|------------|------------|
| Freq. MHz | DCO_HI/hex | DCO_LO/hex | Freq. MHz | DCO_HI/hex | DCO_LO/hex |
| 4.5 | 03E8 | 000 | | | |
| 5.04 | 0460 | 0000 | 5.76 | 0500 | 0000 |
| 5.5 | 04C6 | 038E | 5.85 | 0514 | 0000 |
| 5.58 | 04D8 | 0000 | 5.94 | 0528 | 0000 |
| 5.7421875 | 04FC | 00AA | | | |
| 6.0 | 0535 | 0555 | 6.6 | 05BA | 0AAA |
| 6.2 | 0561 | 0C71 | 6.65 | 05C5 | 0C71 |
| 6.5 | 05A4 | 071C | 6.8 | 05E7 | 01C7 |
| 6.552 | 05B0 | 0000 | | | |
| 7.02 | 0618 | 0000 | 7.2 | 0640 | 0000 |
| 7.38 | 0668 | 0000 | 7.56 | 0690 | 0000 |

6.4. Manual/Compatibility Mode: Description of Demodulator Read Registers

Note: The use of these register is no longer recommended. It should be used only in cases where software compatibility to the MSP 34x0D is required. Using the STANDARD SELECTION register together with the STATUS register provides a more economic way to program the MSP 34x2G and to retrieve information from the IC.

All registers except C_AD_BITS are 8 bits wide. They can be read out of the RAM of the MSP 34x2G if the MSP 34x0D Manual/Compatibility Mode is required.

All transmissions take place in 16-bit words. The valid 8-bit data are the 8 LSBs of the received data word.

If the Automatic Sound Select feature is not used, the NICAM or FM-identification parameters must be read and evaluated by the controller in order to enable appropriate switching of the channel select matrix of the baseband processing part. The FM-identification registers are described in section 6.6.1. To handle the NICAM-sound and to observe the NICAM-quality, at least the registers C_AD_BITS and ERROR_RATE must be read and evaluated by the controller. Additional data bits and CIB bits, if supplied by the NICAM transmitter, can be obtained by reading the registers ADD_BITS and CIB_BITS.

6.4.1. NICAM Mode Control/Additional Data Bits Register

NICAM operation mode control bits and A[2:0] of the additional data bits.

Format:

| MSB | | C_AD_BITS 00 23 _{hex} | | | | | | LSB | |
|---------|-----|--------------------------------|------|------|----|----|----|-----|---|
| 11 | ... | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Auto_FM | ... | A[2] | A[1] | A[0] | C4 | C3 | C2 | C1 | S |

Important: “S” = Bit[0] indicates correct NICAM-synchronization (S = 1). If S = 0, the MSP 3411/3451G has not yet synchronized correctly to frame and sequence, or has lost synchronization. The remaining read registers are therefore not valid. The MSP mutes the NICAM output automatically and tries to synchronize again as long as MODE_REG[6] is set.

The operation mode is coded by C4-C1 as shown in Table 6–16.

Table 6–16: NICAM operation modes as defined by the EBU NICAM 728 specification

| C4 | C3 | C2 | C1 | Operation Mode |
|---|----|----|----|--|
| 0 | 0 | 0 | 0 | Stereo sound (NICAMA/B), independent mono sound (FM1) |
| 0 | 0 | 0 | 1 | Two independent mono signals (NICAMA, FM1) |
| 0 | 0 | 1 | 0 | Three independent mono channels (NICAMA, NICAMB, FM1) |
| 0 | 0 | 1 | 1 | Data transmission only; no audio |
| 1 | 0 | 0 | 0 | Stereo sound (NICAMA/B), FM1 carries same channel |
| 1 | 0 | 0 | 1 | One mono signal (NICAMA). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 0 | Two independent mono channels (NICAMA, NICAMB). FM1 carries same channel as NICAMA |
| 1 | 0 | 1 | 1 | Data transmission only; no audio |
| x | 1 | x | x | Unimplemented sound coding option (not yet defined by EBU NICAM 728 specification) |
| AUTO_FM: monitor bit for the AUTO_FM Status: 0: NICAM source is NICAM 1: NICAM source is FM | | | | |

Note: It is no longer necessary to read out and evaluate the C_AD_BITS. All evaluation is performed in the MSP and indicated in the STATUS register.

6.4.2. Additional Data Bits Register

Contains the remaining 8 of the 11 additional data bits. The additional data bits are not yet defined by the NICAM 728 system.

Format:

| MSB | | ADD_BITS 00 38 _{hex} | | | | | | LSB | |
|-------|------|-------------------------------|------|------|------|------|------|-----|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| A[10] | A[9] | A[8] | A[7] | A[6] | A[5] | A[4] | A[3] | | |

6.4.3. CIB Bits Register

CIB bits 1 and 2 (see NICAM 728 specifications).

Format:

| MSB | | CIB_BITS 00 3E _{hex} | | | | | | LSB | |
|-----|---|-------------------------------|---|---|---|------|------|-----|--|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| x | x | x | x | x | x | CIB1 | CIB2 | | |

6.4.4. NICAM Error Rate Register

| ERROR_RATE | 00 57 _{hex} |
|--------------------|----------------------|
| Error free | 0000 _{hex} |
| maximum error rate | 07FF _{hex} |

Average error rate of the NICAM reception in a time interval of 182 ms, which should be close to 0. The initial and maximum value of ERROR_RATE is 2047. This value is also active if the NICAM bit of MODE_REG is not set. Since the value is achieved by filtering, a certain transition time (approx. 0.5 sec) is unavoidable. Acceptable audio may have error rates up to a value of 700 int. Individual evaluation of this value by the controller and an appropriate threshold may define the fallback mode from NICAM to FM/AM-Mono in case of poor NICAM reception.

The bit error rate per second (BER) can be calculated by means of the following formula:

$$\text{BER} = \text{ERROR_RATE} * 12.3 * 10^{-6} / \text{s}$$

6.4.5. PLL_CAPS Readback Register

It is possible to read out the actual setting of the PLL_CAPS. In standard applications, this register is not of interest for the customer.

| PLL_CAPS | 02 1F _{hex} L |
|-------------------|--------------------------------------|
| minimum frequency | 1111 1111 FF _{hex} |
| nominal frequency | 0101 0110 56 _{hex} RESET |
| maximum frequency | 0000 0000 00 _{hex} |
| PLL_CAPS | 02 1F _{hex} H |
| PLL open | xxxx xxx0 |
| PLL closed | xxxx xxx1 |

6.4.6. AGC_GAIN Readback Register

It is possible to read out the actual setting of AGC_GAIN in Automatic Gain Mode. In standard applications, this register is not of interest for the customer.

| AGC_GAIN | 02 1E _{hex} |
|-------------------------------|-----------------------------|
| max. amplification (20 dB) | 0001 0100 14 _{hex} |
| min. amplification (3 dB) | 0000 0000 00 _{hex} |

6.4.7. Automatic Search Function for FM-Carrier Detection in Satellite Mode

The AM demodulation ability of the MSP 34x2G offers the possibility to calculate the “field strength” of the momentarily selected FM carrier, which can be read out by the controller. In SAT receivers, this feature can be used to make automatic FM carrier search possible.

For this, the MSP has to be switched to AM-mode (MODE_REG[8]), FM-Prescale must be set to 7F_{hex} = +127_{dec}, and the FM DC notch (see section 6.5.7.) must be switched off. The sound-IF frequency range must now be “scanned” in the MSP-channel 2 by means of the programmable quadrature mixer with an appropriate incremental frequency (i.e. 10 kHz). After each incrementation, a field strength value is available at the quasi-peak detector output (quasi-peak detector source must be set to FM), which must be examined for relative maxima by the controller. This results in either continuing search or switching the MSP back to FM demodulation mode.

During the search process, the FIR2 must be loaded with the coefficient set “AUTOSEARCH”, which enables small bandwidth, resulting in appropriate field strength characteristics. The absolute field strength value (can be read out of “quasi-peak detector output FM1”) also gives information on whether a main FM carrier or a subcarrier was detected; and as a practical consequence, the FM bandwidth (FIR1/2) and the deemphasis (50 μs or adaptive) can be switched accordingly.

Due to the fact that a constant demodulation frequency offset of a few kHz leads to a DC level in the demodulated signal, further fine tuning of the found carrier can be achieved by evaluating the “DC Level Readout FM1”. Therefore, the FM DC Notch must be switched on, and the demodulator part must be switched back to FM-demodulation mode.

6.5. Manual/Compatibility Mode: Description of DSP Write Registers

6.5.1. Additional Channel Matrix Modes

| | | |
|----------------------------|----------------------|-------------------|
| Loudspeaker Matrix | 00 08 _{hex} | L |
| Headphone Matrix | 00 09 _{hex} | L |
| SCART1 Matrix | 00 0A _{hex} | L |
| SCART2 Matrix | 00 41 _{hex} | L |
| I ² S Matrix | 00 0B _{hex} | L |
| Quasi-Peak Detector Matrix | 00 0C _{hex} | L |
| SUM/DIFF | 0100 0000 | 40 _{hex} |
| AB_XCHANGE | 0101 0000 | 50 _{hex} |
| PHASE_CHANGE_B | 0110 0000 | 60 _{hex} |
| PHASE_CHANGE_A | 0111 0000 | 70 _{hex} |
| A_ONLY | 1000 0000 | 80 _{hex} |
| B_ONLY | 1001 0000 | 90 _{hex} |

This table shows additional modes for the channel matrix registers.

The sum/difference mode can be used together with the quasi-peak detector to determine the sound material mode. If the difference signal on channel B (right) is near to zero, and the sum signal on channel A (left) is high, the incoming audio signal is mono. If there is a significant level on the difference signal, the incoming audio is stereo.

6.5.2. Volume Modes of SCART1/2 Outputs

| | | |
|--------------------|----------------------|------------------|
| Volume Mode SCART1 | 00 07 _{hex} | [3:0] |
| Volume Mode SCART2 | 00 40 _{hex} | [3:0] |
| linear | 0000 RESET | 0 _{hex} |
| logarithmic | 0001 | 1 _{hex} |

| Linear Mode | | |
|--|----------------------|-------------------|
| Volume SCART1 | 00 07 _{hex} | H |
| Volume SCART2 | 00 40 _{hex} | H |
| OFF | 0000 0000 RESET | 00 _{hex} |
| 0 dB gain (digital full scale (FS) to 2 V _{RMS} output) | 0100 0000 | 40 _{hex} |
| +6 dB gain (–6 dBFS to 2 V _{RMS} output) | 0111 1111 | 7F _{hex} |

Note: SCART Volume linear mode will not be supported in the future (documented for compatibility reasons only).

6.5.3. FM Fixed Deemphasis

| | | |
|---------------|----------------------|-------------------|
| FM Deemphasis | 00 0F _{hex} | H |
| 50 μ s | 0000 0000 RESET | 00 _{hex} |
| 75 μ s | 0000 0001 | 01 _{hex} |
| J17 | 0000 0100 | 04 _{hex} |
| OFF | 0011 1111 | 3F _{hex} |

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Auto-matic Sound Select (MODUS[0]=1) is on.

6.5.4. FM Adaptive Deemphasis

| | | |
|----------------------------|----------------------|-------------------|
| FM Adaptive Deemphasis WP1 | 00 0F _{hex} | L |
| OFF | 0000 0000 RESET | 00 _{hex} |
| WP1 | 0011 1111 | 3F _{hex} |

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Auto-matic Sound Select (MODUS[0]=1) is on.

6.5.5. NICAM Deemphasis

A J17 Deemphasis is always applied to the NICAM signal. It is not switchable.

6.5.6. Identification Mode for A2 Stereo Systems

| Identification Mode | 00 15 _{hex} | L |
|---------------------------------|----------------------|-------------------|
| Standard B/G (German Stereo) | 0000 0000 RESET | 00 _{hex} |
| Standard M (Korean Stereo) | 0000 0001 | 01 _{hex} |
| Reset of Ident-Filter | 0011 1111 | 3F _{hex} |

To shorten the response time of the identification algorithm after a program change between two FM-Stereo capable programs, the reset of the ident-filter can be applied.

Sequence:

1. Program change
2. Reset ident-filter
3. Set identification mode back to standard B/G or M
4. Wait approx. 500 ms
5. Read stereo detection register

Note: This register is initialized during STANDARD SELECTION and is automatically updated when Auto-matic Sound Select (MODUS[0]=1) is on.

6.5.7. FM DC Notch

The DC compensation filter (FM DC Notch) for FM input can be switched off. This is used to speed up the automatic search function (see Section 6.4.7.). In normal FM-mode, the FM DC Notch should be switched on.

| FM DC Notch | 00 17 _{hex} | L |
|-------------|----------------------|-------------------|
| ON | 0000 0000 Reset | 00 _{hex} |
| OFF | 0011 1111 | 3F _{hex} |

6.6. Manual/Compatibility Mode: Description of DSP Read Registers

All readable registers are 16-bit wide. Transmissions via I²C bus have to take place in 16-bit words. Some of the defined 16-bit words are divided into low and high byte, thus holding two different control entities.

These registers are not writable.

6.6.1. Stereo Detection Register for A2 Stereo Systems

| Stereo Detection Register | 00 18 _{hex} | H |
|---------------------------|---|---|
| Stereo Mode | Reading (two's complement) | |
| MONO | near zero | |
| STEREO | positive value (ideal reception: 7F _{hex}) | |
| BILINGUAL | negative value (ideal reception: 80 _{hex}) | |

Note: It is no longer necessary to read out and evaluate the A2 identification level. All evaluation is performed in the MSP and indicated in the STATUS register.

6.6.2. DC Level Register

| DC Level Readout FM1 (MSP-Ch2) | 00 1B _{hex} | H+L |
|-----------------------------------|---|-----|
| DC Level Readout FM2 (MSP-Ch1) | 00 1C _{hex} | H+L |
| DC Level | [8000 _{hex} ... 7FFF _{hex}] values are 16 bit two's complement | |

The DC level register measures the DC component of the incoming FM signals (FM1 and FM2). This can be used for seek functions in satellite receivers and for IF FM frequencies fine tuning. A too low demodulation frequency (DCO) results in a positive DC-level and vice versa. For further processing, the DC content of the demodulated FM signals is suppressed. The time constant τ , defining the transition time of the DC Level Register, is approximately 28 ms.

6.7. Demodulator Source Channels in Manual Mode

6.7.1. Terrestrial Sound Standards

Table 6–17 shows the source channel assignment of the demodulated signals in case of manual mode for all terrestrial sound standards. See Table 2–2 for the assignment in the Automatic Sound Select mode. In manual mode for terrestrial sound standards, only two demodulator sources are defined.

6.7.2. SAT Sound Standards

Table 6–18 shows the source channel assignment of the demodulated signals for SAT sound standards.

6.8. Exclusions of Audio Baseband Features

In general, all functions can be switched independently. Two exceptions exist:

1. NICAM cannot be processed simultaneously with the FM2 channel.
2. FM adaptive deemphasis cannot be processed simultaneously with FM-identification.

6.9. Compatibility Restrictions to MSP 34x0D

The MSP 34x2G is fully hardware compatible to the MSP 34x0D. However, to substitute a MSP 34x0D by the corresponding MSP 34x2G, the controller software has to be adapted slightly:

1. The register FM-Matrix (00 0E_{hex} low part) must be changed from “no matrix (00_{hex})” to “sound A mono (03_{hex})” during mono transmission of all TV-sound standards (see also Table 6–17).
2. With the MSP 34x2G, the STANDARD SELECTION initializes the FM-deemphasis, which is not the case for the MSP 34x0D. So, if STANDARD SELECTION is applied, this I²C instruction can be omitted.

Table 6–17: Manual Sound Select Mode for Terrestrial Sound Standards

| | | | | Source Channels of Sound Select Block | |
|---|--------------------------------|--|--------------------------------|---------------------------------------|---|
| Broadcasted Sound Standard | Selected MSP Standard Code | Broadcasted Sound Mode | FM Matrix | FM/AM (use 0 for channel select) | Stereo or A/B (use 1 for channel select) |
| B/G-FM D/K-FM M-Korea M-Japan | 03 04, 05 02 30 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | German Stereo Korean Stereo | Stereo | Stereo |
| | | BILINGUAL, Languages A and B | No Matrix | Left = A Right = B | Left = A Right = B |
| B/G-NICAM L-NICAM I-NICAM D/K-NICAM D/K-NICAM (with high deviation FM) | 08 09 0A 0B 0C, 0D | NICAM not available or NICAM error rate too high | Sound A Mono ¹⁾ | analog Mono | no sound with AUTO_FM: analog Mono |
| | | MONO | Sound A Mono ¹⁾ | analog Mono | NICAM Mono |
| | | STEREO | Sound A Mono ¹⁾ | analog Mono | NICAM Stereo |
| | | BILINGUAL, Languages A and B | Sound A Mono ¹⁾ | analog Mono | Left = NICAM A Right = NICAM B |
| BTSC | 20 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |
| | | MONO + SAP | Sound A Mono | Mono | Mono |
| | | STEREO + SAP | Korean Stereo | Stereo | Stereo |
| | 21 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | | | |
| | | MONO + SAP | No Matrix | Left = Mono Right = SAP | Left = Mono Right = SAP |
| | | STEREO + SAP | | | |
| FM-Radio | 40 | MONO | Sound A Mono | Mono | Mono |
| | | STEREO | Korean Stereo | Stereo | Stereo |

¹⁾ Automatic refresh to Sound A Mono, do not write any other value to the register FM Matrix!

Table 6–18: Manual Sound Select Modes for SAT-Standards

| | | | | Source Channels of Sound Select Block for SAT-Modes | | | |
|----------------------------|----------------------------|------------------------|--------------|---|-------------------------------------|-----------------------------------|-----------------------------------|
| Broadcasted Sound Standard | Selected MSP Standard Code | Broadcasted Sound Mode | FM Matrix | FM/AM (source select: 0) | Stereo or A/B (source select: 1) | Stereo or A (source select: 3) | Stereo or B (source select: 4) |
| FM SAT | 6, 50 _{hex} | MONO | Sound A Mono | Mono | Mono | Mono | Mono |
| | 51 _{hex} | STEREO | No Matrix | Stereo | Stereo | Stereo | Stereo |
| | | BILINGUAL | No Matrix | Left = A (FM1) Right = B (FM2) | Left = A (FM1) Right = B (FM2) | A (FM1) | B (FM2) |

7. Appendix C: Application Information

7.1. Phase Relationship of Analog Outputs

The analog output signals: Loudspeaker, headphone, and SCART2 all have the same phases. The user does not need to correct output phases when using these analog outputs directly. The SCART1 output has opposite phase.

Using the I²S-outputs for other DSPs or D/A converters, care must be taken to adjust for the correct phase. If the attached coprocessor is one of the MSP family, the following schematics help to determine the phase relationship.

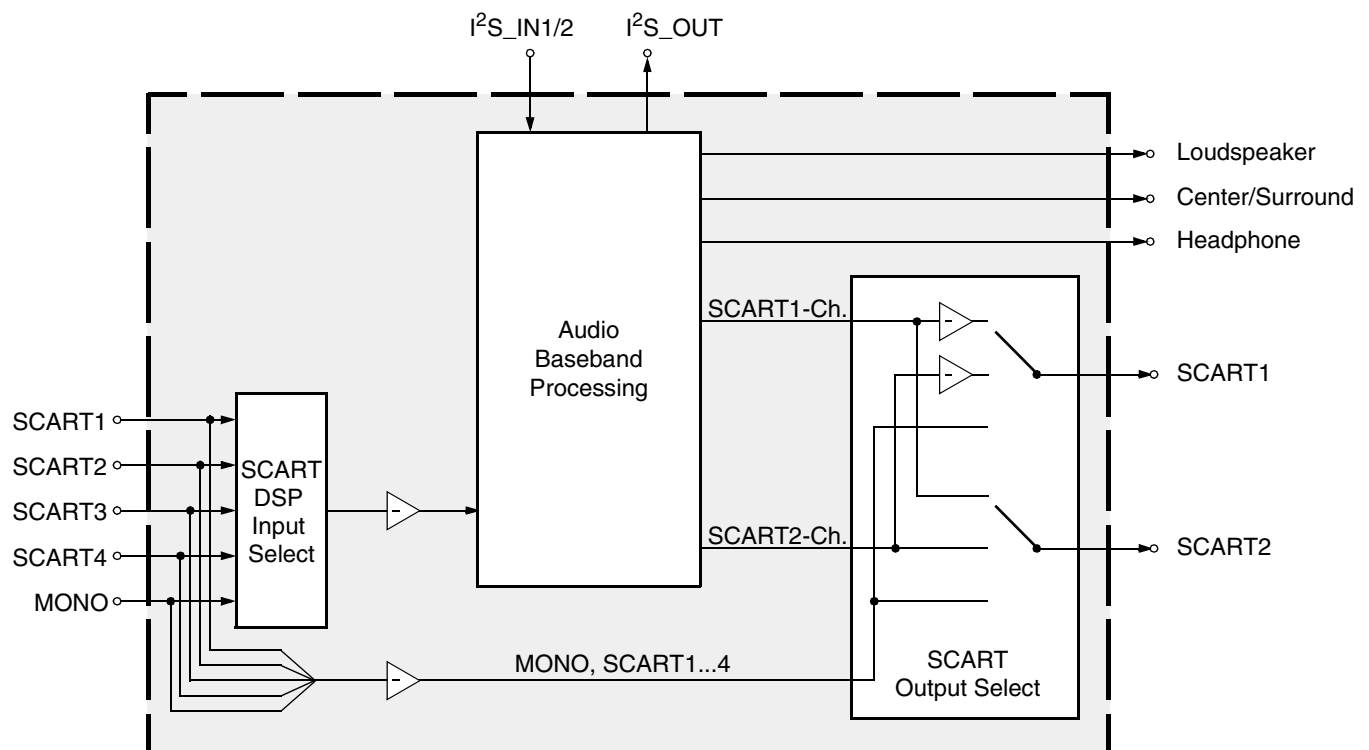


Fig. 7-1: Phase diagram of the MSP 34x2G

8. Appendix D: MSP 34x2G Version History

MSP 3452G-A1

First release

MSP 34x2G-A2

- J17 FM-deemphasis implemented
- MDB implemented
- acoustical compensation filter implemented
- several feedback paths to source selector added
- equalizer for center channel added
- Main path: switching facilities built in
- input specification for RESETQ and TESTEN changed

MSP 34x2G-B3

- FM-Radio available in non-BTSC versions with activation key MSP 3402G/3412G
- implementation of SRS WOW
- The Automatic Sound Select (ASS) malfunction has been corrected. In the previous version, under certain circumstances and depending on the baseband features used, e.g.: Micronas BASS, Virtual Surround Sound, Equalizer... etc., the Automatic Sound Select Feature (ASS) did not work correctly.

9. Data Sheet History

1. Preliminary data sheet: "MSP 34x2G Multistandard Sound Processor Family with Dolby Surround Pro Logic", March 5, 2001, 6251-520-2PD. Second release of the preliminary data sheet.
Major changes:
 - specification for version A2 added (see Appendix E: Version History)
 - description for MDB added
 - I²C-bus description changed
 - ACB register: documentation for bit allocation D_CTR_I/O changed
2. Data Sheet: "MSP 34x2G Multistandard Sound Processor Family with Dolby Pro Logic", June 3, 2003, 6251-520-1DS. First release of the data sheet.
Major changes:
 - specification for version B3 added
 - implementation of SRS WOW
 - Section 4.1.: diagrams for all packages changed
 - PLQFP64 changed to PMQFP64-2
 - Micronas Dynamic Bass (MDB) changed to Micronas BASS (MB)

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Printed in Germany
 Order No. 6251-520-1DS

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