OKI semiconductor

MSM82C84A-2RS/GS/JS

CLOCK GENERATOR AND DRIVER

GENERAL DESCRIPTION

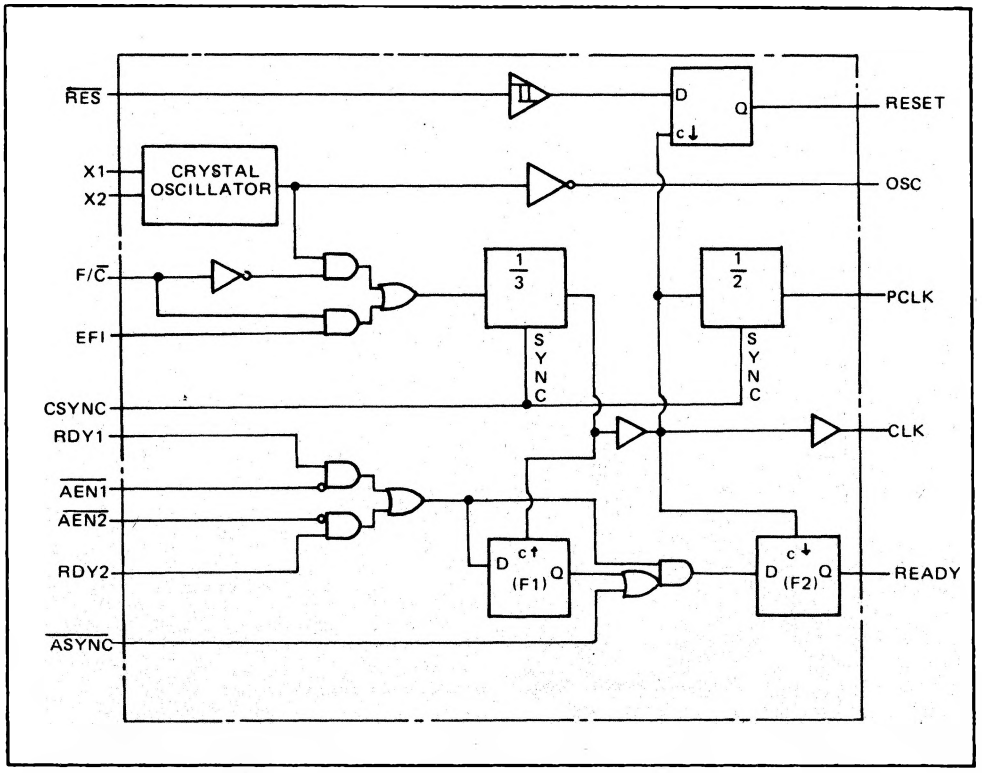
The MSM82C84A-2RS/GS is a clock generator designed to generate MSM80C86 and MSM80C88 system clocks.

Due to the use of silicon gate CMOS technology, standby current is only 40 μA (MAX.), and the power consumption is very low with 16 mA (MAX.) when a 8 MHz clock is generated.

FEATURES

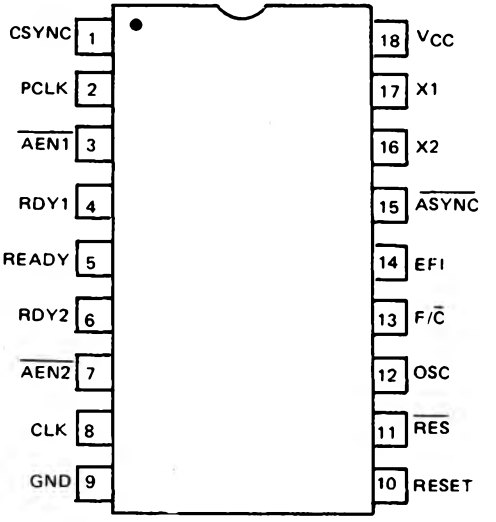
- Operating frequency of 6 to 24 MHz (CLK output 2 to 8 MHz)
- 3μ silicon gate CMOS technology for low power consumption
- Built-in crystal oscillator circuit
- 3V ~ 6V single power supply
- Built-in synchronized circuit for MSM80C86 and MSM80C88 READY and RESET
- TTL compatible
- Built-in Schmitt trigger circuit ($\overline{RES}$ input)
- 18-pin DIP (MSM82C84A-2RS)
- 24-pin flat package (MSM82C84A-2GS)
- 20-pin PLCC (MSM82C84A-2JS)

FUNCTIONAL BLOCK DIAGRAM

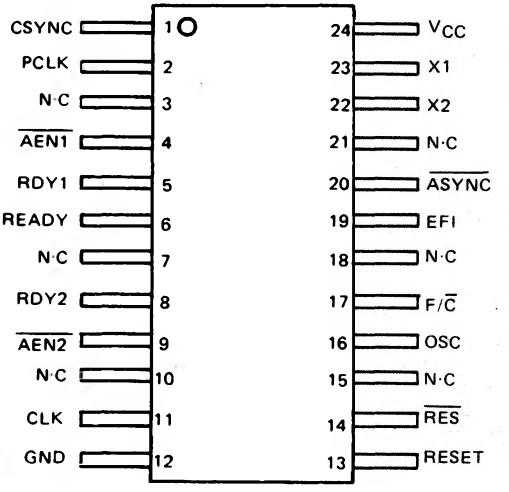


PIN CONFIGURATION

18 Lead Plastic DIP

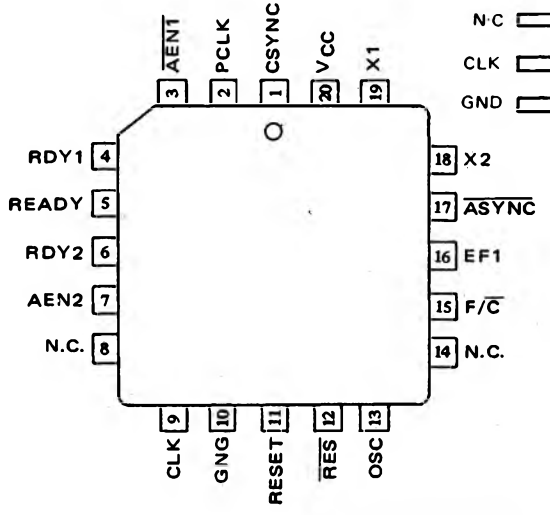


24 Lead Plastic Flat Package



(N·C not connected)

20 Lead PLCC



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits		Unit	Conditions
		MSM82C84A-2RS/JS	MSM82C84A-2GS		
Supply Voltage	V_{CC}	−0.5 ~ +7		V	Respect to GND
Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5		V	
Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5		V	
Storage Temperature	Tstg	−55 ~ +150		°C	−
Power Dissipation	P_D	0.8	0.7	W	Ta = 25°C

OPERATING RANGES

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 ~ 6	V
Operating Temperature	T_{OP}	−40 ~ +85	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Level Input Voltage	V_{IL}	−0.5		+0.8	V
"H" Level Input Voltage (except $\overline{RES}$)	V_{IH}	2.2		V_{CC} +0.5	V
"H" Level Input Voltage ($\overline{RES}$)		0.6*V_{CC}			

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

Parameter	Symbol	MIN	MAX	Unit	Conditions
"L" Level Output Voltage (CLK)	V_{OL}	−	0.4	V	I_{OL} = 4 mA
"L" Level Output Voltage (OTHERS)	V_{OL}	−	0.4	V	I_{OL} = 2.5mA
"H" Level Output Voltage (CLK)	V_{OH}	V_{CC} − 0.4	−	V	I_{OH} = −4mA
"H" Level Output Voltage (OTHERS)	V_{OH}	V_{CC} − 0.4		V	I_{OH} = −1mA
$\overline{RES}$ Input Hysteresis	$V_{IHR} - V_{ILR}$	0.2 * V_{CC}		V	
Input Leak Current (EXCEPT $\overline{ASYNC}$)	I_{LI}	−1	+1	μA	$0 \leq V_{in} \leq V_{CC}$
Input Current ($\overline{ASYNC}$)	I_{LIA}	−100	+10	μA	$0 \leq V_{in} \leq V_{CC}$
Standby Supply Current	I_{CCS}		40	μA	NOTE 1
Operating Supply Current	I_{CC}		16	mA	f = 24MHz, C_L = O_{pF}
Input Capacitance	C_{in}		7	pF	f = 1 MHz

NOTE 1: X1 $\geq$ V_{CC} − 0.2V, X2 $\leq$ 0,2V
F/C $\geq$ V_{CC} − 0.2V, $\overline{ASYNC}$ = V_{CC} or open
VIH $\geq$ V_{CC} − 0.2V, VIL $\leq$ 0,2V

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = −40 ~ 85°C)

(1)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
EFI "H" Pulse Width	t_{EHEL}	13		ns	90%–90%	Output load capacitance CLK output C_L = 100pF Others 30pF
EFI "L" Pulse Width	t_{ELEH}	17		ns	10%–10%	
EFI Cycle Time	t_{ELEL}	36		ns		
Crystal Oscillator Frequency		6	24	MHz		
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Active)	t_{R1VCL}	35		ns	$\overline{ASYNC}$ = High	
Set Up Time of RDY1 or RDY2 to CLK Rising Edge (Active)	t_{R1VCH}	35		ns	$\overline{ASYNC}$ = Low	
Set Up Time of RDY1 or RDY2 to CLK Falling Edge (Inactive)	t_{R1VCL}	35		ns		
Hold Time of RDY1 or RDY2 to CLK Falling Edge	t_{CLR1X}	0		ns		
Set Up Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{AYVCL}	50		ns		
Hold Time of $\overline{ASYNC}$ to CLK Falling Edge	t_{CLAYX}	0		ns		
Set Up Time of $\overline{AEN1}$ ($\overline{AEN2}$) to RDY1 (RDY2) Rising Edge	t_{A1R1V}	15		ns		
Hold Time of $\overline{AEN1}$ ($\overline{AEN2}$) to CLK Falling Edge	t_{CLA1X}	0		ns		
Set Up Time of CSYNC to EFI Rising Edge	t_{YHEH}	20		ns		
Hold Time of CSYNC to EFI Rising Edge	t_{EHYL}	10		ns		
CSYNC Pulse Width	t_{YHYL}	2 x t_{ELEL}		ns		
Set Up Time of $\overline{RES}$ to CLK Falling Edge	t_{I1HCL}	65		ns		
Hold Time of $\overline{RES}$ to CLK Falling Edge	t_{CLI1H}	20		ns		
Input Rising Edge Time	t_{ILIH}		15	ns		
Input Falling Edge Time	t_{IHIL}		15	ns		

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = −40 ~ 85°C)

(2)

Parameter	Symbol	MIN	MAX	Unit	Conditions	
CLK Cycle Time	t_{CLCL}	125		ns		Output load capacitance CLK output C_L = 100pF Others 30pF
CLK "H" Pulse Width	t_{CHCL}	$\frac{1}{3}T_{CLCL}+2$		ns		
CLK "L" Pulse Width	t_{CLCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
CLK Rising and Falling Edge Times	t_{CH1CH2} t_{CL2CL1}		10	ns	1.0V–3.5V	
PCLK "H" Pulse Width	t_{PHPL}	$T_{CLCL}-20$		ns		
PCLK "L" Pulse Width	t_{PLPH}	$T_{CLCL}-20$		ns		
Time from READY Falling Edge to CLK Falling Edge	t_{RYLCL}	−8		ns		
Time from READY Rising Edge to CLK Rising Edge	t_{RYHCH}	$\frac{2}{3}T_{CLCL}-15$		ns		
Delay from CLK Falling Edge to RESET Falling Edge	t_{CLIL}		40	ns		
Delay from CLK Falling Edge to PCLK Rising Edge	t_{CLPH}		22	ns		
Delay from CLK Falling Edge to PCLK Falling Edge	t_{CLPL}		22	ns		
Delay from OSC Falling Edge to CLK Rising Edge	t_{OLCH}	−5	22	ns		
Delay from OSC Falling Edge to CLK Falling Edge	t_{OLCL}	2	35	ns		
Output Rising Edge Time (Except CLK)	t_{OLOH}		15	ns	0.8V~2.2V	
Output Falling Edge Time (Except CLK)	t_{OHOL}		15	ns	2.2V~0.8V	

Note: Parameters where timing has not been indicated in the above table are measured at V_L = 1.5V and V_H = 1.5V for both inputs and outputs.

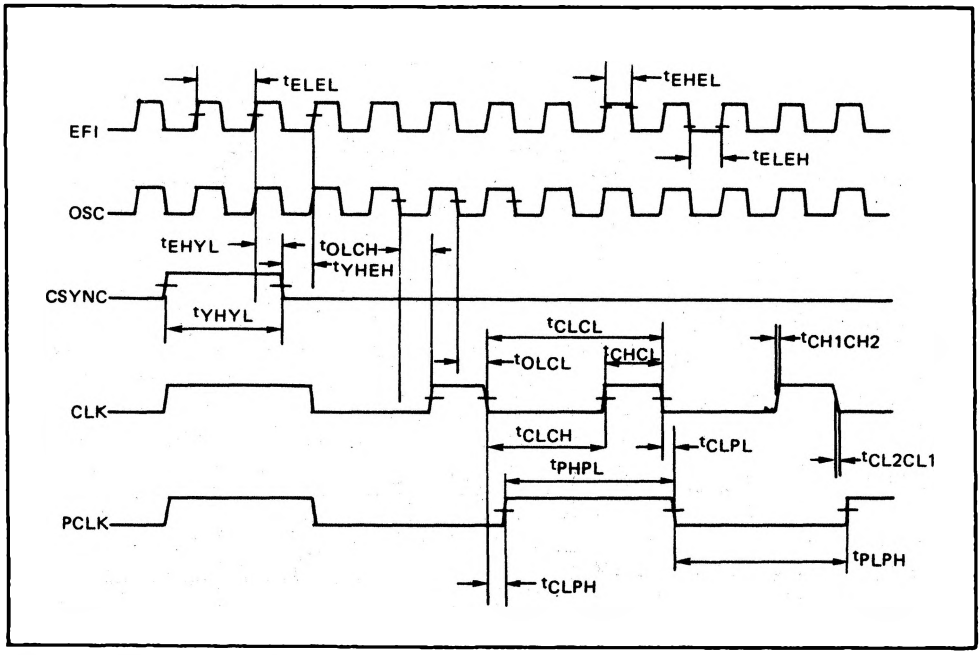
PIN DESCRIPTION

Pin symbol	Name	Input/ output	Function
CSYNC	Clock synchronization singal	Input	Synchronizing signal for output of in-phase CLK signals when more than one MSM82C84A-2 is used. The internal counter is reset when this signal is at high level, and a high level CLK output is generated. The internal counter is subseqently activated and a 33% duty CLK output is generated when this signal is switched to low level. When this signal is used, external synchronization of EFI is necessary. When the internal oscillator is used, it is necessary for this pin to be kept to be low level.
PCLK	Peripheral clock output	Output	This peripheral circuit clock signal is output in a 50% duty cycle at a frequency half that of the clock signal.
$\overline{AEN1}$ $\overline{AEN2}$	Address enable signals	Input	The $\overline{AEN1}$ signal enables $\overline{RDY1}$, and the $\overline{AEN2}$ signal enables RDY2. The respective RDY inputs are activated when the level applied to these pins is low. Although two separate inputs are used in multi-master systems, only the $\overline{AEN}$ which enables the RDY input to be used is to be switched to low level in the case of not using multi-master systems.
RDY1 RDY2	Bus ready signals	Input	Completion of data bus reading and writing by the device connected to the system data bus is indicated when one of these signals is switched to high level. The relevant RDY input is enables only when the corresponding $\overline{AEN}$ is at low level.
READY	Ready output	Output	This signal is obtained by synchronizing the bus ready signal with CLK. This signal is output after guaranteeing the hold time for the CPU in phase with the RDY input.
CLK	Clock output	Output	This signal is the clock used by the CPU and peripheral devices connected to the CPU system data bus. The output waveform is generated in a 33% duty cycle at a frequency 1/3 the oscillating frequency of the crystal oscillator connected to the X1 and X2 pins, or at a frequency 1/3 the EFI input frequency.
$\overline{RES}$	Reset in	Input	This low-level active input is used to generate a CPU reset signal. Since a Schmitt trigger is included in the input circuit for this signal, "power on resetting" can be achieved by connection of a simple RC circuit.
RESET	Reset output	Output	This signal is obtained by CLK synchronization of the input signal applied to $\overline{RES}$ and is output in opposite phase to the $\overline{RES}$ input. This signal is applied to the CPU as the system reset signal.
F/C	Clock select signal	Input	This signal selects the fundamental signal for generation of the CLK signal. The CLK is generated from the crystal oscillator output when this signal is at low level, and from the EFI input signal when at high level.
EFI	External clock signal	Input	The signal applied to this input pin generates the CLK signal when F/$\overline{C}$ is at high level. The frequency of the input signal needs to be three times greater than the desired CLK frequency.
X1, X2	Crystal oscillator connecting pins	Input	Crystal oscillator connections. The crystal oscillator frequency needs to be three times greater than the desired CLK frequency.
OSC	Crystal resonator output	Output	Crystal oscillator output. This output frequency is the same as the oscillating frequency of the oscillator connected to the X1 and X2 pins. As long as a Xtal oscillator is connected to the X1 and X2 pins, this output signal can be obtained independently even if F/C is set to high level to enable the EFI input to be used for CLK generation purposes.

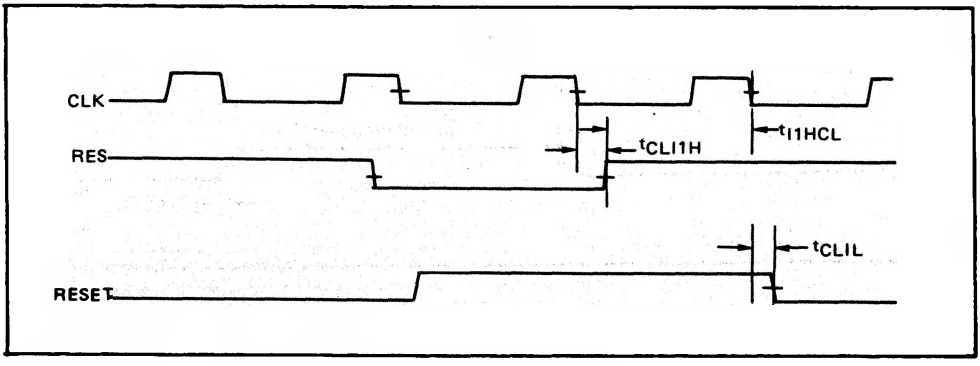
Pin symbol	Name	Input/ output	Function
$\overline{ASYNC}$	Ready synchronization select signal	Input	Signal for selection of the synchronization mode of the READY signal generator circuit. When this signal is at low level, the READY signal is generated by double synchronization. And When at high level, the READY signal is generated by single synchronization. This pin is equipped with internal pull-up resister.
V_{CC}			+5V power supply
GND			GND

TIMING CHART

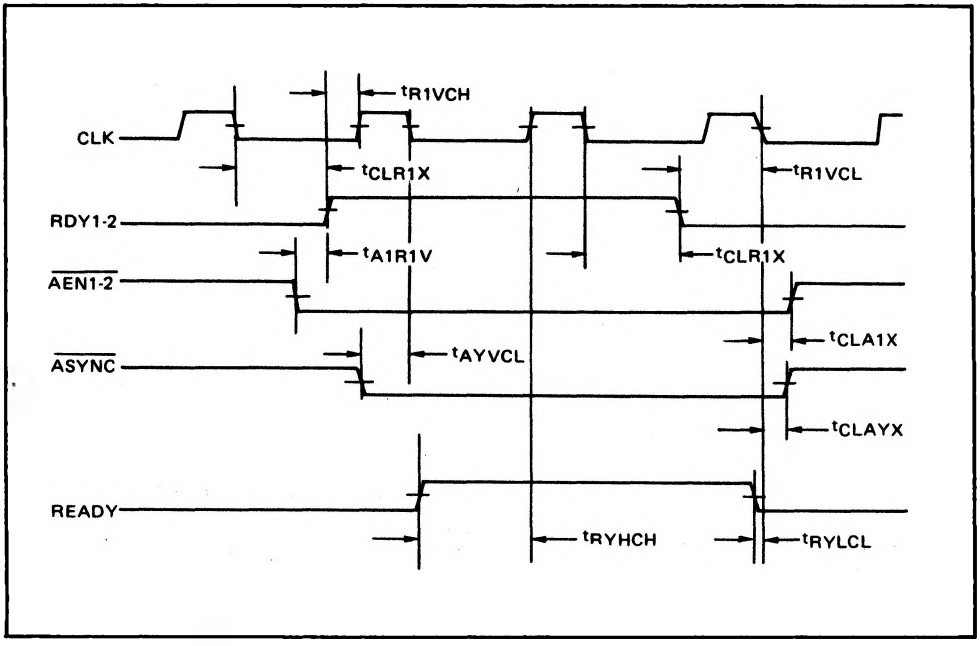
CLK · PCLK · OSC waveforms



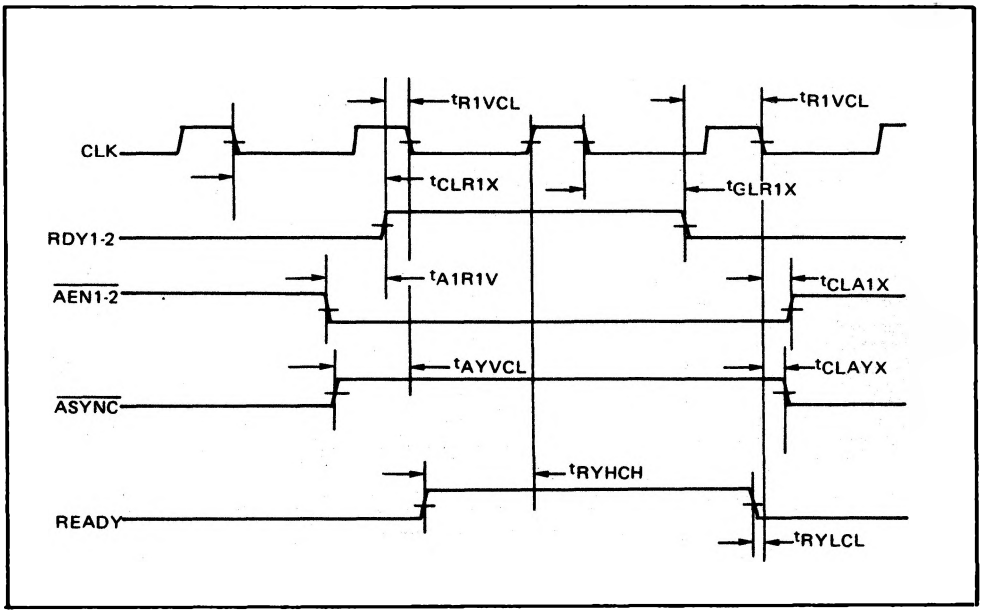
RESET waveform



READY waveform ($\overline{ASYNC}$ = L)



READY waveform ($\overline{ASYNC}$ = H)



DESCRIPTION OF OPERATION

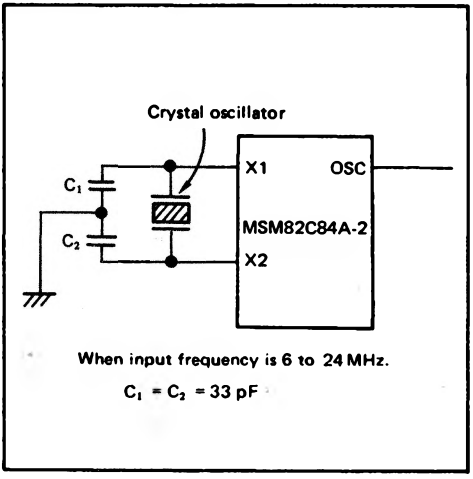
(1) Oscillator Circuit

The MSM82C84A-5 internal oscillator circuit can be driven by connecting a crystal oscillator to the X1 and X2 pins.

The frequency of the crystal oscillator in this case needs to be three times greater than the desired CLK frequency.

Since the oscillator circuit output (the same output as for the crystal resonator frequency) appears at the OSC pin, independent use of this output is also possible.

Recommended Oscillator Circuit



When input frequency is 6 to 24 MHz.

$C_1 = C_2 = 33$ pF

(2) Clock Generator Circuit

This circuit generates two clock outputs—CLK obtained by dividing the input external clock or crystal oscillator circuit output by three, and PCLK obtained by halving CLK. CLK and PCLK are generated from the external clock applied to the EFI pin when F/C is at high level, and are generated from the crystal oscillator circuit when at low level.

(3) Reset Circuit

Since a Schmitt trigger circuit is used in the $\overline{RES}$ input, the MSM82C84A-2 can be reset by "power on" by connection to a simple RC circuit. If the 80C86 or 80C88 is used as the CPU in this case, it is necessary to keep the $\overline{RES}$ input at low level for at least 50 μs after V_{CC} reaches the 4.5V level.

(4) Ready Circuit

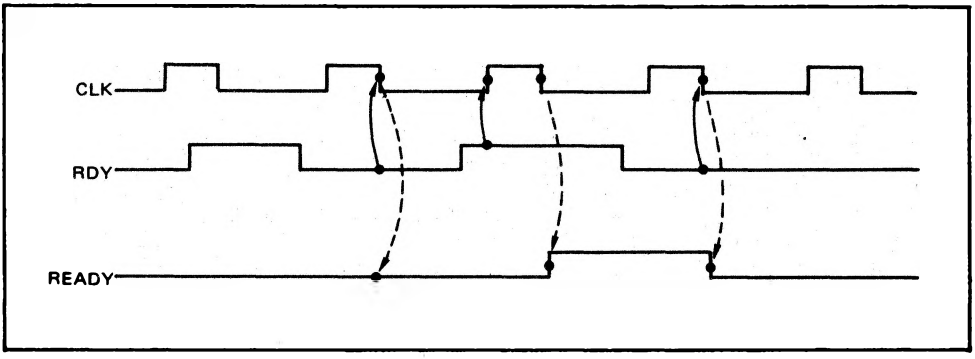
The READY signal generator circuit can be set to synchronization mode by $\overline{ASYNC}$.

(i) When $\overline{ASYNC}$ is at low level

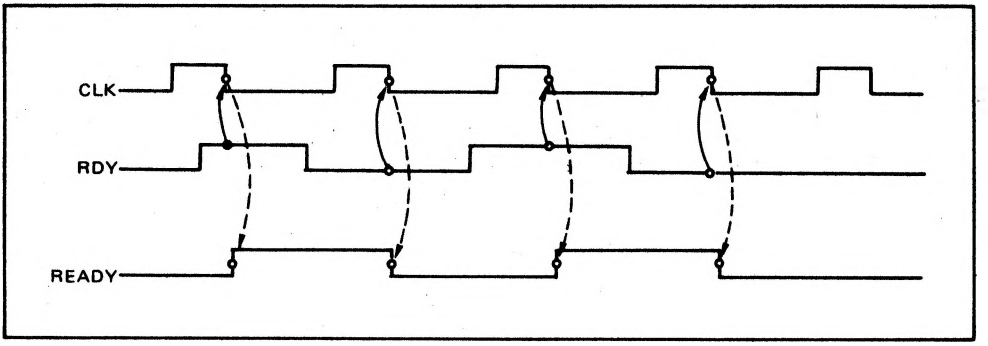
The RDY input is output as the READY signal by double synchronization.

The high-level RDY input is synchronized once by the rising edge of the CLK of the first stage flip-flop (F1 in the circuit diagram), and then synchronized again by the falling edge of the CLK of the next stage flip-flop (F2 in the circuit diagram), resulting in output of a high-level READY output signal (see diagram below).

- The low-level RDY input is synchronized directly by the falling-edge of the CLK of the next stage flip-flop, resulting in output of a low-level READY output signal (see diagram below).



(ii) When $\overline{\text{ASYNC}}$ is at high level
The RDY input is output as the READY signal by single synchronization.
- Both low-level and high-level RDY inputs are synchronized by the falling edge of the CLK of the next stage flip-flop, resulting in output of respective low-level and high-level READY output signals (see diagram below).



EXAMPLE OF USE (CSYNC)

The 82C84A-2 1/3 frequency divider counter is unsettled when the power is switched on. Therefore, the CSYNC pin has been included to synchronize CLK with another signal. When CSYNC is at high level, both CLK and PCLK are high-level outputs. If CSYNC is then switched to low level, CLK is output from the next input clock rising edge, and is divided by 3.

If CSYNC has not been synchronized with the input clock, use the following circuit to achieve the required synchronization