OKI semiconductor

MSM82C53-5RS/GS/JS
MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

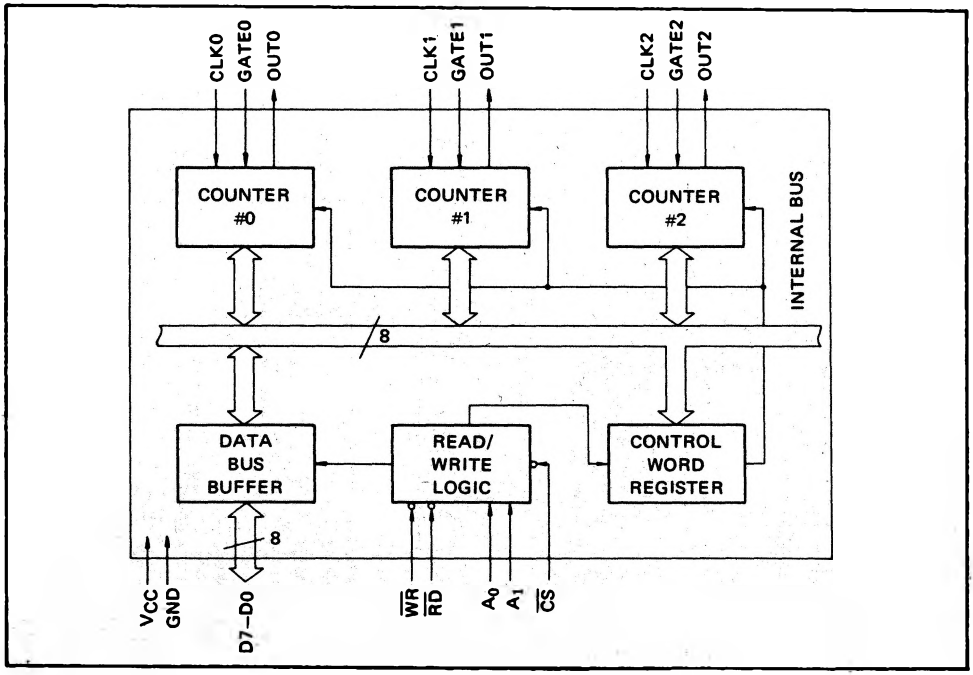
The MSM82C53-5RS/GS/JS and MSM82C53-2RS/GS/JS are programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100 μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 5 mA (max.) at 5 MHz of current required.

The devices consist of three independent counters, and can count up to a maximum of 5 MHz (MSM82C53-5) and 8 MHz (MSM82C53-2). The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

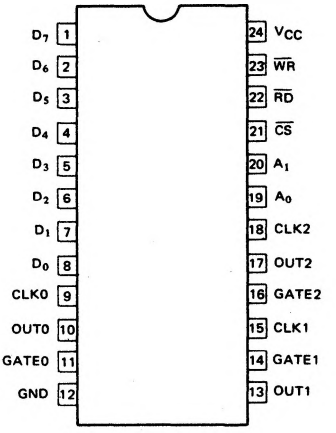
- Maximum operating frequency of 5 MHz (MSM82C53-5)
- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology.
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes available for each counter
- Binary and decimal counting possible
- 24-pin DIP (MSM82C53-5RS/MSM82C53-2RS)
- 32-pin flat package (MSM82C53-5GS/MSM82C53-2GS)
- 28-pin PLCC Package (MSM82C53-5JS/MSM82C53-2JS)

FUNCTIONAL BLOCK DIAGRAM

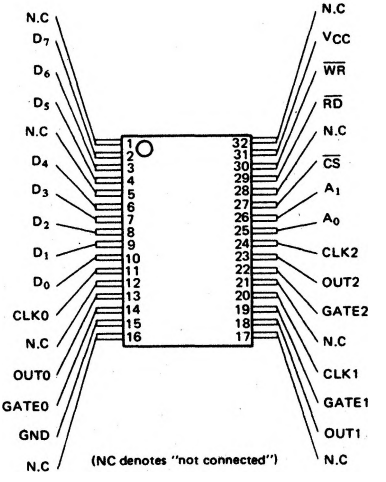


PIN CONFIGURATION

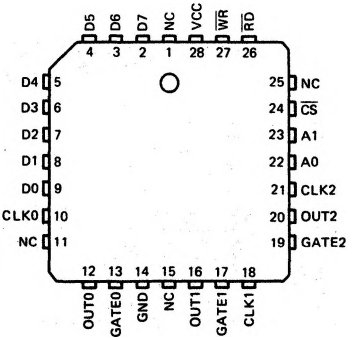
MSM82C53-5RS (Top View)
MSM82C53-2RS
24 LEAD PLASTIC DIP



MSM82C53-5GS (Top View)
MSM82C53-2GS
32 LEAD PLASTIC FLAT PACKAGE



MSM82C53-5JS (Top View)
MSM82C53-2JS
28 Plastic Leaded Chip Carrier



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-5RS MSM82C53-2RS	MSM82C53-5GS MSM82C53-2GS	MSM82C53-5J5 MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA	V_{CC}=4.5V to 5.5V Ta=−40°C to +85°C			0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC}$ −0.2V $V_{IH} \geqq V_{CC}$ − 0.2V $V_{IL} \leqq 0.2V$				100	μA
Operating Supply Current	I_{CC}	t_{CLK} = 200 ns C_L = 0pF				5	mA
		t_{CLK} = 125 ns C_L = 0pF	MSM82C53-2			8	mA

AC CHARACTERISTICS

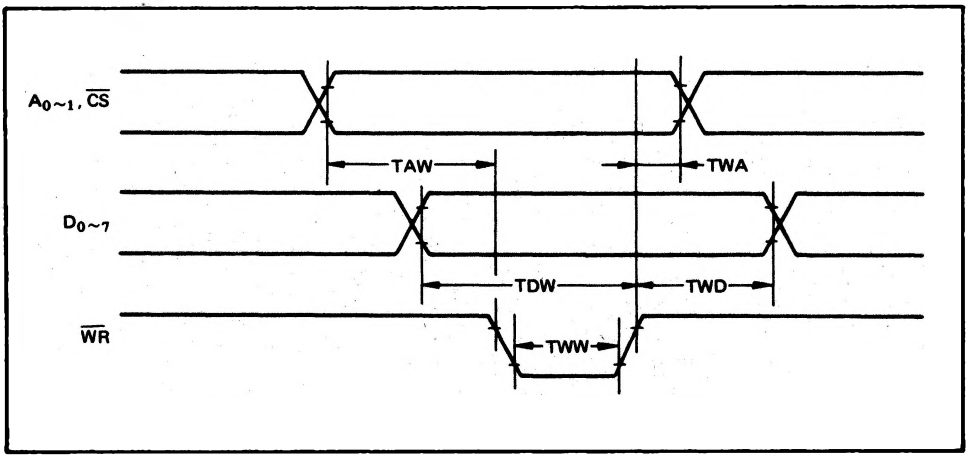
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	MSM82C53-5		MSM82C53-2		Unit	Conditions	
		Min.	Max.	Min.	Max.			
Address Set-up Time before reading	TAR	30		30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		0		ns		
Read Pulse Width	TRR	150		150		ns		
Read Recovery Time	TRVR	200		200		ns		
Address Set-up Time before writing	TAW	0		0		ns	Write cycle	
Address Hold Time after writing	TWA	30		20		ns		
Write Pulse Width	TWW	150		150		ns		
Data Input Set-up Time before writing	TDW	100		100		ns		
Data Input Hold Time after writing	TWD	30		20		ns		
Write Recovery time	TRVW	200		200		ns		
Clock Cycle Time	TCLK	200	D.C.	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		60		ns		
Clock "L" Pulse Width	TPWL	60		60		ns		
"H" Gate Pulse Width	TGW	50		50		ns		
"L" Gate Pulse Width	TGL	50		50		ns		
Gate Input Set-up Time before clock	TGS	50		50		ns		
Gate Input Hold Time after clock	TGH	50		50		ns		
Output Delay Time after reading	TRD		120		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	5	90	ns		
Output Delay Time after gate	TODG		120		120	ns		
Output Delay Time after clock	TOD		150		150	ns		
Output Delay Time after address	TAD		180		180	ns		

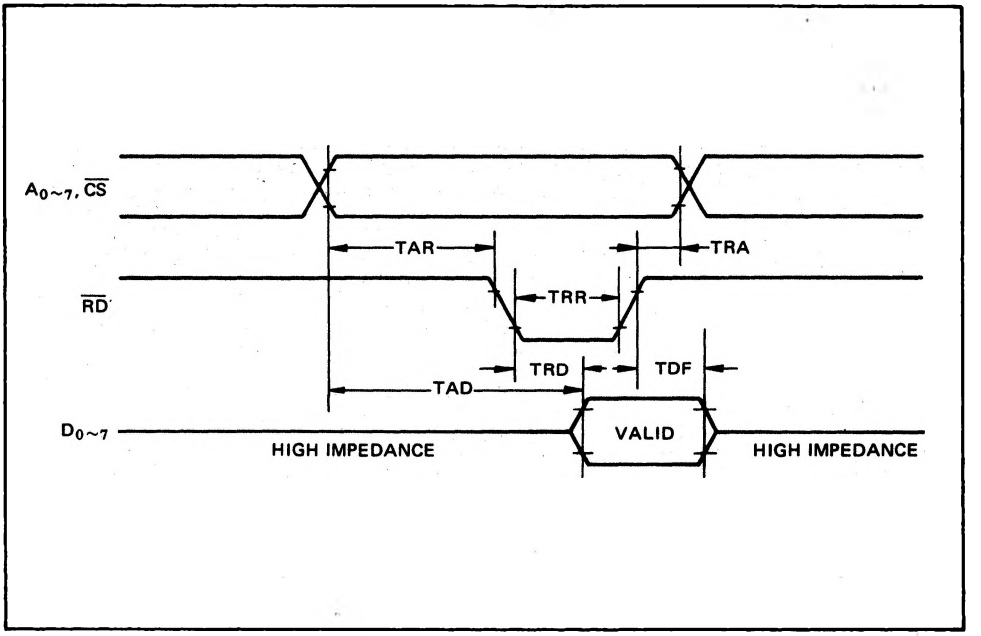
Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

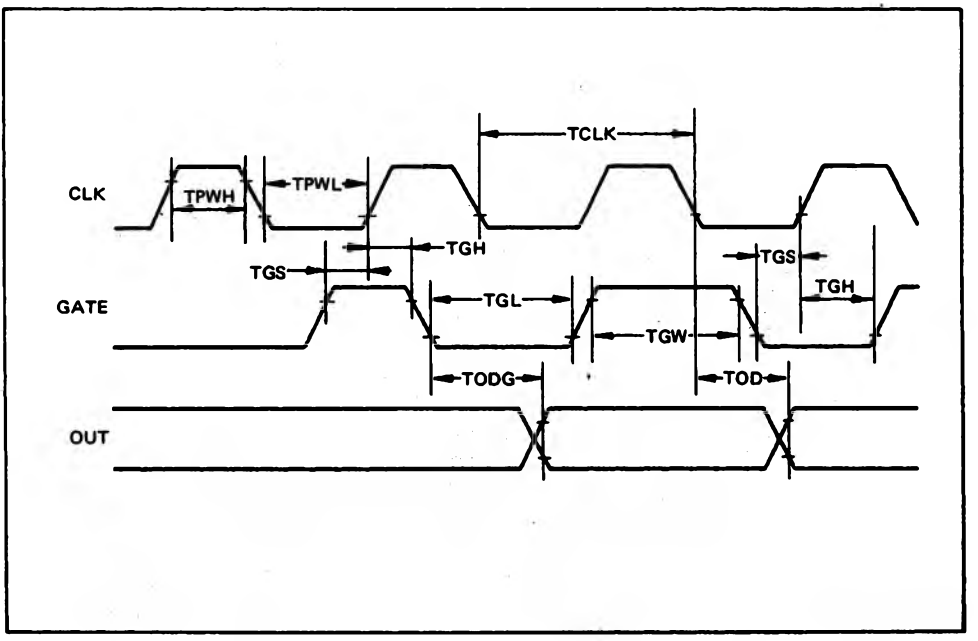
Write Timing



Read Timing



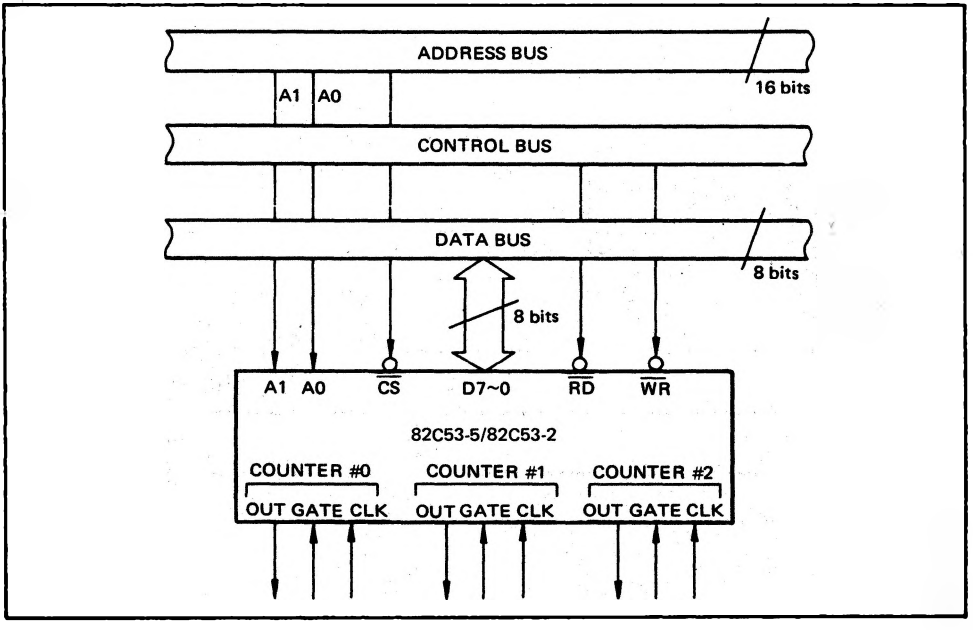
Clock & Gate Timing



DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance to the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/ Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

- **Example of control word and count value setting**

```
Counter # 0: Read/Load LSB only, Mode 3,
             Binary count, count value 3H
Counter # 1: Read/Load MSB only, Mode 5,
             Binary count, count value AA00H
Counter # 2: Read/Load LSB and MSB, Mode 0,
             BCD count, count value 1234

MVI A, 1EH
OUT n3      Counter #0 control word setting
MVI A, 6AH
OUT n3      Counter #1 control word setting
MVI A, B1H
OUT n3      Counter #2 control word setting
MVI A, 03H
OUT n0      Counter #0 count value setting
MVI A, AAH
OUT n1      Counter #1 count value setting
MVI A, 34H
OUT n2
MVI A, 12H  Counter #2 count value setting
OUT n2      (LSB then MSB)
```

Note: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**

The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.

Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.

When Count Values are written during counting, the operation is as follows:

1 byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**

The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.

Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**

The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.

An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

- **Mode 3 (square waveform rate generator)**

The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.

The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only $(n+1)/2$ clock inputs at "H" level and $(n-1)/2$ clock inputs at "L" level.

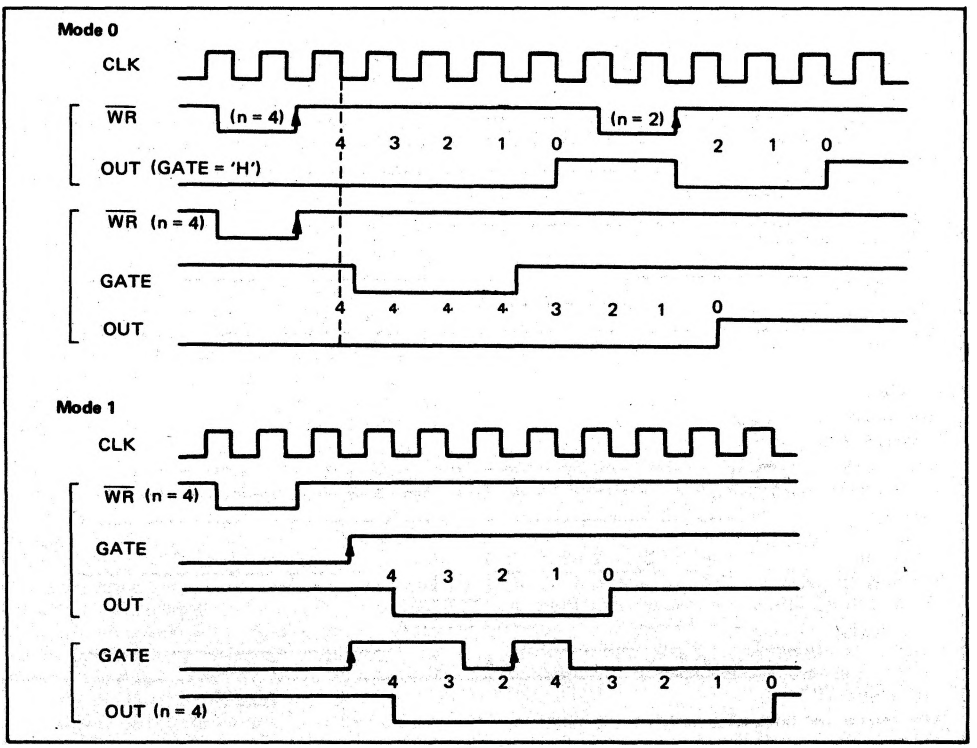
If a new count value is written during counting, the new count value is reflected immediately after the

change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

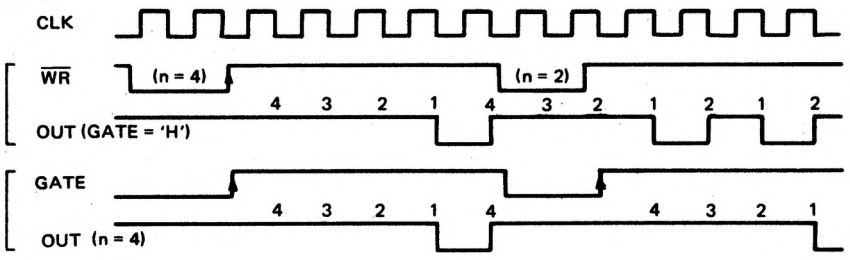
- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

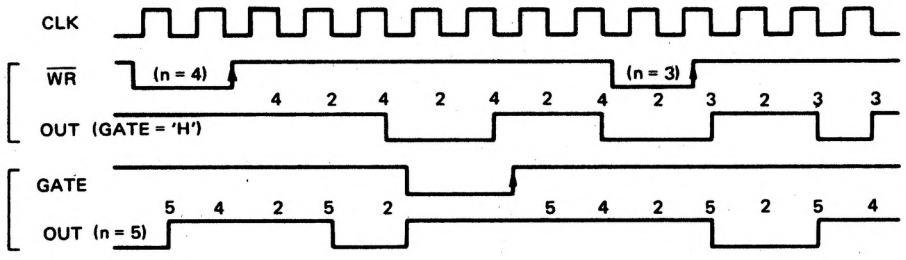
Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



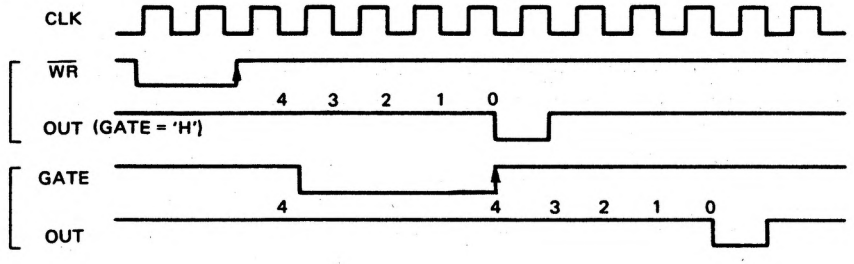
Mode 2



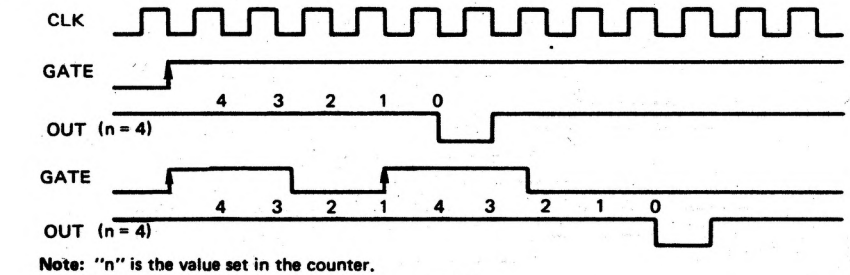
Mode 3



Mode 4



Mode 5



Note: "n" is the value set in the counter.
Figures in these diagrams refer to counter values.

Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

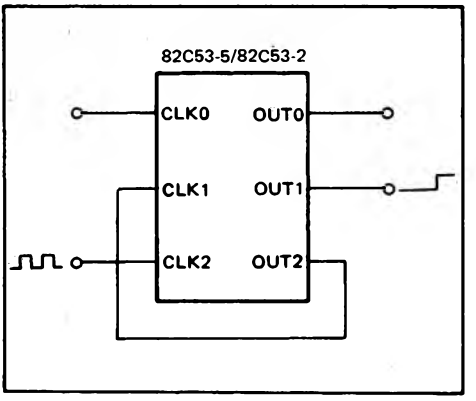
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  0 1 0 0 x x x x
         └─ Denotes counter latching
OUT n3 ──┬─ Write in control word address (n3)
         └─ The counter value at this point is latched
IN n1  ──┬─ Reading of the LSB of the counter value latched from counter #1.
         └─ n1: Counter #1 address
MOV B, A
IN n1  ──── Reading of MSB from counter #1.
MOV C, A
```

Example of Practical Application

- 82C53 used as a 32-bit counter.



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}.