OKI semiconductor

MSM82C12RS/GS

8-BIT INPUT/OUTPUT PORT

GENERAL DESCRIPTION

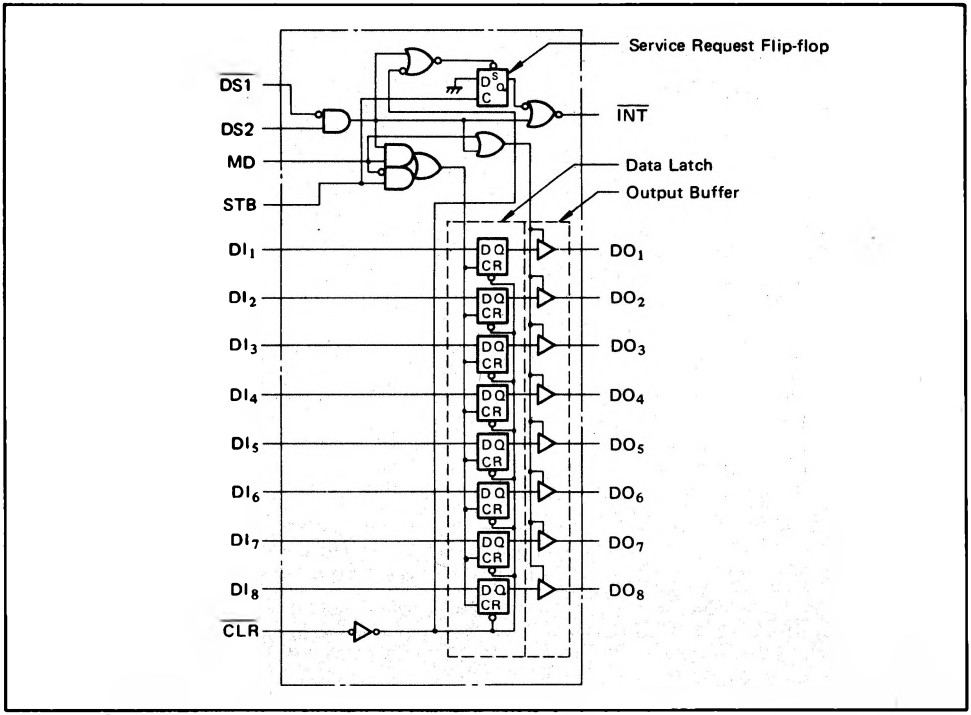
The MSM82C12 is an 8 bit input output port employing 3 μ silicon gate CMOS technology. It insures low operating power. This device incorporates a service request flip-flop for generation and control of interrupts for a CPU, in addition to an 8-bit latch circuit having a three-state output buffer.

It is effective when used as an address latch device to separate the time division bus line outputs in systems employing the MSM80C85A CPU or similar processors using multiplexed address/data bus line.

FEATURES

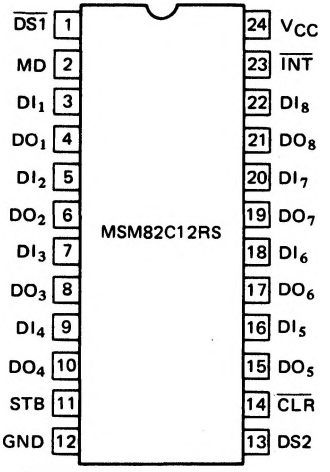
- Operated on low power consumption due to silicon gate CMOS.
- 3 V ~ 6 V single power supply
- Full static operation
- Parallel 8-bit data register and buffer
- Provided with an interrupt generating function through the adoption of a service request flip-flop
- Equipped with a clear terminal which operates asynchronously
- TTL compatible
- 24-pin DIP (MSM82C12RS)
- 24-pin flat package (MSM82C12GS)
- Functionally compatible with the 8212

CIRCUIT CONFIGURATION

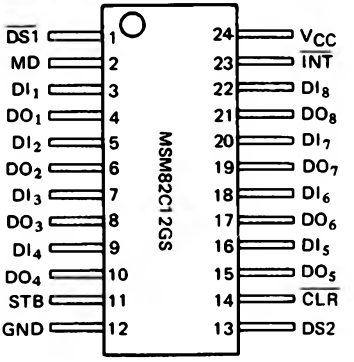


PIN CONFIGURATION

MSM82C12RS (Top View) 24 Lead Plastic DIP



MSM82C12GS (Top View) 24 Lead Plastic Flat Package



PIN DESCRIPTION

Pin Name	Item	Input/Output	Function
DI_1~DI_8	Data input	Input	These pins are 8-bit data inputs. The data input is connected to the input D pins of the 8-bit data latch circuit built inot the device.
DO_1~DO_8	Data output	Output	These pins are 8-bit data outputs. Each bit is composed of 3-state output buffers. These buffers can be made into enable or disable (high impedance status).
MD	Mode input	Input	This pin is a clock input for the data latch. It is also used to reset the internal service request flip-flop at the same time.
STB	Strobe input	Input	This pin is a clock input for the data latch. It is also used to reset the internal service request flip-flop at the same time.
$\overline{DS1}$, DS2	Device select input	Input	The AND of these two input functions make the status control of output buffers or becomes a clock input to the data latch. It also functions to perform set/reset of the internal service request flip-flop.
$\overline{CLR}$	Clear input	Input	This pin clears the internal data latch in low level. It also sets the internal service request flip-flop at this time. The clear is operated asynchronously to the clock.
$\overline{INT}$	Interrupt output	Output	This pin is the ouput of the internal service request flip-flop, but is inverted to ouptut it in low level operation.
V_{CC}			+5V power supply
GND			GND

FUNCTIONAL DESCRIPTION

Output Buffer Status Control and Data Latch Clock Input

When the input MD is at high level, the ouptut buffer is enabled and the device select input (DS1.DS2) becomes the clock input to the data latch. When the input MD is in low level, the status of the output buffer is determined by the device select input (DS1.DS2) (the output buffer is enabled when (DS1.DS2) is in high level). At this time, the input STB becomes the clock input to the data latch.

MD	$(\overline{DS1} \cdot DS2)$	STB	$DO_1 \sim DO_8$
0	0	0	High impedance status
0	0	1	High impedance status
1	0	0	Data latch
1	0	1	Data latch
0	1	0	Data latch
0	1	1	Data in
1	1	0	Data in
1	1	1	Data in

Service Request Flip-flop

The service request flip-flop is used to generate and control the interrupt for the CPU when the MSM82C12 is used as an input/output port in a microcomputer system. The flip-flop is set asynchronously by input CLR. When the flip-flop is set, the system is in non-interrupt status.

$\overline{CLR}$	$(\overline{DS1} \cdot DS2)$	STB	Q	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↓	1	0
1	1	0	1	0
1	0	0	1	1
1	0	↓	0	0

Clear

When the clear input becomes low level, the internal data latch is cleared irrespective of the clock and becomes low level.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits		Unit
			MSM82C12RS	MSM82C12GS	
Supply Voltage	V_{CC}	With respect to GND	−0.5 to +7		V
Input Voltage	V_{IN}		−0.5 to V_{CC}+0.5		V
Output Voltage	V_{OUT}		−0.5 to V_{CC}+0.5		V
Storage Temperature	T_{stg}		−55 to +150		°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to +85	°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA	V_{CC} = −4.5V to 5.5V Ta = −40°C to +85°C			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −4mA		3.7			V
Input Leak Current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{CC}$		−10		10	μA
Supply Current (Standby)	I_{CCS}	$V_{IH} \geqq V_{CC} - 0.2V$ $V_{IL} \leqq 0.2V$			0.1	100	μA
Average Supply Current (active)	I_{CC}	f = 1 MHz				1	mA

AC CHARACTERISTICS

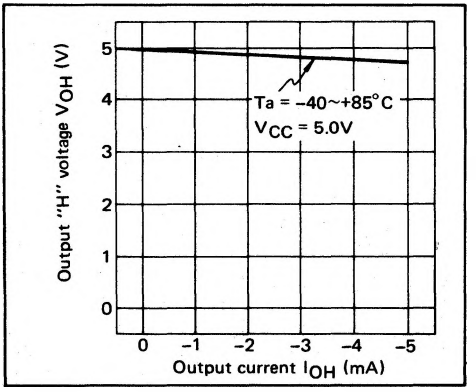
(V_{CC} = 4.5 ~ 5.5V, Ta = −40°C +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Pulse Width	t_{PW}	30			ns	Load 30pF
Data to Output Delay	t_{PD}		20	45	ns	
Write Enable to Output Delay	t_{WE}		31	60	ns	
Data Set Up Time	t_{SET}	15			ns	
Data Hold Time	t_H	30			ns	
Clear to Output Delay	t_C		19	40	ns	
Reset to Output Delay	t_R		21	45	ns	
Set to Output Delay	t_S		25	45	ns	
Output Enable Time	t_E		52	90	ns	Load 20pF + 1 kΩ
Output Disable Time	t_D		30	55	ns	

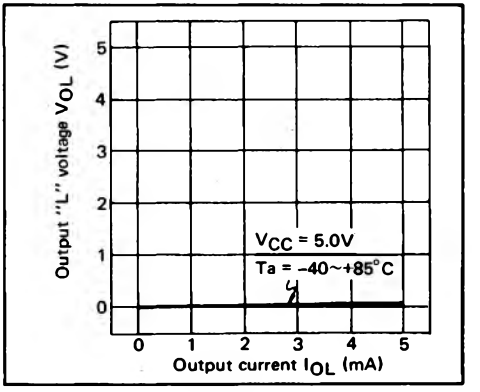
Note: TYP is measured where V_{CC} = 5 V and Ta = 25°C.
Timing is measured where VL = VH = 1.5V in both input and output.
t_E and t_D are measured at V_{OL} + 0.5V or V_{OH} − 0.5V when the two are made into high impedance status.

OUTPUT CHARACTERISTICS (DC Characteristics Reference Value)

(1) Output "H" voltage (V_{OH}) vs. output current (I_{OH})



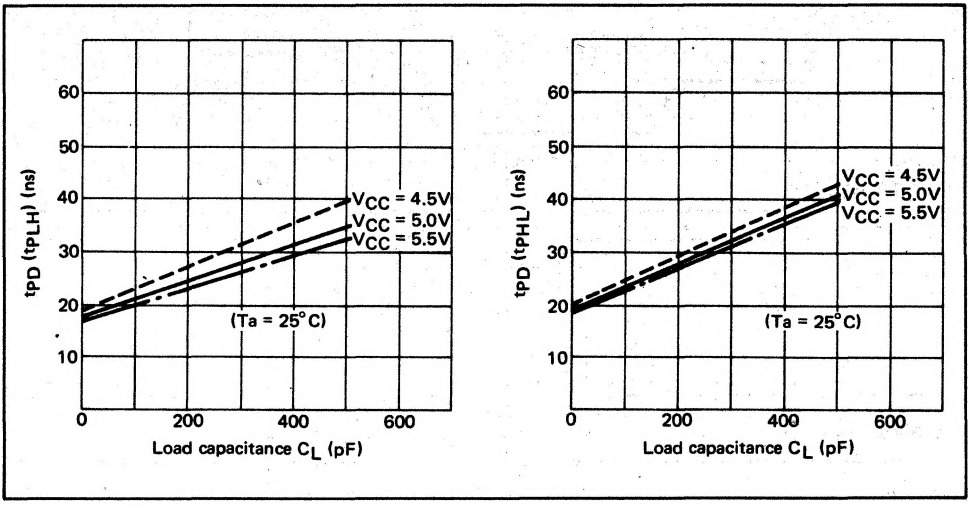
(2) Output "L" voltage (V_{OL}) vs. output current (I_{OL})



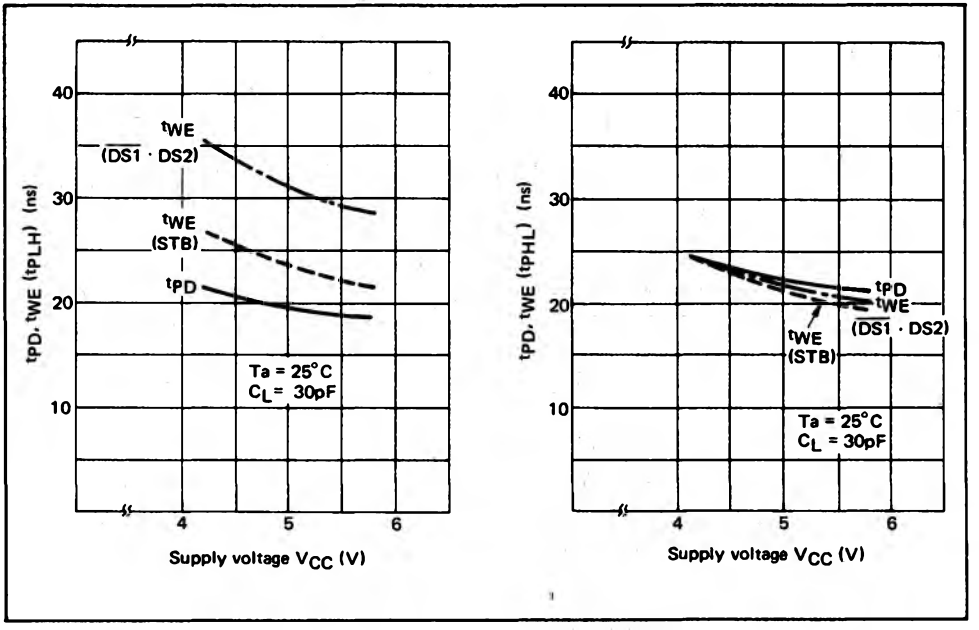
Note: The direction of flow in is taken as positive for output current.

OUTPUT CHARACTERISTICS (AC Characteristics Reference Value)

(1) t_{PD} vs. load capacitance

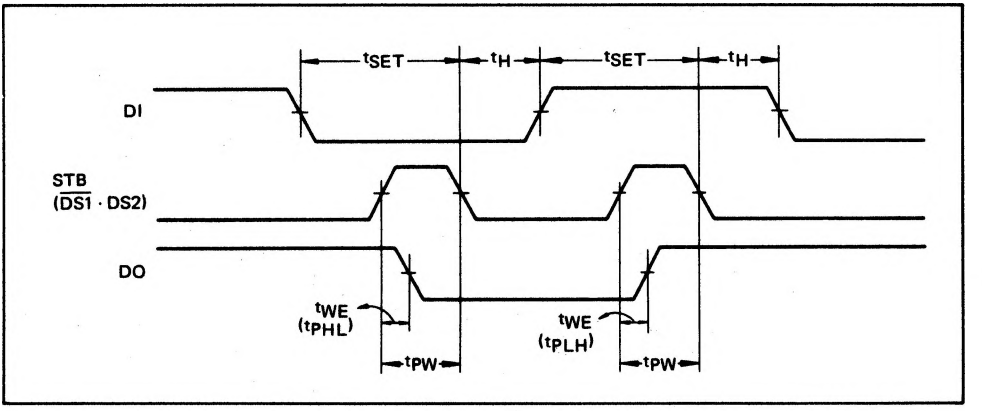


(2) t_{PD} and t_{WE} vs. supply voltage

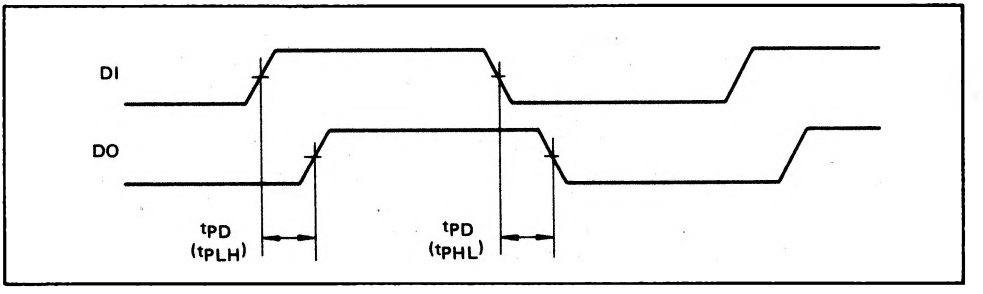


TIMING CHART

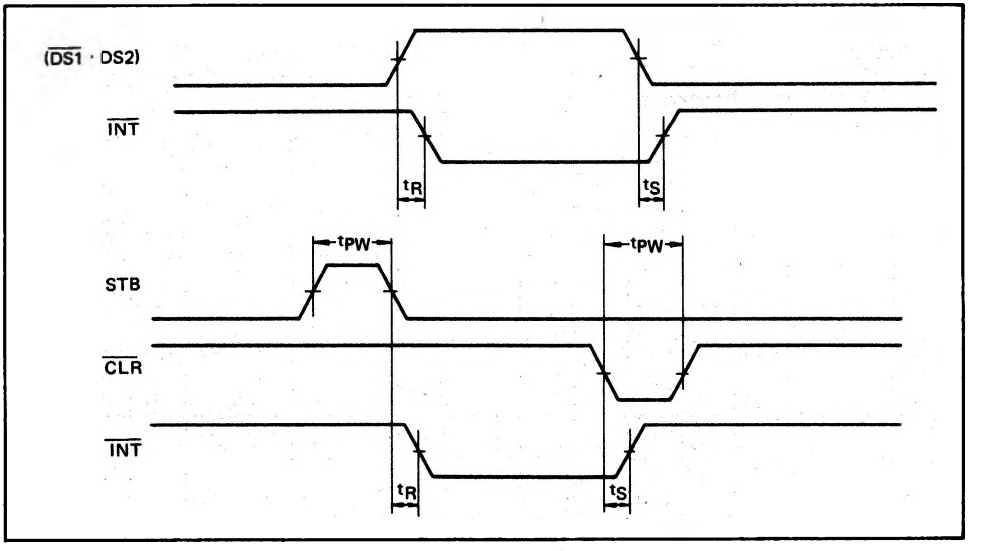
Data Latch Operation



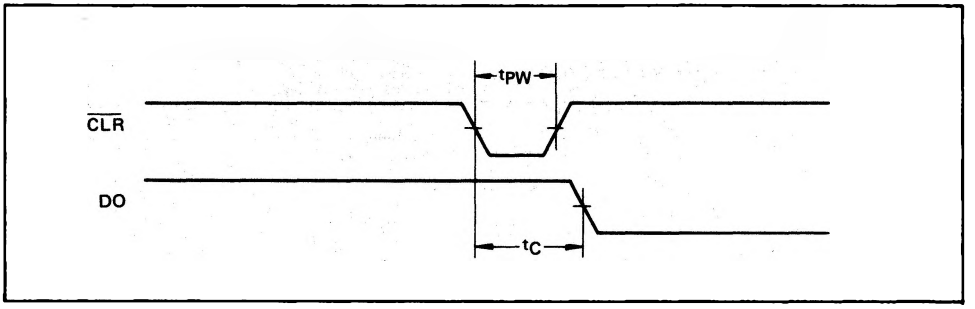
Gate Buffer Operation



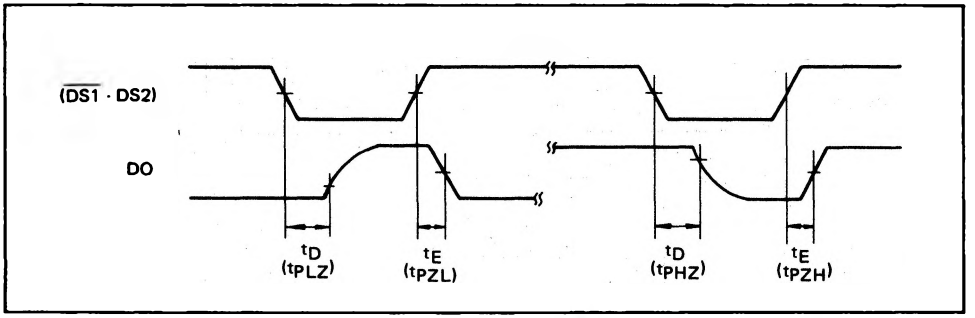
Interrupt Operation



Clear Operation



Output Buffer Enable/Disable (High Impedance Status) Operation



EXAMPLE OF APPLICATION OF MSM82C12

Address Latch of MSM80C85A

Used to separate the time division data bus (8 low order bits of the address bus and 8-bit data bus) into the address bus and data bus by means of the ALE (Address Latch Enable) signal.