OKI semiconductor

MSM80C85A RS/GS/JS

8-BIT CMOS MICROPROCESSOR

GENERAL DESCRIPTION

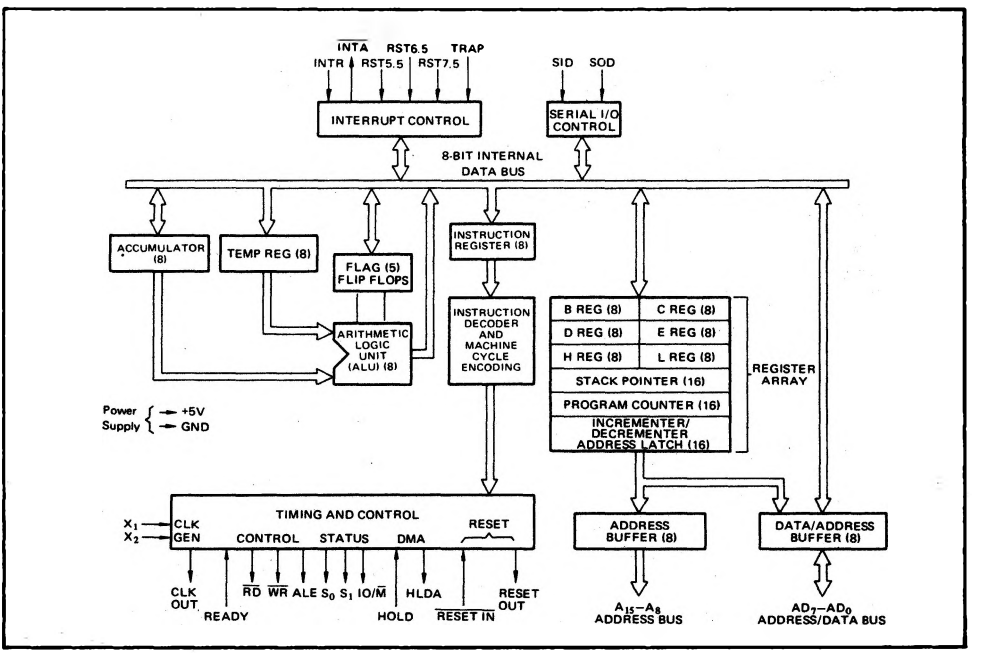
The MSM80C85A is a complete 8-bit parallel central processor implemented in silicon gate C-MOS technology. It is designed with the same processing speed and lower power consumption compared with MSM8085A, thereby offering a high level of system integration.

The MSM80C85A uses a multiplexed address/data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of MSM81C55/MSM83C55 memory products allow a direct interface with the MSM80C85A.

FEATURES

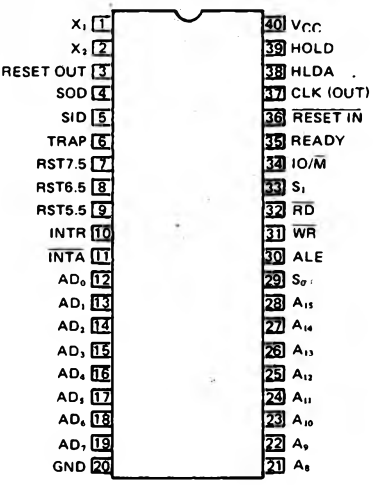
- Low Power Dissipation: 50 mW Typ
- Single +4 to +6 V Power Supply
- –40 to +85°C, Operating Temperature
- 1.3μ Instruction Cycle
- On-Chip Clock Generator (with External Crystal)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- TTL Compatible
- Four Vectored Interrupt Inputs (One is non-maskable) Plus the 8080A-compatible interrupt.
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Addressing Capability to 64K Bytes of Memory
- 40-pin Plastic DIP (MSM80C85ARS)
- 44-pin Plastic Flat Package (MSM80C85AGS)
- 44-pin PLCC Package (MSM80C85AJS)

FUNCTIONAL BLOCK DIAGRAM

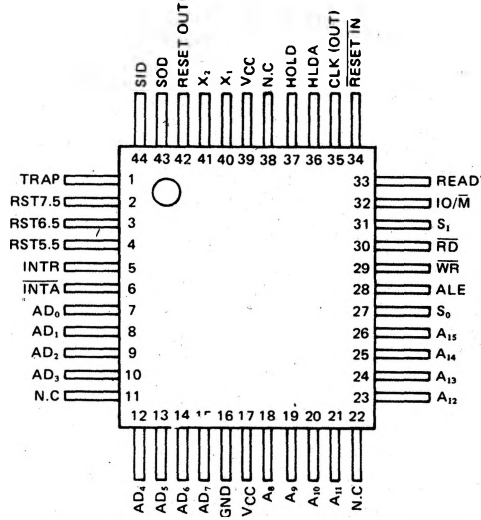


PIN CONFIGURATION

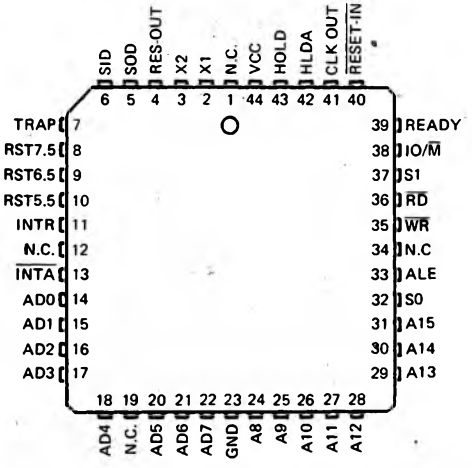
MSM80C85ARS (Top View)
40 Lead Plastic DIP



MSM80C85AGS (Top View)
44 Lead Plastic Flat Package



MSM80C85AJS (Top View)
44 Plastic Leaded Chip Carrier



MSM80C85A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol	Function
A_8–A_{15} (Output, 3-state)	Address Bus: The most significant 8-bits of the memory address or the 8-bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_0–AD_7 (Input/Output) 3-state	Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE (Output)	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, IO/$\overline{M}$ (Output)	Machine cycle status: IO/$\overline{M}$ S_1 S_0 States 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge 0 0 Halt · = 3-state x x Hold (high impedance) x x Reset x = unspecified S_1 can be used as an advanced R/W status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$ (Output, 3-state)	READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$ (Output, 3-state)	WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR, 3-stated during Hold and Halt modes and during RESET.
READY (Input)	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD (Input)	HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA (Output)	HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR (Input)	INTERRUPT REQUEST: Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) $\overline{RD}$ during the instruction cycle after an INTR is accepted.
RST 5.5 RST 6.5 RST 7.5 (Input)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same timing as INTR or RST 5.5–7.5. It is unaffected by any mask or Interrupt Disable. It has the highest priority of any interrupt. (See Table 1.)

Symbol	Function
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
GND	Ground Reference.

Table 1 Interrupt Priority, Restart Address, and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge and high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	(2)	High level until sampled.

Notes: (1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

FUNCTIONAL DESCRIPTION

The MSM80C85A is a complete 8-bit parallel central processor. It is designed with silicon gate C-MOS technology and requires a single +5 volt supply. Its basic clock speed is 3MHz, thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (MSM80C85A), a RAM/IO (MSM81C55), and a ROM/IO chip (MSM83C55).

The MSM80C85A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or a 16-bit register pairs. The MSM-80C85A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8-bits
PC	Program Counter	16-bit address
BC, DE, HL	General-Purpose Registers; data pointer (HL)	8-bit x 6 or 16-bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The MSM80C85A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data Bus. These lower 8-bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The MSM80C85A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1 and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. Hold and all Interrupts are synchronized with the processor's internal clock. The MSM80C85A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for a simple serial interface.

In addition to these features, the MSM80C85A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.

INTERRUPT AND SERIAL I/O

The MSM80C85A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP, INTR is identical in function to the 8080A INT. Each of the three RESTART inputs, 5.5, 6.5, and 7.5, has a programmable mask. TRAP is also a RESTART interrupt but it is nonmaskable.

The three maskable interrupts cause the internal execution of RESTART (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RESTART vector independent of the state of the interrupt enable or masks. (See Table 1.)

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the 8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive.

For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a $\overline{RESET\ IN}$ to the MSM80C85A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP—highest priority, RST 7.5, RST 6.5, RST 5.5, INTR—lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt an RST 7.5 routine if the interrupts are re-enabled before the end of the RST 7.5 routine.

The TRAP interrupt is useful for catastrophic events such as power failure or bus error. The TRAP input is recognized just as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high until it is acknowledged. It will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. Figure 3 illustrates the TRAP interrupt request circuitry within the MSM80C85A. Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it disables interrupts, but preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR or RST 5.5–7.5 will provide current interrupt Enable status, revealing that interrupts are disabled.

The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

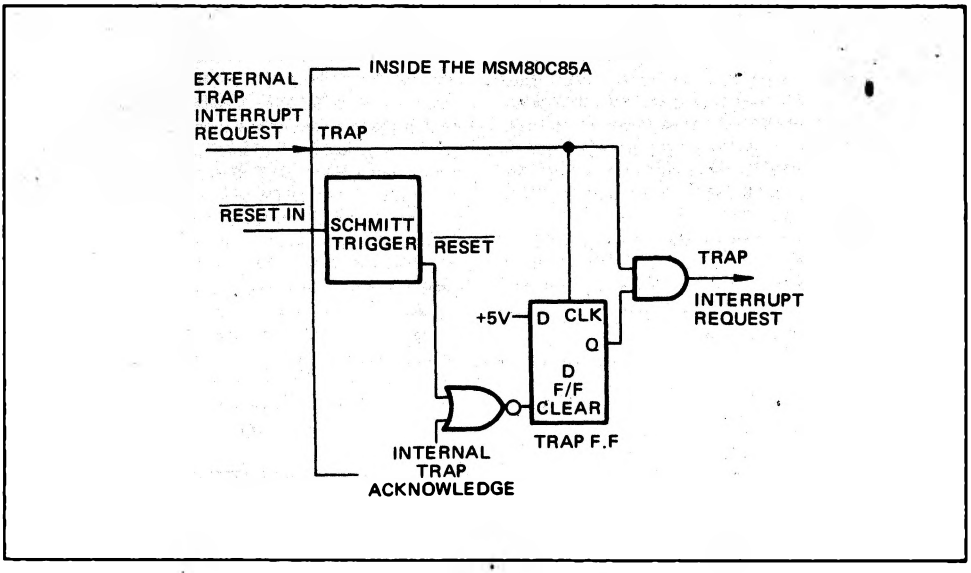


Figure 3 Trap and $\overline{\text{RESET IN}}$ Circuit

DRIVING THE X_1 and X_2 INPUTS

You may drive the clock inputs of the MSM80C-85A with a crystal, or an external clock source. The driving frequency must be at least 1 MHz, and must be twice the desired internal clock frequency; hence, the MSM80C85A is operated with a 6 MHz cyrstal (for 3 MHz clock). If a crystal is used, it must have the following characteristics:

Parallel resonance at twice the clock frequency desired
C_L (load capacitance) $\leq$ 30 pF
C_S (shunt capacitance) $\leq$ 7 pF
R_S (equivalent shunt resistance) $\leq$ 75 ohms
Drive level: 10 mW
Frequency tolerance: ±.005% (suggested)

Note the use of the capacitors between X_1, X_2 and ground. These capacitors are required to assure oscillator startup at the correct frequency.

Figure 4 shows the recommended clock driver circuits. Note in B that a pullup resistor is required to assure that the high level voltage of the input is at least 4V.

For driving frequencies up to and including 6 MHz you may supply the driving signal to X_1 and leave X_2 open-circuited (Figure 4B). To prevent self-oscillation of the MSM80C85A, be sure that X_2 is not coupled back to X_1 through the driving circuit.

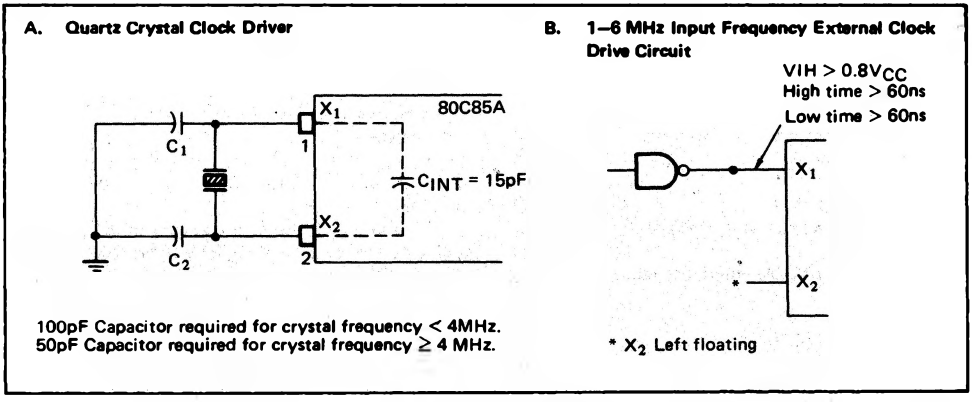


Figure 4 Clock Driver Circuits

BASIC SYSTEM TIMING

The MSM80C85A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8-bits of address on the Data Bus. Figure 5 shows an instruction fetch, memory read and I/O write cycle (as would occur during processing of the OUT instruction). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

There are seven possible types of machine cycles. Which of these seven takes place is defined by the status of the three status lines ($IO/\overline{M}$, S_1, S_0) and the three control signals ($\overline{RD}$, $\overline{WR}$, and $\overline{INTA}$). (See Table 2.) The status line can be used as advanced controls (for device selection, for example), since they become active at the T_1 state, at the outset of each machine cycle. Control lines $\overline{RD}$ and $\overline{WR}$ become active later, at the time when the transfer of data is to take place, so are used as command lines.

A machine cycle normally consists of three T states, with the exception of OPCODE FETCH, which normally has either four or six T states (unless $\overline{WAIT}$ or HOLD states are forced by the receipt of $\overline{READY}$ or HOLD inputs). Any T state must be one of ten possible states, shown in Table 3.

Table 2 MSM80C85A Machine Cycle Chart

Machine Cycle		Status			Control		
		$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	(OF)	0	1	1	0	1	1
Memory Read	(MR)	0	1	0	0	1	1
Memory Write	(MW)	0	0	1	1	0	1
I/O Read	(IOR)	1	1	0	0	1	1
I/O Write	(IOW)	1	0	1	1	0	1
Acknowledge of INTR	(INA)	1	1	1	1	1	0
Bus Idle	(BI): DAD	0	1	0	1	1	1
	RST, TRAP						
	HALT	1	1	1	1	1	1
		TS	0	0	TS	TS	1

Table 3 MSM80C85A Machine State Chart

Machine State	Status & Buses				Control		
	S_1, S_0	$IO/\overline{M}$	A_8–A_{15}	AD_0–AD_7	$\overline{RD}, \overline{WR}$	$\overline{INTA}$	ALE
T_1	X	X	X	X	1	1	1 (1)
T_2	X	X	X	X	X	X	0
T_{WAIT}	X	X	X	X	X	X	0
T_3	X	X	X	X	X	X	0
T_4	1	0 (2)	X	TS	1	1	0
T_5	1	0 (2)	X	TS	1	1	0
T_6	1	0 (2)	X	TS	1	1	0
T_{RESET}	X	TS	TS	TS	TS	1	0
T_{HALT}	0	TS	TS	TS	TS	1	0
T_{HOLD}	X	TS	TS	TS	TS	1	0

0 = Logic "0"
1 = Logic "1"
TS = High Impedance
X = Unspecified

Notes: (1) ALE not generated during 2nd and 3rd machine cycles of DAD instruction.
(2) $IO/\overline{M}$ = 1 during T_4~T_6 of INA machine cycle.

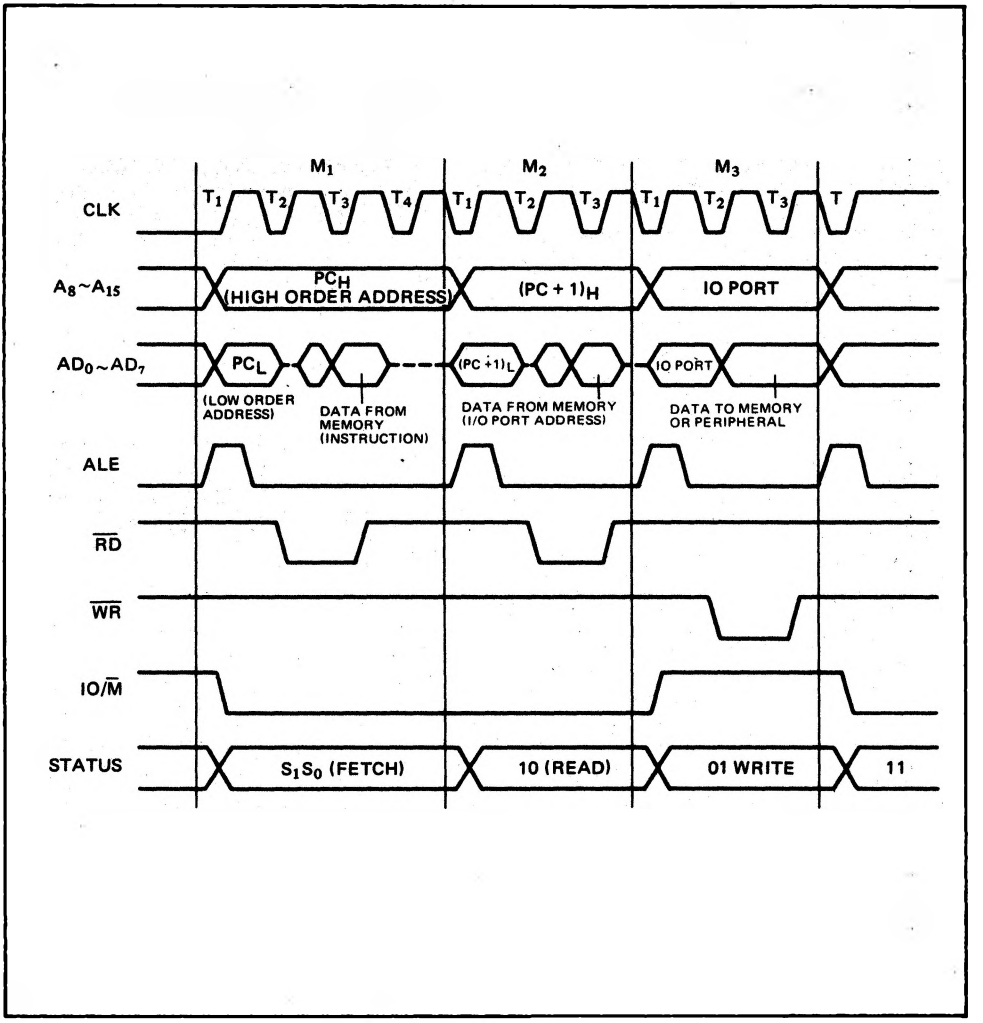


Figure 5· MSM80C85A Basic System Timing

Table 4 Absolute Maximum Ratings

Ambient Temperature under Bias	−40°C to + 85°C
Storage Temperature	−55°C to + 150°C
Supply Voltage Respect to Ground	−0.3V to + 7.0V
Input Voltage Respect to Ground	−0.3V to V_{CC} + 0.3V
Power Dissipation	1.0 Watt (DIP)
	0.7 Watt (FLAT)
	1.0 Watt (PLCC)

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

(T_A = –40°C to + 85°C; V_{CC} = 5V ±10%; unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Low Voltage	V_{IL}	–0.3		+0.8	V	
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = –400μA
		4.2			V	I_{OH} = –40μA
Input Leak	I_{LI}	–10		10	μA	$0V \leq V_{IN} \leq V_{CC}$
Output Leak	I_{LO}	–10		10	μA	$0V \leq V_{OUT} \leq V_{CC}$
Input Low Level, RESET	V_{ILR}	–0.3		+0.8	V	
Input High Level, RESET	V_{IHR}	3.0		V_{CC} + 0.3	V	
Hysteresis, RESET	V_{HY}	0.25			V	
Power Supply Current	I_{CC}		10	22	mA	V_{CC} = 4.5V to 5.5V, T_A = –40°C to +85°C, t_{CYC} = 320ns
			10	17	mA	V_{CC} = 4.75V to 5.25V, T_A = 0°C to +85°C, Reset Active, CL=0pF
Power Supply Voltage	V_{CC}	4	5	6	V	

A.C. CHARACTERISTICS

(T_A = –40°C to 85°C; V_{CC} = 5V ±10%)

Parameter	Symbol	80C85A		Units
		Min.	Max.	
CLK Cycle Period	t_{CYC}	320	2000	ns
CLK Low Time	t_1	80		ns
CLK High Time	t_2	120		ns
CLK Rise and Fall Time	t_r, t_f		30	ns
X_1 Rising to CLK Rising	t_{XKR}	30	120	ns
X_1 Rising to CLK Falling	t_{XKF}	30	150	ns
$A_{8\sim15}$ Valid to Leading Edge of Control (1)	t_{AC}	270		ns
$A_{0\sim7}$ Valid to Leading Edge of Control	t_{ACL}	240		ns
$A_{0\sim15}$ Valid to Valid Data In	t_{AD}		575	ns
Address Float After Leading Edge of $\overline{RD}$ ($\overline{INTA}$)	t_{AFR}		0	ns
$A_{8\sim15}$ Valid Before Trailing Edge of ALE(1)	t_{AL}	115		ns
$A_{0\sim7}$ Valid Before Trailing Edge of ALE	t_{ALL}	90		ns
READY Valid from Address Valid	t_{ARY}		220	ns
Address (A_8–A_{15}) Valid After Control	t_{CA}	120		ns
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		ns
Trailing Edge of Control to Leading Edge of ALE	t_{CL}	50		ns
Data Valid to Trailing Edge of $\overline{WR}$	t_{DW}	420		ns
HLDA to Bus Enable	t_{HABE}		210	ns
Bus Float After HLDA	t_{HABF}		210	ns

A.C. CHARACTERISTICS (cont'd)

Parameter	Symbol	80C85A		Units
		Min.	Max.	
HLDA Valid to Trailing Edge of CLK	t_{HACK}	110		ns
HOLD Hold Time	t_{HDH}	0		ns
HOLD Setup Time to Trailing Edge of CLK	t_{HDS}	170		ns
INTR Hold Time	t_{INH}	0		ns
INTR, RST, and TRAP Setup Time to Falling Edge of CLK	t_{INS}	160		ns
Address Hold Time After ALE	t_{LA}	100		ns
Trailing Edge of ALE to Leading Edge of Control	t_{LC}	130		ns
ALE Low During CLK High	t_{LCK}	100		ns
ALE to Valid Data During Read	t_{LDR}		460	ns
ALE to Valid Data During Write	t_{LDW}		200	ns
ALE Width	t_{LL}	140		ns
ALE to READY Stable	t_{LRY}		110	ns
Trailing Edge of $\overline{RD}$ to Re-Enabling of Address	t_{RAE}	150		ns
$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300	ns
Control Trailing Edge to Leading Edge of Next Control	t_{RV}	400		ns
Data Hold Time After $\overline{RD}$ $\overline{INTA}$ (7)	t_{RDH}	0		ns
READY Hold Time	t_{RYH}	0		ns
READY Setup Time to Leading Edge of CLK	t_{RYS}	110		ns
Data Valid After Trailing Edge of $\overline{WR}$	t_{WD}	100		ns
LEADING Edge of $\overline{WR}$ to Data Valid	t_{WDL}		40	ns

Notes: (1) A_8–A_{15} address Specs apply to IO/$\overline{M}$, S_0, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.

(2) Test conditions: t_{CYC} = 320ns C_L = 150pF

(3) For all output timing where C_L = 150pF use the following correction factors:
25pF ≤ C_L < 150pF: –0.10ns/pF
150pF < C_L ≤ 300pF: +0.30ns/pF

(4) Output timings are measured with purely capacitive load.

(5) All timings are measured at output voltage V_L = 0.8V, V_H = 2.2V, and 1.5V with 10ns rise and fall time on inputs.

(6) To calculate timing specifications at other values of t_{CYC} use Table 7.

(7) Data hold time is guaranteed under all loading conditions.

Input Waveform for A.C. Tests:

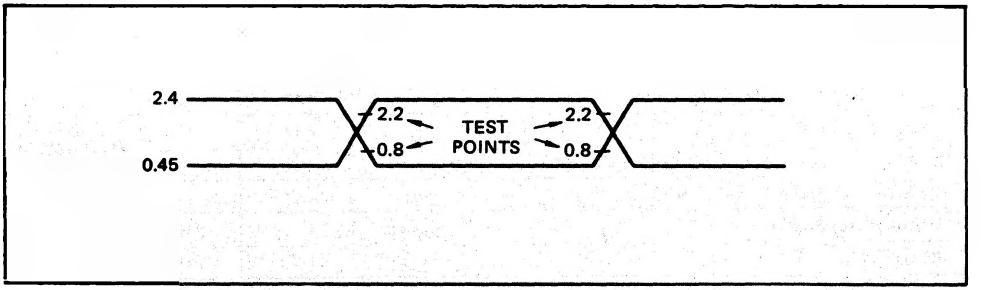


Table 7 Bus Timing Specification as a T_{CYC} Dependent

MSM80C85A			
t_{AL}	–	(1/2)T – 45	MIN
t_{LA}	–	(1/2)T – 60	MIN
t_{LL}	–	(1/2)T – 20	MIN
t_{LCK}	–	(1/2)T – 60	MIN
t_{LC}	–	(1/2)T – 30	MIN
t_{AD}	–	(5/2 + N)T – 225	MAX
t_{RD}	–	(3/2 + N)T – 180	MAX
t_{RAE}	–	(1/2)T – 10	MIN
t_{CA}	–	(1/2)T – 40	MIN
t_{DW}	–	(3/2 + N)T – 60	MIN
t_{WD}	–	(1/2)T – 60	MIN
t_{CC}	–	(3/2 + N)T – 80	MIN
t_{CL}	–	(1/2)T – 110	MIN
t_{ARY}	–	(3/2)T – 260	MAX
t_{HACK}	–	(1/2)T – 50	MIN
t_{HABF}	–	(1/2)T + 50	MAX
t_{HABE}	–	(1/2)T + 50	MAX
t_{AC}	–	(2/2)T – 50	MIN
t_1	–	(1/2)T – 80	MIN
t_2	–	(1/2)T – 40	MIN
t_{RV}	–	(3/2)T – 80	MIN
t_{LDR}	–	(2+N)T – 180	MAX

Note: N is equal to the total WAIT states.
T = t_{CYC}

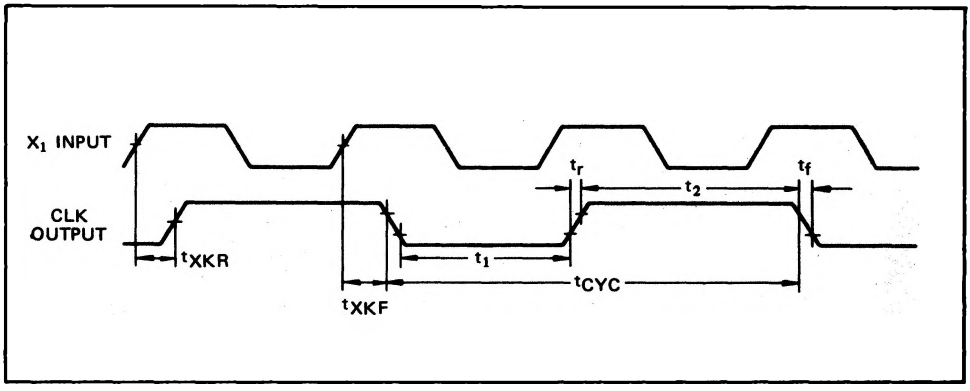
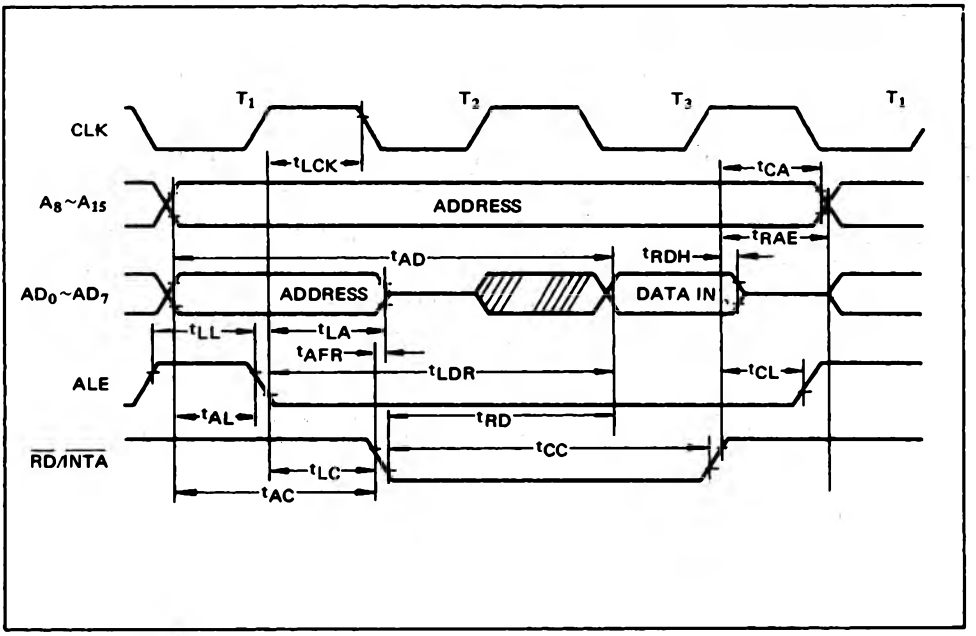
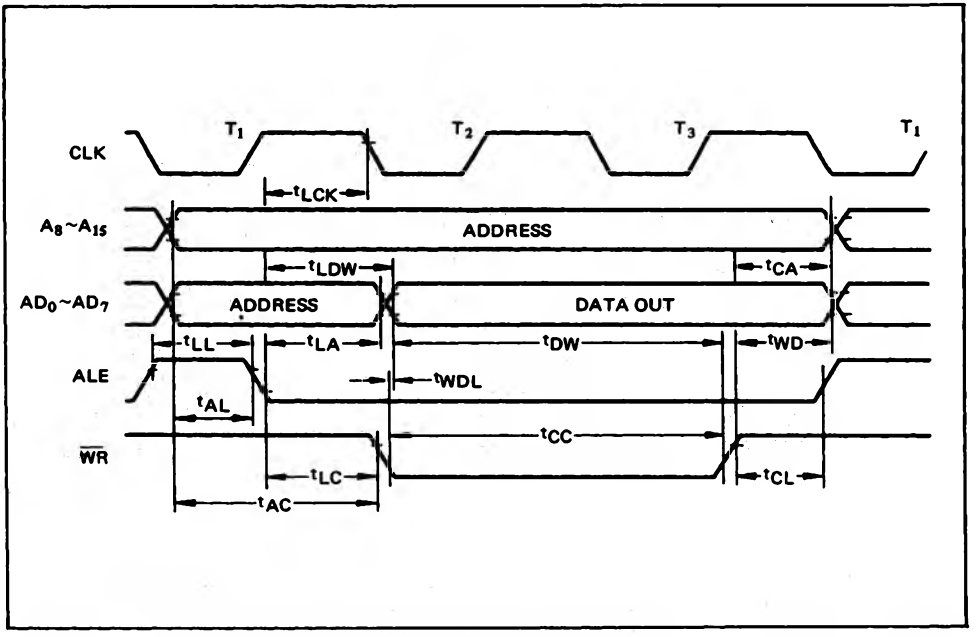


Figure 6 Clock Timing Waveform

READ OPERATION



WRITE OPERATION



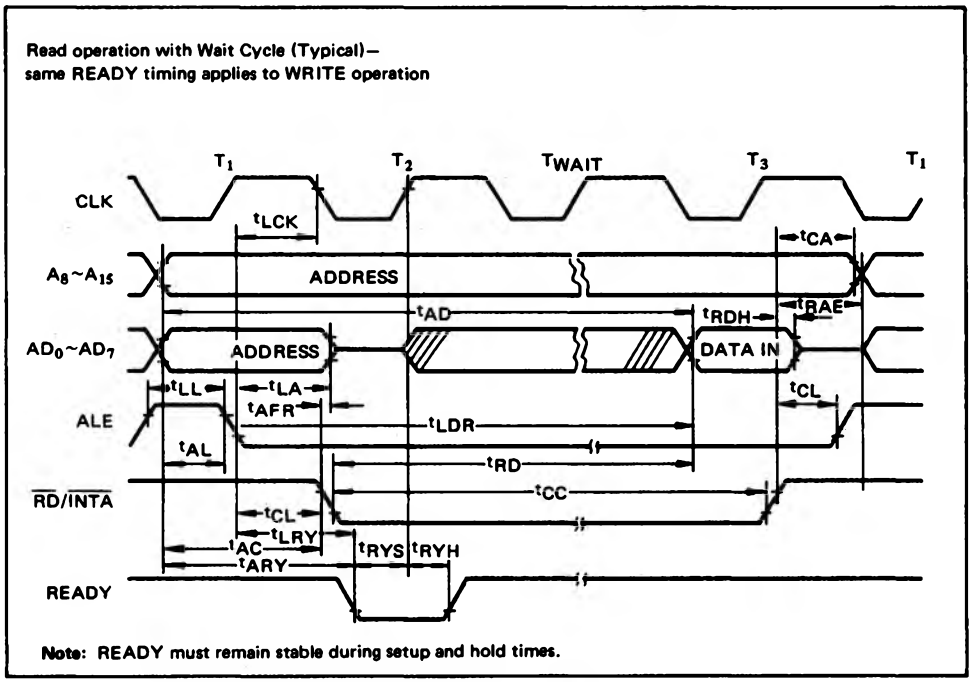


Figure 7 MSM80C85A Bus Timing, With and Without Wait

HOLD OPERATION

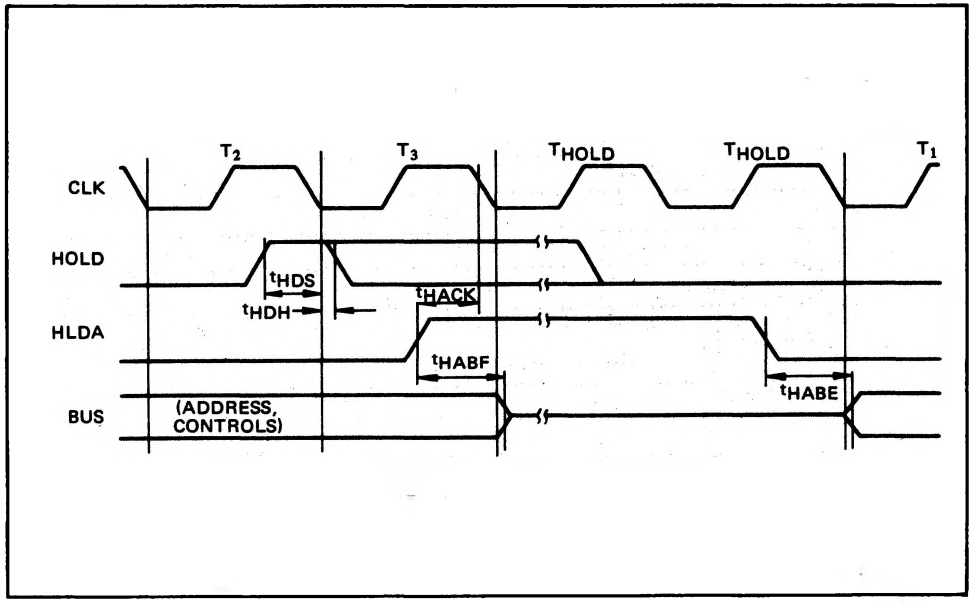
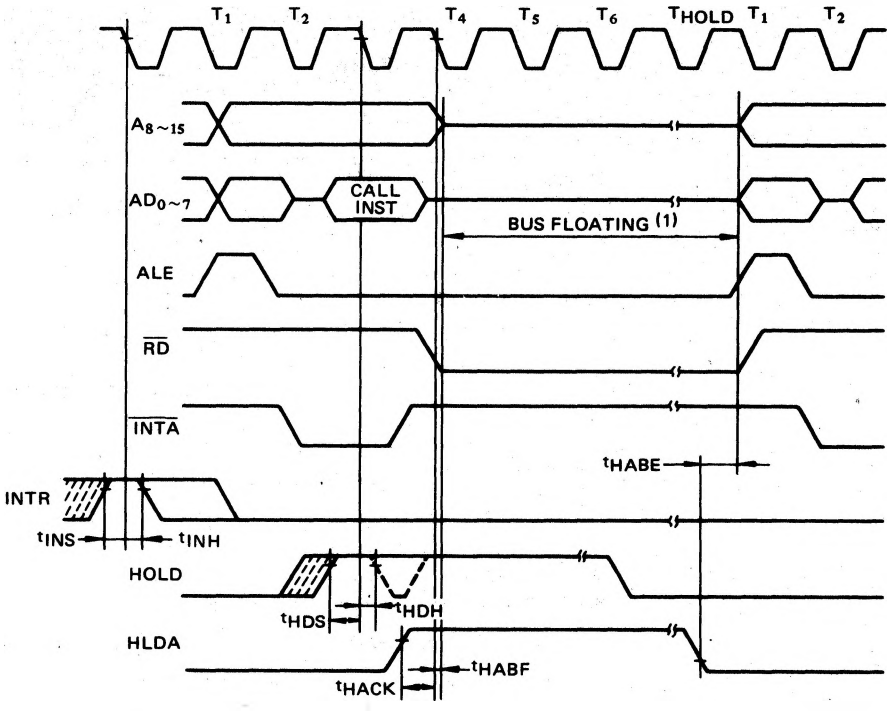


Figure 8 MSM80C85A Hold Timing



Note: (1) IO/$\overline{M}$ is also floating during this time.

Figure 9 MSM80C85A Interrupt and Hold Timing

Table 8 Instruction Set Summary

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock (2) Cycles
MOVE, LOAD, AND STORE										
MOVr1 r2	Move register to register	0	1	D	D	D	S	S	S	4
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	12
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	12
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	12
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	12
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	16
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	6
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	7/10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	7/10
JZ	Jump on zero	1	1	0	0	1	0	1	0	7/10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	7/10
JP	Jump on positive	1	1	1	1	0	0	1	0	7/10
JM	Jump on minus	1	1	1	1	1	0	1	0	7/10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	7/10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	7/10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	6
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	18
CC	Call on carry	1	1	0	1	1	1	0	0	9/18
CNC	Call on no carry	1	1	0	1	0	1	0	0	9/18
CZ	Call on zero	1	1	0	0	1	1	0	0	9/18
CNZ	Call on no zero	1	1	0	0	0	1	0	0	9/18
CP	Call on positive	1	1	1	1	0	1	0	0	9/18
CM	Call on minus	1	1	1	1	1	1	0	0	9/18
CPE	Call on parity even	1	1	1	0	1	1	0	0	9/18
CPO	Call on parity odd	1	1	1	0	0	1	0	0	9/18

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code(1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock(2) Cycles
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	6/12
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12
RNZ	Return on no zero	1	1	0	0	0	0	0	0	6/12
RP	Return on positive	1	1	1	1	0	0	0	0	6/12
RM	Return on minus	1	1	1	1	1	0	0	0	6/12
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	12
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	4
DCR r	Decrement register	0	0	D	D	D	1	0	1	4
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	6
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	6
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	6
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	6
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	6
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	6
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	6
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	6
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7

Table 8 Instruction Set Summary cont'd

Mnemonic	Description	Instruction Code (1) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock(2) Cycles
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
CONTROL										
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable Interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	5
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4

Notes: (1) DDD or SSS. B 000. C 001. D 010. E 011. H 100. L 101. Memory 110. A 111.
(2) Two possible cycle times, (6/12) indicate instruction cycles dependent on condition flags.