OKI semiconductor

MSM6243

SPEECH SYNTHESIS LSI WITH 192 KBIT ROM

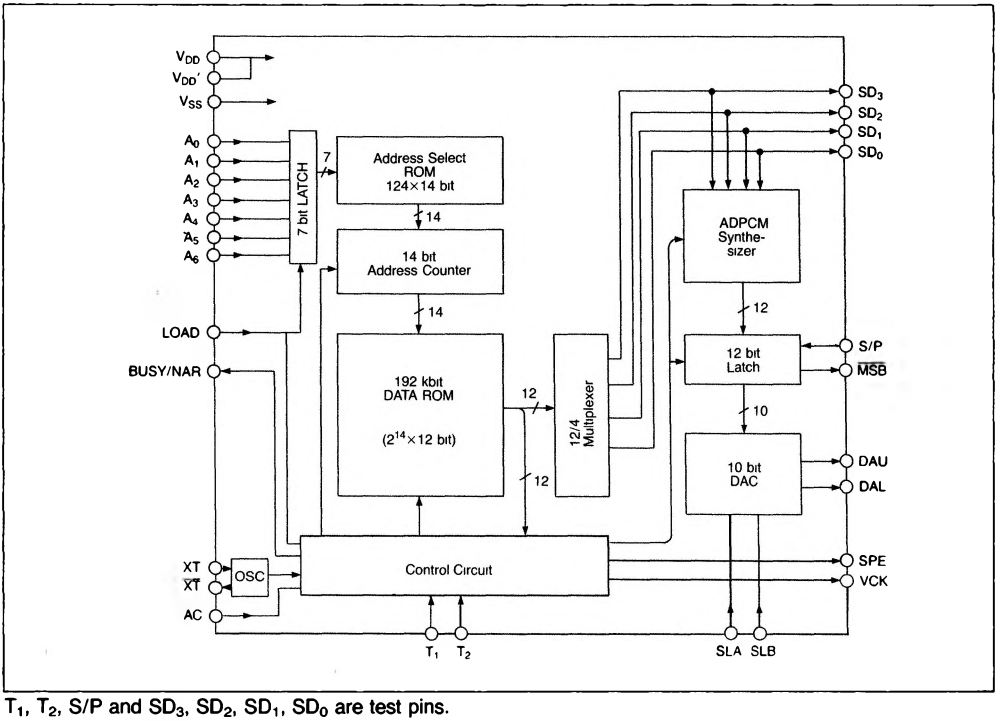
GENERAL DESCRIPTION

The Oki MSM6243 is a single-chip, CMOS, speech synthesis LSI for ADPCM systems. It contains 192k bits of speech data ROM storage. This IC has an input interface, a timing generation circuit, and a 10 bit DA converter. Therefore, voice output systems may be constructed easily by connecting the voice output circuit consisting of a simple input circuit, filter, amplifier, and speaker to the chip.

FEATURES

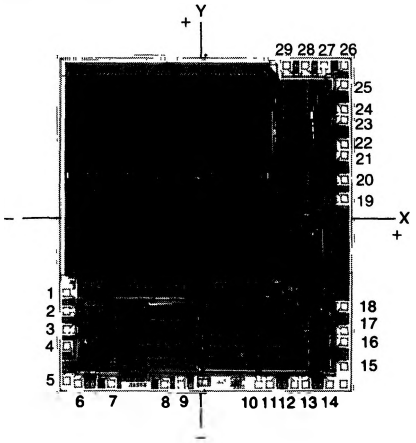
- CMOS single chip
- Low power consumption
- Custom ROM
- Selection of supply voltage: 3V system or 5V system.
- ADPCM bit length: 4 bits
- Maximum word number: 124 words
- Maximum speaking time: 20 seconds (compressed ADPCM)
- Selection of class A or class B analogue output is possible.
- Built-in 10 bit DA converter
- Oscillator frequency: 30 to 132 kHz (5V system).
- Chip, 40 pins plastic DIP, 44 pins or 60 pins plastic flat package. 2 types of plastic flat package are provided depending on terminal pin bending or not bending.
  - Terminal pin not bending
    - MSM6243-XXGS
  - Terminal pin bending
    - MSM6243-XXGS-K
  - When placing an order, specify the type.
- Word selection through an internal random number circuit is possible (maximum 32 words).

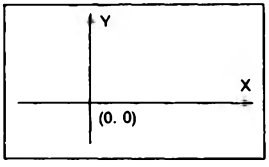
BLOCK DIAGRAM



T_1, T_2, S/P and SD_3, SD_2, SD_1, SD_0 are test pins.

PAD LAYOUT





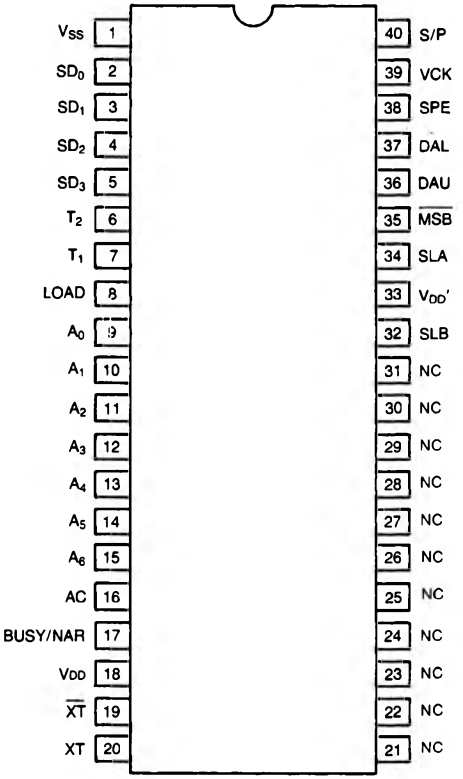
Note: • Chip size: 4.91 mm × 5.57 mm
• Chip thickness: 350 ± 30 µm

PAD LOCATION

Pad No.	Symbol	Position	
		X	Y
1	SLB	−2300	−1125
2	V_{DD}'	−2300	−1425
3	SLA	−2300	−1725
4	$\overline{MSB}$	−2300	−2000
5	DAU	−2300	−2570
6	DAL	−2110	−2615
7	SPE	−1560	−2615
8	VCK	−675	−2625
9	S/P	−395	−2625
10	V_{SS}	885	−2625
11	SD_0	1075	−2625
12	SD_1	1480	−2625
13	SD_2	1660	−2625
14	SD_3	2060	−2625
15	T_2	2295	−2325
16	T_1	2295	−1925
17	LOAD	2295	−1745
18	A_0	2295	−1345
19	A_1	2295	440
20	A_2	2295	745
21	A_3	2295	1145
22	A_4	2295	1325
23	A_5	2295	1730
24	A_6	2295	1910
25	AC	2295	2310
26	BUSY/NAR	2295	2625
27	V_{DD}	1965	2625
28	$\overline{XT}$	1650	2625
29	XT	1345	2625

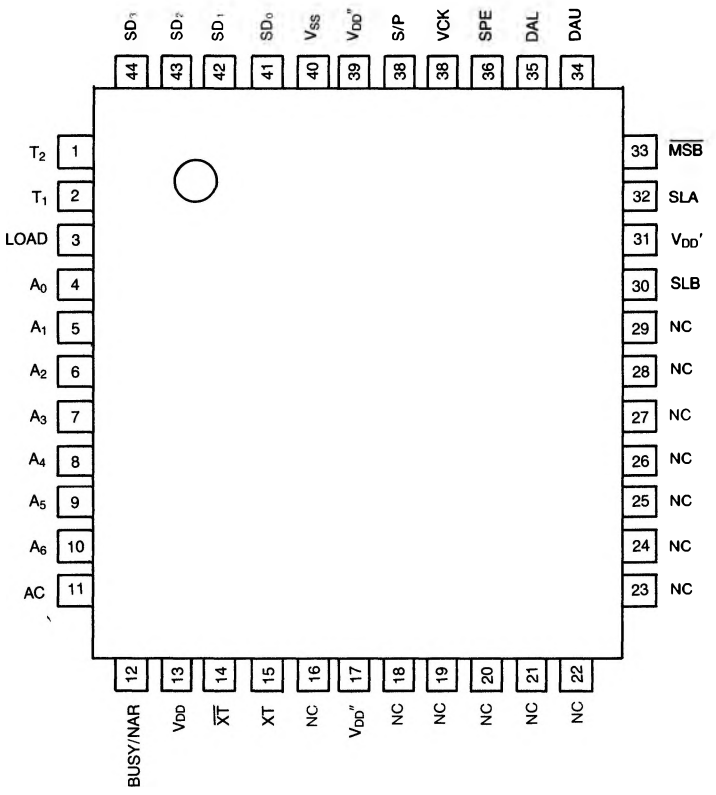
PIN CONFIGURATION

(Top View) 40 Lead Plastic DIP



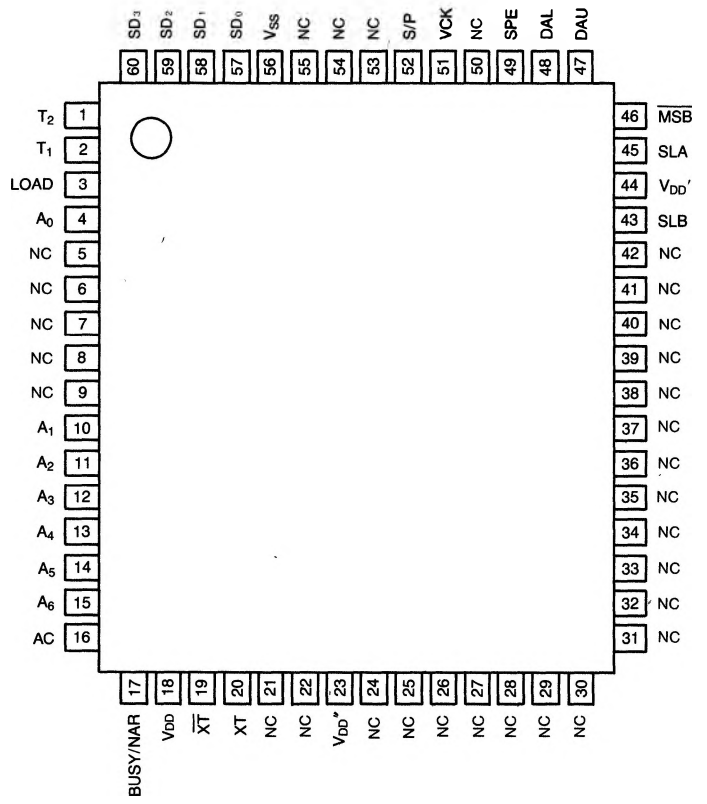
Note: This pinout applies to the MSM6243-XXRS.

(Top View) 44 Lead Plastic Flat Package



Note 1. This pinout applies to the MSM6243-XXGS and -XXGS-K.
Note 2. Since 17 and 39 pin (V_{DD}") is substrate continuity, short-circuits with V_{DD} and V_{DD}' in the outside.

(Top View) 60 Load Plastic Flat Package



Note 1. This pinout applies to the MSM6243-XXGS and -XXGS-K.
Note 2. Connect pin 23 (V_{DD}'') with V_{DD} and V_{DD}' externally. This pin is conducted to the substrate.

ELECTRICAL CHARACTERISTICS

3V System (V_{DD} = 3.1V TYP)

- **Absolute maximum rating**

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ +5.0	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Storage Temperature	T_{stg}	—	−55 ~ +150	°C

- **Operating range**

(V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	—	+2.4 ~ 3.6	V
Operating Temperature	T_{op}	—	−10 ~ +60	°C
DAU, DAL Output Level	V_{DD}	No-load	0 ~ V_{DD}	V

- **DC characteristics**

(V_{DD} = 3.1V, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.6	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Input Current*1	I_{IH1}	V_{IH} = 3.1V	—	0.01	0.5	μA
"H" Input Current*2	I_{IH2}	V_{IH} = 3.1V	10	—	150	μA
"L" Input Current	I_{IL}	V_{IL} = 0V	—	−0.01	−0.5	μA
"H" Output Current	I_{OH}	V_{OH} = 2.7V	−200	—	—	μA
"L" Output Current	I_{OL}	V_{OL} = 0.4V	200	—	—	μA
Operating Power Consumption	I_{DD1}	—	—	0.1	0.5	mA
Standby Power Consumption	I_{DD2}	Class B output selection and oscillation stop.	—	0.01	0.5	μA
Power Consumption*3 in the case of oscillation	I_{DD3}	Standby and class B output selection.	—	4	30	μA
DA Output Precision	$\lvert V_E \rvert$	No-load and class A output selection.	—	—	100	mV
DA Output Impedance	V_{OR}	—	—	50	—	kΩ

Notes:

*1. This applies to the AC, LOAD and A_0 to A_6 pins.

*2. This applies to the input pin except AC, LOAD and A_0 to A_6 pins.
For SLA, and SLB pins, this applies in the case of AC input "H". (In the case of AC input "L", this conforms to Note 1.)

*3. This applies when R_{FB} exists and f_{OSC} = 32.768 kHz.

5V System (V_{DD} = 5.0V TYP)

- **Absolute maximum rating** (V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7.0	V
Input Voltage	V_I		−0.3 ~ V_{DD}	V
Storage Temperature	T_{stg}	—	−55 ~ +150	°C

- **Operating range** (V_{SS} = 0V)

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{DD}	—	+4.5 ~ +5.5	V
Operating Temperature	T_{OP}	—	−30 ~ +70	°C
DAU, DAL Output Level	V_{OD}	No-load	0 ~ V_{DD}	V

- **DC characteristics** (V_{DD} = 3.1V, V_{SS} = 0V, Ta = −30~+70°)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Input Current*1	I_{IH1}	V_{IH} = 5.0V	—	—	1	μA
"H" Input Current*2	I_{IH2}	V_{IH} = 5.0V	20	—	400	μA
"L" Input Current	I_{IL}	V_{IL} = 0V	—	—	−1	μA
"H" Output Current	I_{OH}	V_{OH} = 4.6V	−1	—	—	mA
"L" Output Current	I_{OL}	V_{OL} = 0.4V	1	—	—	mA
Operating Power Consumption	I_{DD1}	—		0.2	0.7	mA
Standby Power Consumption	I_{DD2}	Class B output selection and oscillation stop.	—	0.01	10	μA
Power Consumption*3 in the case of oscillation	I_{DD3}	Standby and class B output selection.	—	15	100	μA
DA Output Precision	$\|V_E\|$	No-load and class A output selection	—	—	130	mV
DA Output Impedance	V_{OR}	—	—	60	—	kΩ

Notes:

*1. This applies to the AC, LOAD and A_0 to A_6 pins.

*2. This applies to the input pin except AC, LOAD and A_0 to A_6 pins.
For the pins of SLA and SLB, this applies in the case of AC input "H". (In the case of AC input "L", this conforms to Note 1.)

*3. This applies when R_{FB} exists and f_{OSC} = 32.768 kHz.

AC CHARACTERISTICS

(V_{DD} = +2.4 to +5.5V are common for 3V system and 5V systems.
Ta = −30 to +70°C, f_{osc} = 32.768 kHz.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillator frequency (1)	f_{OSC1}	3V system	30	32.768	35	kHz
Oscillator frequency (2)	f_{OSC2}	5V system	30	32.768	120	kHz
Oscillator duty-cycle	f_{duty}	—	40	50	60	%
LOAD input*1 pulse width	t_L	In the case of f_{sample} = 8.19 kHz and CPU interface	1	—	40	μS
AC input pulse width	$t_{W(AC)}$	—	1	—	—	μS
Sampling frequency (1)	f_{S1}	$f_{OSC}/4$	—	8.192	—	kHz
Sampling frequency (2)	f_{S2}	$f_{OSC}/5$	—	6.554	—	kHz
Sampling frequency (3)	f_{S3}	$f_{OSC}/8$	—	4.096	—	kHz
NAR minimum "H" level width	t_{MN}	In the case of f_{S1} selection	1	—	—	μS
Hold time for LOAD	t_H	In the case of f_{S1} selection	1	—	—	μS

*1. $t_{L(MAX)}$ in the case of SW input interface is equal to the speaking time of a specified word.

PIN DESCRIPTION

Pin Name	Terminal Number				I/O
	CHIP	40 DIP	44 FLT	60 FLT	
AC	25	16	11	16	I

All clear
LSI comes to standby state by "H" input, and SLA and SLB pins are pulled down to "L" level. Since this pin is started by LOAD input, pulse input can be used.
In this LSI, since power on clear circuit is not built-in, apply AC pulse when power is turned on.

A_0	18	9	4	5	I
A_1	19	10	5	10	I
A_2	20	11	6	11	I
A_3	21	12	7	12	I
A_4	22	13	8	13	I
A_5	23	14	9	14	I
A_6	24	15	10	15	I

Address
These pins are used to specify the speaking word code.
Speaking word code is latched into inside by the LOAD pulse rise.

LOAD	17	8	3	3	I

Speaking word code is latched into inside by the LOAD pulse rise.
When the system is reset by previously applied AC signal, the system reset is cancelled in the case of LOAD pulse rise, and LSI is started. And when NAR output mentioned later is in the "H" level, LOAD signal comes to effective.

BUSY/NAR	26	17	12	17	O

Next address request
BUSY/NAR can be switched in an LSI, and an either of them may be specified on the occasion of order. In the case of NAR use, LOAD input comes to effective with "H" level, and in the case of BUSY use, LOAD input comes to effective with "L" level.

XT	29	20	15	20	I

Crystal
This is crystal input pin for internal clock oscillation.
This also becomes input pin when an external clock is used.

$\overline{XT}$	28	19	14	19	I

This is crystal input pin for internal clock oscillation.

DAU	5	36	34	47	O
DAL	6	37	35	48	O

DA upper, DA lower
The output of 10 bits DA converter is connected to these pins directly. Since output impedance of these pins are great and LPF is not built in, connect the LPF through a low impedance output buffer outside. In the selection of class A mode, output pin is only DAU.

PIN DESCRIPTION (Continued)

Pin Name	Terminal Number				I/O
	CHIP	40 DIP	44 FLT	60 FLT	
SLA	3	34	32	45	I
SLB	1	32	30	43	I

Selecter A, selecter B
Switchover of DA converter output condition to class A mode or class B mode.

SLA	SLB	Mode	Output Pin
Open (L)	Open (L)	Class B × 2	DAU, DAL
V_{DD} (H)	Open (L)	Class B × 1	Same as above
Open (L)	V_{DD} (H)	Class B × 4	Same as above
V_{DD} (H)	V_{DD} (H)	Class A	DAU

$\overline{MSB}$	4	35	33	46	I/O

In the case of class B mode, this pin becomes as follows:
- In the case of MSB = "L" output, DAU output is effective.
- In the case of MSB = "H" output, DAL output is effective.

In the case of class A mode, this pin becomes as follows:
- In the case of MSB = "L" output, DAU output value is $V_{DD}/2$ or more.
- In the case of MSB = "H" output, DAU output value becomes $V_{DD}/2$ or less.

In the case of internal circuit test, this pin is used as input pin.

SPE	7	38	36	49	I/O

Speaker enable
In the case of "H" level output, DA output is effective. In the case of internal circuit test, this pin is used as input pin.

VCK	8	39	38	51	O

Voice clock
Sampling frequency is output through this pin.

SD_0	11	2	41	57	I/O
SD_1	12	3	42	58	I/O
SD_2	13	4	43	59	I/O
SD_3	14	5	44	60	I/O

These pins are used for internal circuit test. These pins carry out I/O of 4 bits ADPCM data. Usually, set them to open.

S/P	9	40	38	52	I

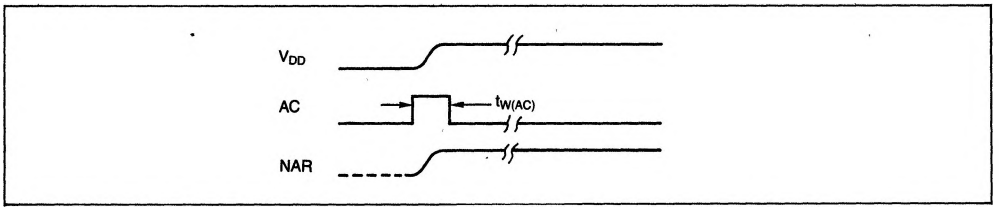
Serial/parallel
These pins are used for internal circuit test. Usually, set them to GND level.

T_1	16	7	2	2	I
T_2	15	6	1	1	

Test
These pins are used for internal circuit test. Usually, set them to GND level

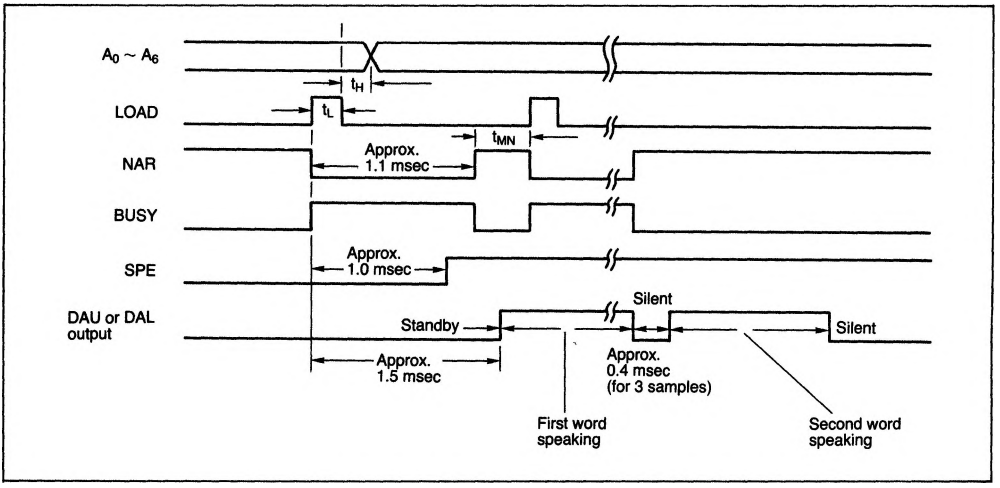
TIMING CHART

Power On

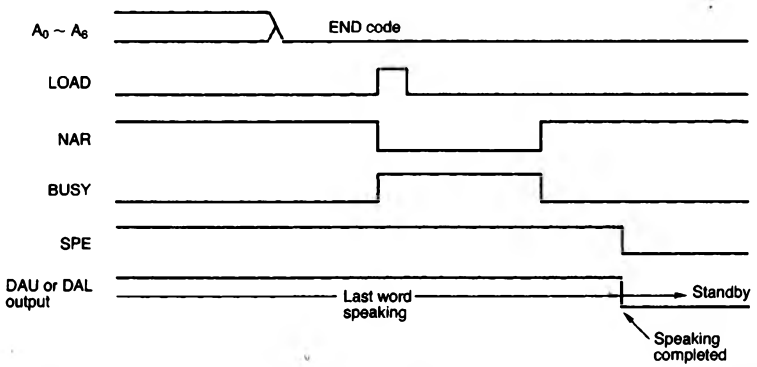


LSI Start and No Operation (Standby)

1. Start in the case of CPU interface



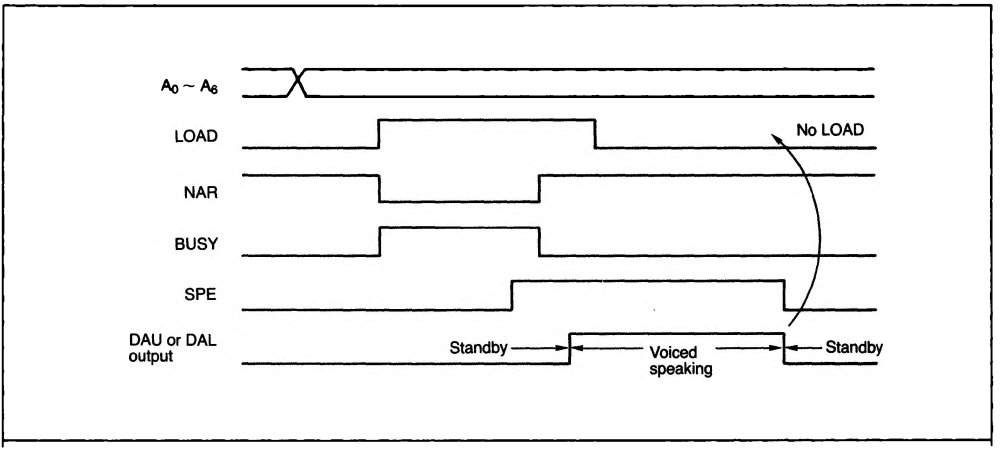
2. Transfer to standby in the case of CPU interface



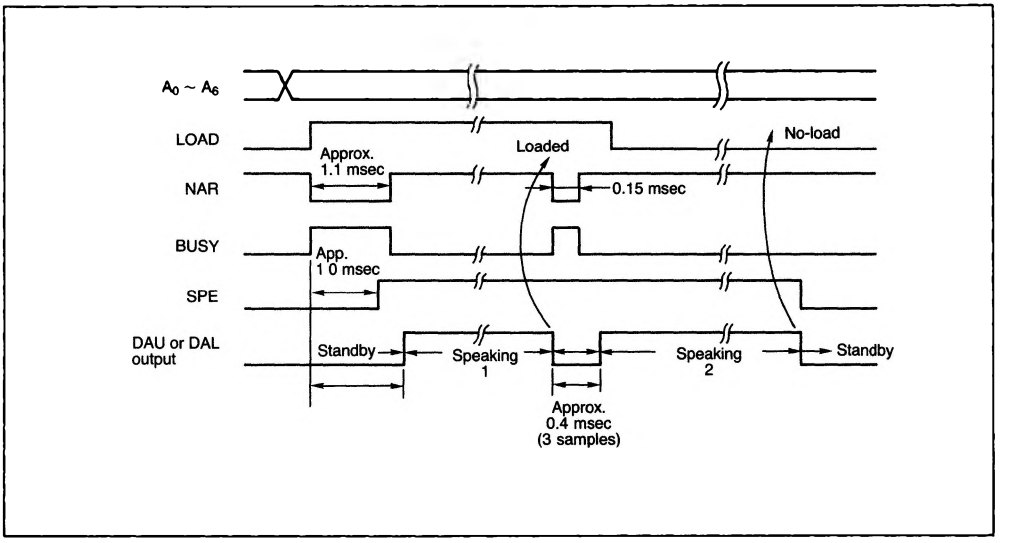
When END code (A_0 to A_6 = "L") is accompanied with LOAD, LSI comes to the same state as standby because of AC input.

Start of SW input interface and standby

1. Single word speaking



2. Repetition of word speaking



FUNCTIONAL DESCRIPTION

Speaking Word Code Specification
User can specify word codes set by $A_0 \sim A_6$ and can select either CPU interface or SW input interface.

1. CPU Interface
In this case, user specified words are maximum 124 words. For A_0 to A_6, the following 3 codes, "1111111", "0111111", "1011111", are test codes, and the code "0000000" is an END code, therefore, these 4 codes can not be used.

The procedure up to the LSI operation start is as follows:
Input A_0 to $A_6 \rightarrow$ LOAD pulse apply $\rightarrow$ latched inside, also LSI operation starts simultaneously.

LOAD pulse is effective when NAR output is "H".

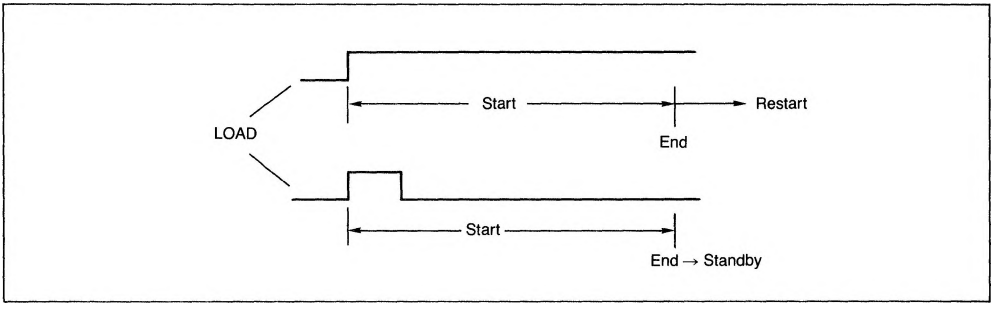
2. SW Input Interface
By the reason described in clause 9.1.1. CPU interface, number of words is set to maximum 124 words with combination of A_0 to A_6.

After the code is set by A_0 to A_6, when "H" level LOAD input is switched by push switch, etc., the specified word starts speaking. (From standby to operation state).

When speaking of the specified word is completed, if the LOAD input is set being "H" as it is, repeat speaking of the same word, and if the LOAD input turns to "L", LSI moves to standby state automatically.

Therefore, for example, so far the push switch is being pushed as it is, speaking of the same word is repeated. When the push switch is released, the repetition is stopped at the same time of the speaking ends.

To make speaking of different words continuously, change the codes of A_0 to A_6 before the first word speaking comes to end, and keep the LOAD in "H" state.



Sampling Frequency Specification
An user can specify available sampling frequency for each word when ordering.

Relation between sampling frequency and oscillator frequency is as follows:

In the case of $f_{(OSC)} = 32.768$ kHz

Selection 1. $\dfrac{32.768 \text{ kHz}}{4} \fallingdotseq 8.2$ kHz

Selection 2. $\dfrac{32.768 \text{ kHz}}{5} \fallingdotseq 6.55$ kHz

Selection 3. $\dfrac{32.768 \text{ kHz}}{8} \fallingdotseq 4.1$ kHz

Straight ADPCM and Compressed ADPCM

1. Straight ADPCM

Features of the straight ADPCM are as follows:

1) ADPCM bit length ..... Fixed in 4 bits.
2) Deletion of silent component is possible.
3) High bit rate, high tone quality.
4) Suitable for a sound effect

Bit rate (B·R) example:

f_{SAMPLE} = 8.2 kHz
ADPCM bit length = 4 bits
Deleted silent data ≒ 1/5 (voice)
B·R ≒ 8.2×4×4/5 ≒ 26.3 kbits/sec

2. Compressed ADPCM

Features of the compressed ADPCM are as follows:

1) ADPCM bit length ..... Fixed in 4 bits
2) Deletion of data by repeated detection of speech waveform.
3) Deletion of silent component is possible.
4) Low bit rate
5) Mainly applies to speech.

Bit rate example:

f_{SAMPLE} = 8.2 kHz
ADPCM bit length = 4 bits
Number of average waveform repetition = 3 (deleted data = 2/3)
Deleted silent data ≒ 1/5
B·R ≒ 8.2×4×1/3×4/5 ≒ 8.8 kbits/sec

Sampling Frequency and Band

1. Simple relation between sampling frequency and band

$f_{SAMPLE} \times 1/2 = f_{BAND(UL)}$

Here, $f_{BAND(UL)}$ means upper limit of the band.

f_{SAMPLE}	f_{BAND}	Characteristics
8.2 kHz	DC ~ 4.1 kHz	Clear comprehending almost all tones of voice.
6.55 kHz	DC ~ 3.2 kHz	High tone female voice sounds usual.
4.1 kHz	DC ~ 2.0 kHz	Both male and female voices sound nasal and unclear.

2. Relation between sampling frequency and LPF (Low Pass Filter) is as follows:

$f_{SAMPLE} \times 1/2 = f_C$ (cut-off frequency of ideal filter)

Practically, according to the skirt characteristics of filter, f_C shall be designed to be lower than the above mentioned equation. That is, the band will be further narrowed according to filter characteristics.

As an example, the f_C and skirt characteristics of filter used for speech analysis by OKI are shown as follows.

f_{SAMPLE}	f_C	Skirt character	f_{BAND}
8.2 kHz	3.4 kHz	−48 dB/oct	Dc ~ 3.4 kHz
5.55 kHz	2.7 kHz	−48 dB/oct	DC ~ 2.7 kHz
4.1 kHz	1.7 kHz	−48 dB/oct	DC ~ 1.7 kHz

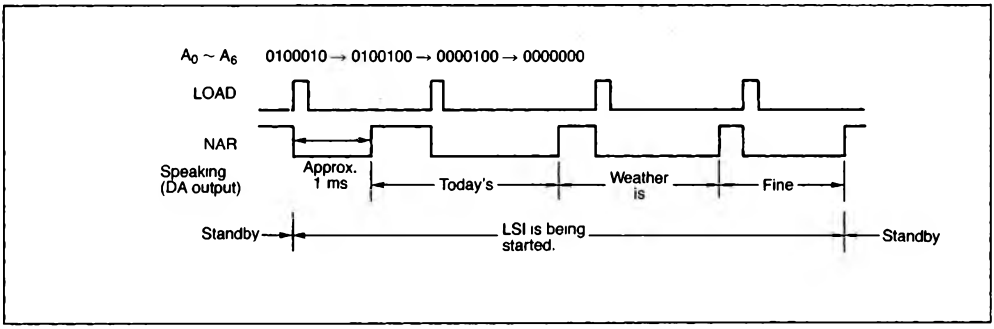
Precautions in Use

1. Relation between LOAD and NAR

A LOAD pulse input is effective when NAR output is "H" state, and at the LOAD pulse rise NAR output transfers to "L" state which will be held till the completion of the former word speaking.

Therefore, use of NAR output is capable of speaking smoothly of the sentence composed of some words.

Example:	"Today's"	"Weather is"	"Fine"	"END"
Corresponding codes by A_0 to A_6	0100010	0100100	0000100	0000000



2. Internal random number circuit

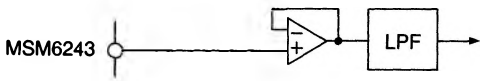
Use of internal random number circuit may be specified on the occasion of order, but the specification prohibits external code input by $A_0 \sim A_6$ and maximum word number is limited to 32 words.

3. Analog output (DAU, DAL)

The output of 10 bits DA converter is connected to DAU and DAL pins directly.

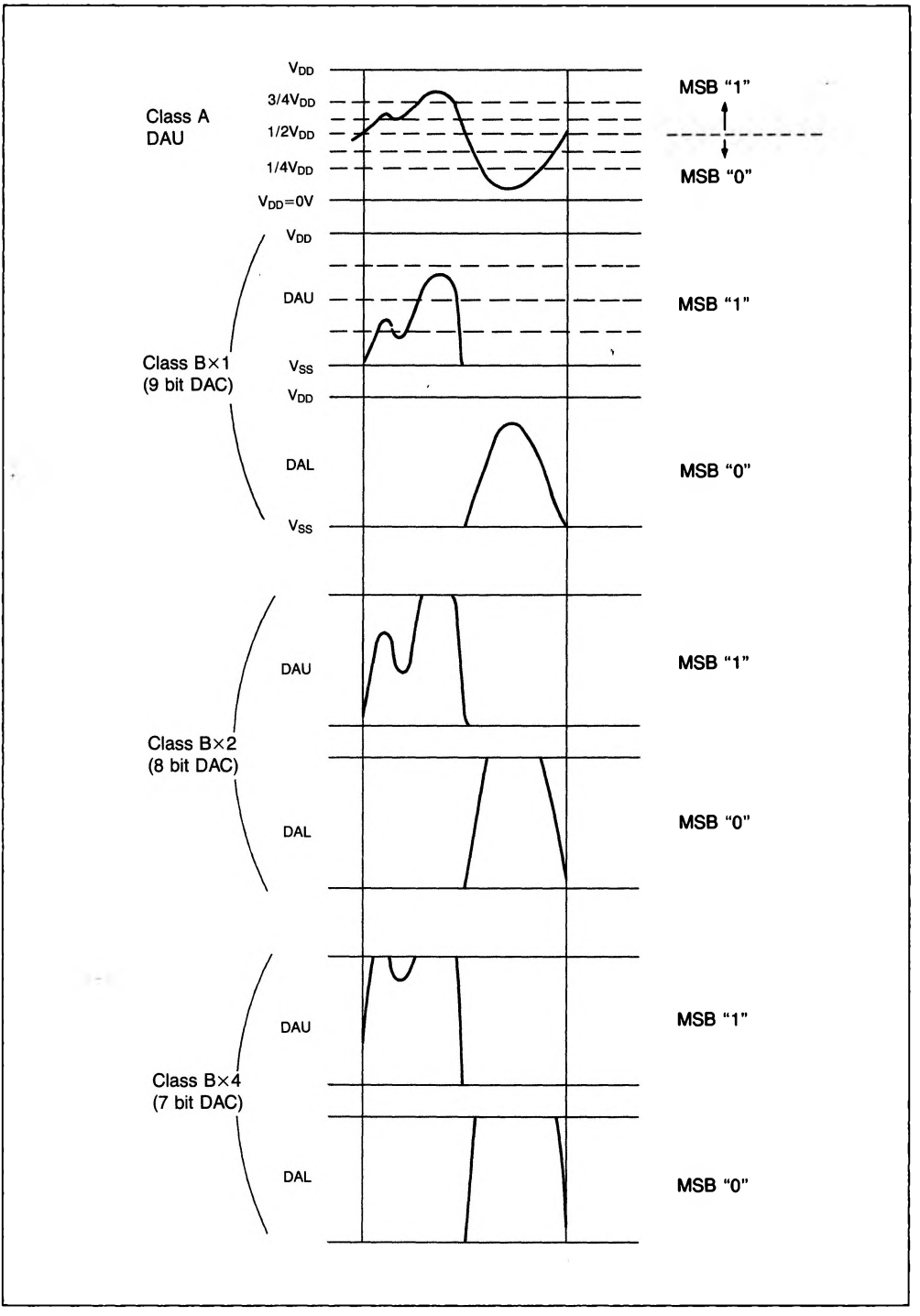
Since this output impedance is great and LPF is not built-in, it is necessary to connect outside LPF through the low impedance output buffer.

Circuit example:



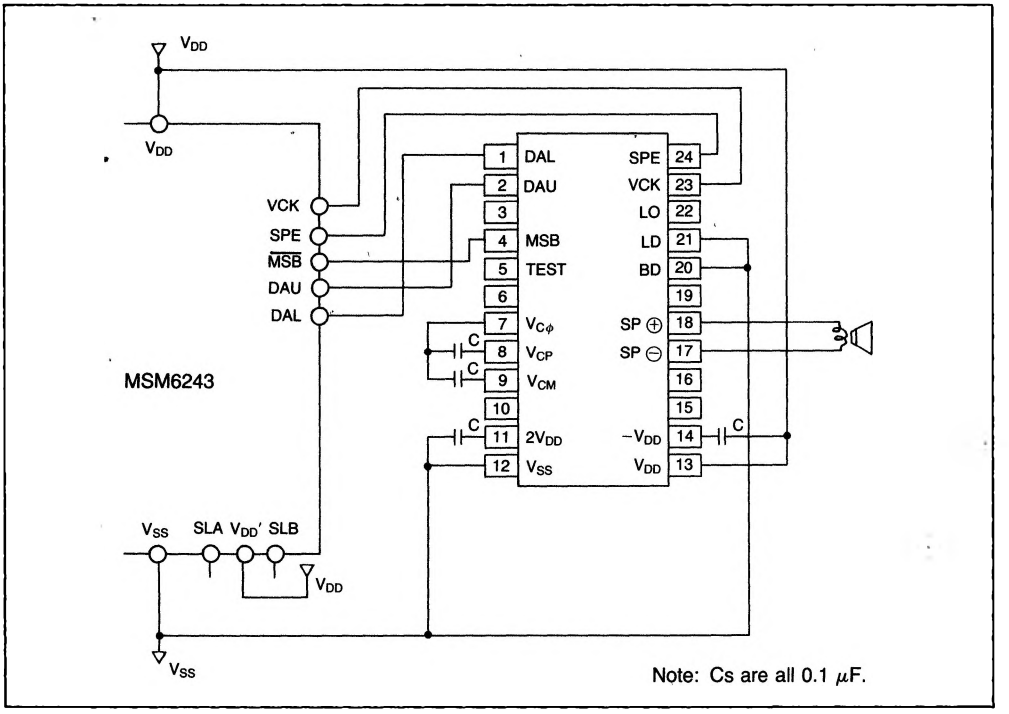
For output status, the following modes of class A and class B are obtained by 2 pins of SLA and SLB.

SLA	SLB	Mode	Output pin
Open (L)	Open (L)	Class B×2	DAU, DAL
V_{DD} (H)	Open (L)	Class B×1	Same as above
Open (L)	V_{DD} (H)	Class B×4	Same as above
V_{DD} (H)	V_{DD} (H)	Class A	DAU

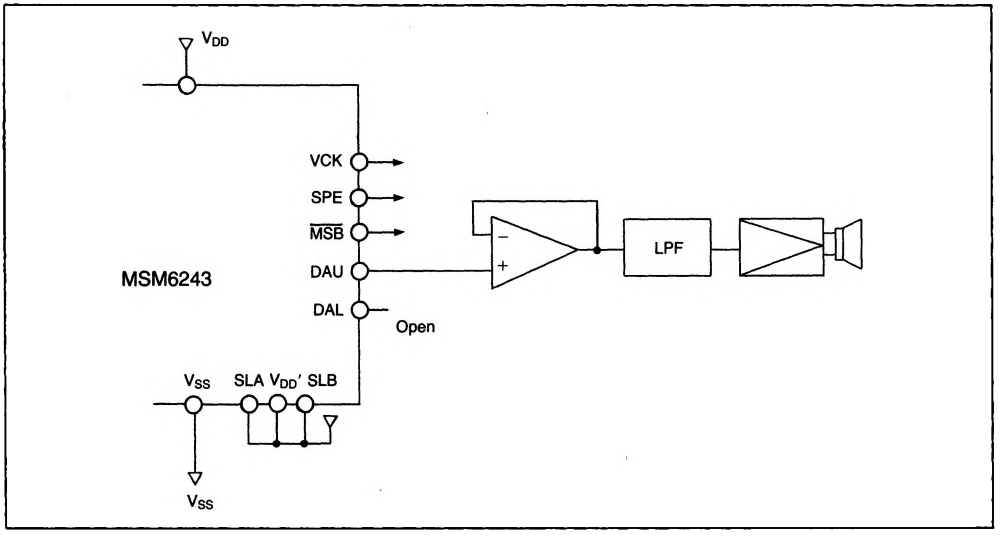

Class A
DAU
V_{DD}
3/4V_{DD}
1/2V_{DD}
1/4V_{DD}
V_{DD}=0V
MSB "1"
MSB "0"
Class B×1
(9 bit DAC)
V_{DD}
DAU
V_{SS}
V_{DD}
DAL
V_{SS}
MSB "1"
MSB "0"
Class B×2
(8 bit DAC)
DAU
DAL
MSB "1"
MSB "0"
Class B×4
(7 bit DAC)
DAU
DAL
MSB "1"
MSB "0"

EXAMPLE OF OUTPUT INTERFACE

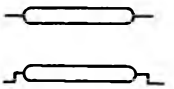
- In the case of class B use, output interface is connected with MSC1161GS (provided, for only 3V system)



- Output of class A



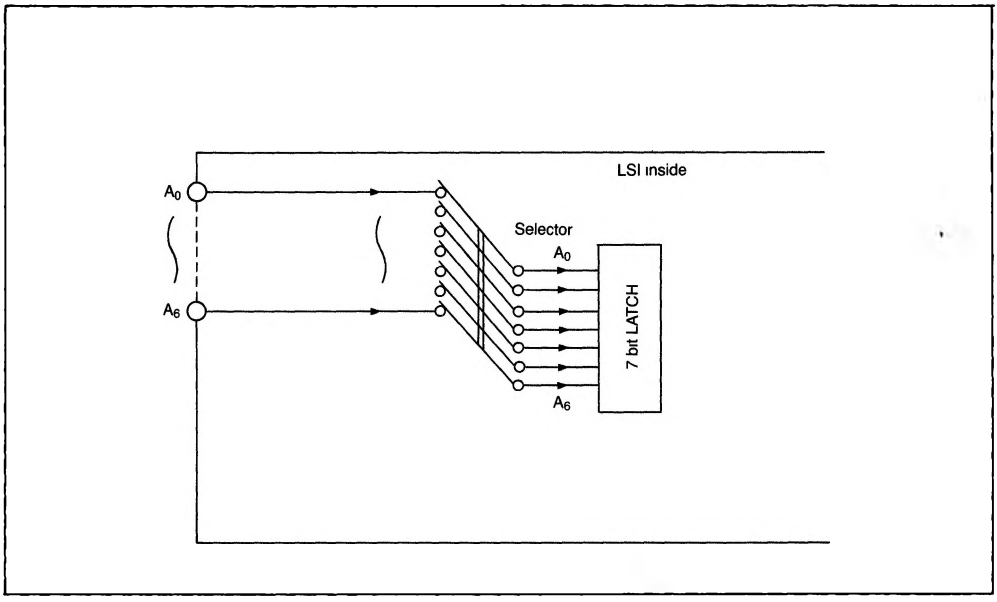
USER SPECIFIED PARAMETER

No.	Item	User specification				Remarks
1	Shipping form	Chip	DIP (40 pin)	Flat (60 pin) GS	Flat (60 pin) GS-K	Pin without bending for GS Pin bending for GS-K  Package side view
2	Supply voltage	3V system (2.4 ~ 3.6V)		5V system (4.5 ~ 5.5V)		
3	Operational temperature	___°C ~ ___°C				
4	Interface condition	SW input interface		CPU input interface		
5	BUSY/NAR	BUSY		NAR		
6	Word code input	External		Internal random number		Refer to circuit 1.
7	Oscillator	32.768 kHz		Other than 32.768 kHz		In the case other than 32.768 kHz, specify the oscillator frequency in the range of 30 to 132 kHz.
8	Sampling frequency	8.2 kHz (1/4)	6.55 kHz (1/5)	4.1 kHz (1/8)		When oscillator frequency is other than 32.768 kHz, specify dividing ratio within a parenthesis.
9	R_{FB} of internal oscillation circuit	Exists		Not exists		Exists → Connect the resonator to XT and XT. Not exists → Apply external clock to TX. Refer to circuit 2.
10	Specification of correspondence between speaking word and word code (A_0 to A_6)	Specify		Not specify		When specified, attach corresponsing table with this paper When not specified, OKI decides it.
11	Editing of speaking words	Editing		No editing		In the case of editing, attach an example sentence with this paper. Ex. 3 o'clock 10 minutes

Note 1. For parameters of No. 4, 5, 6, 8, 9, 10, and 11, corresponds with ROM mask.

Note 2. When an user creates a voice data, never write the voice data in 256 words×126 bits (3 kbits) from the top.

Circuit 1. The following chart shows simple circuit when the word is specified.



Circuit 2. The following charts show the interface examples for XT and $\overline{XT}$.