OKI semiconductor

MSM58421

CMOS 4-BIT SINGLE CHIP MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

The OKI MSM58421 is a low-power, high-performance 4-bit single-chip microcontroller implemented in complementary metal oxide semiconductor technology.

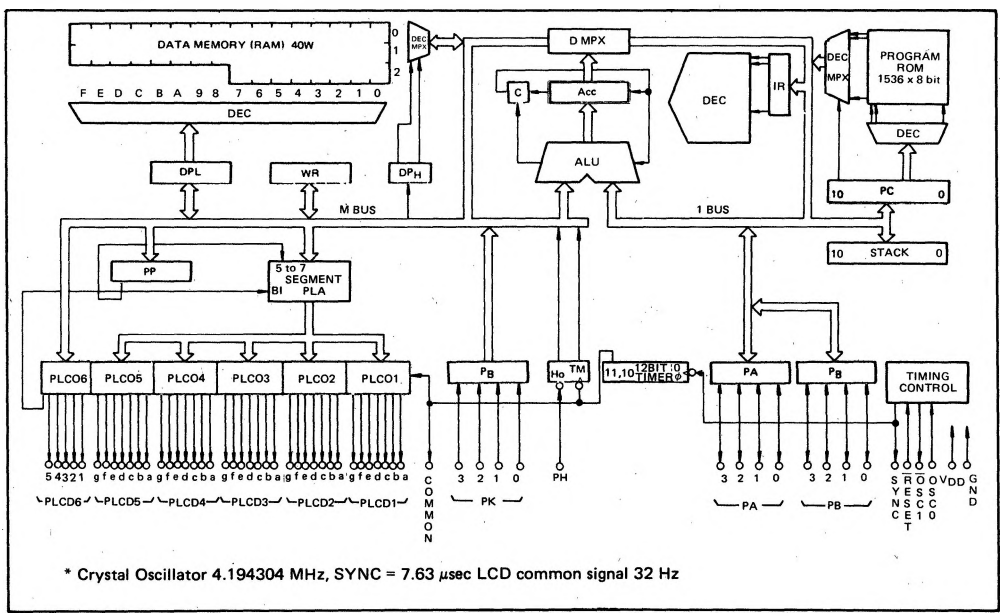
Integrated within this one chip is a 5 digit 7-segment LCD driver and PLA which can change the character font for the 7 segments freely under the control of the mask programmable data.

Also integrated in this chip are mask ROM of 1536 × 8 bits for programming, data RAM of 40 × 4 bits, 13 general-purpose input/output ports, 12-bit timer, and clock oscillator to facilitate easy application to equipment with an LCD display.

FEATURES

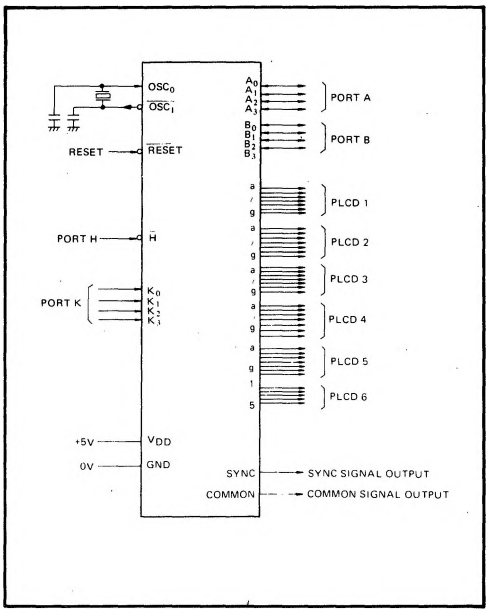
- Low Power Consumption CMOS 4-bit One-Chip Microcomputer
- 100% Static Logic
- 1536 × 8 bits Mask ROM
- 40 × 4 bits Data RAM
- 1 Static Register
- Built-in 12-bit Timer (with 32 Hz Common Output)
- All Input Ports Contain Schmitt Trigger Circuits
- 8-bit Interface Bus
- 52 Instructions
- 94% of the 52 Instructions are 1 Byte and 1 Machine Cycle
- Integrated with 13 Input/Output Ports and 40 Static LCD Driver Circuit
- +5V Single Power Supply, 60-Pin Mold Flat Package
- 7-Segment Character User Programmable Font (32 Words × 7 Segments)
- Various Functions Changeable under Mask Program Control

FUNCTIONAL BLOCK DIAGRAM

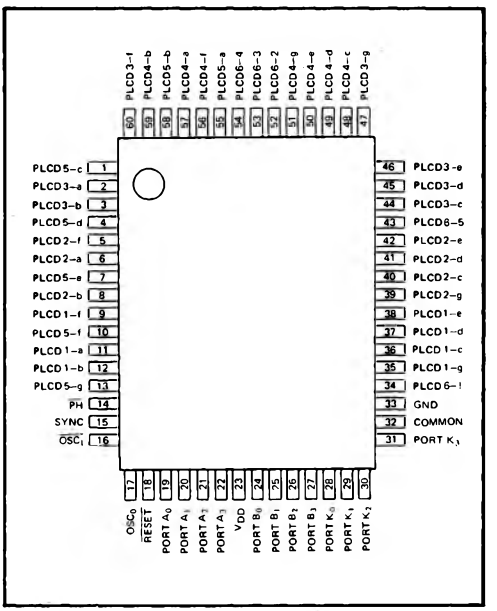


* Crystal Oscillator 4.194304 MHz, SYNC = 7.63 μsec LCD common signal 32 Hz

LOGIC SYMBOL



PIN CONFIGURATION



PIN DESCRIPTION

Designation	Pin No.	Function
GND	33	Circuit GND potential
V_{DD}	23	Main power source (+5V)
OSC_0	17	Crystal OSC input, external clock input
$\overline{OSC_1}$	16	Crystal OSC input, external clock output (not TTL compatible)
PA, PB	19 to 22 24 to 27	Pseudo-bidirectional ports for 4-bits parallel I/O. To input data from these ports, it is necessary to write "1" to them beforehand. When nothing is applied to their terminals, the content of output ports is written in them, so they can also be used as registers. In addition, it is possible to use them for make 8-bit parallel output depending on instructions.
PK	28 to 31	Input ports for 4-bit parallel input with no latching function.
PH	14	Input port with latching function to be set by negative logical signal. That is, this terminal is set at the time when the negative logical signal is applied to it from the outside. It is reset automatically after execution of the test instruction of this port.
$\overline{RESET}$	18	The RESET signal which input has priority over all of other signals and performs the following functions: (1) Resets all bits of the program counter; (2) Resets the timer counter and timer flag; (3) Resets the port pointer; (4) Resets the accumulator; (5) Resets I/O ports PA and PB; (6) Resets the input port PH flag; (7) Initializes the output port PLCD for LCD; (8) Resets the machine cycle to M_1. Since the $\overline{RESET}$ terminal is pulled up to V_{DD} by an internal resistor (approx. 800 kΩ), it is possible to make power ON/reset by connecting it with an external capacitor.

PIN DESCRIPTION (CONT.)

<table>
<tr><th>Designation</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>SYNC</td><td>15</td><td>General-purpose synchronizing signal output. The signal is output at the beginning of each machine cycle. Output constantly, this signal is used also as clock pulse to external units.
The cycle of SYNC becomes 32 times that of the original oscillation (8 μs when the clock pulse is 4 MHz).</td></tr>
<tr><td>PLCD
1 ~ 6</td><td>1 to 13
34 to 60</td><td>PLCD 1 ~ 6 (Pins 1 ~ 13 and 34 ~ 60)
7-bit and 5-bit parallel output ports, respectively. They are used to direct drive an LCD (static type). Specification of each port is done by the port pointer (PP) as shown in the table below:

<table>
<tr><th colspan="4">Content of PP</th><th rowspan="2">Port Specified</th></tr>
<tr><th>b_3</th><th>b_2</th><th>b_1</th><th>b_0</th></tr>
<tr><td>x</td><td>0</td><td>0</td><td>0</td><td>PLCD1</td></tr>
<tr><td>x</td><td>0</td><td>0</td><td>1</td><td>PLCD2</td></tr>
<tr><td>x</td><td>0</td><td>1</td><td>0</td><td>PLCD3</td></tr>
<tr><td>x</td><td>0</td><td>1</td><td>1</td><td>PLCD4</td></tr>
<tr><td>x</td><td>1</td><td>0</td><td>0</td><td>PLCD5</td></tr>
<tr><td>x</td><td>1</td><td>0</td><td>1</td><td>PLCD6 1 ~ 4</td></tr>
<tr><td>x</td><td>1</td><td>1</td><td>0</td><td>PLCD6 5 and BI</td></tr>
<tr><td>x</td><td>1</td><td>1</td><td>1</td><td>——</td></tr>
</table>

X: Don't care
BI: 7 Segment Decoder PLA Blank Input
The data of b_0, of the internal 4-bit bus is written to 5 of PLCD6, and that of b_3 to BI.</td></tr>
<tr><td>COMMON</td><td>32</td><td>COMMON (Pin 32)
COMMON output terminal. This output signal is connected to the common electrode of static type LCD. The frequency of the COMMON signal output is given with the following equation:
$f_{(COM)} = f_{(OSC)}/2^{17}$
Where the basic clock $f_{(OSC)}$ is 4.19304 MHz, $f_{(COM)}$ becomes 32 Hz (duty ratio: 50%).</td></tr>
</table>

MASK OPTION TABLE

f(osc)=4.194304MHz

No.	Port K0 28 pin	Port K2 30 pin	Port K3 31 pin	Commom 32 pin	Timer
0	K_0	K_2	K_3	32Hz	12 bit
1	K_0	BUZZER	$\overline{\text{COMMON}}$	32Hz	12 bit
2	K_0	BUZZER	K_3	32Hz	12 bit
3	K_0	BUZZER	K_3	64Hz	11 bit
4	K_0	K_2	K_3	64Hz	11 bit
5	K_0	K_2	K_3	128Hz	10 bit
6	K_0	BUZZER	K_3	128Hz	10 bit
7	K_0	K_2	K_3	256Hz	9 bit
8	K_0	K_2	K_3	512Hz	8 bit
9	K_0	BUZZER	K_3	512Hz	8 bit

f (BUZZER)=2048Hz

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3 to 7	V
Input Voltage	V_I	Ta = 25°C	−0.3 to V_{DD}	V
Power Dissipation	P_D	Ta = 25°C per 1 package	200	mW
Storage Temperature	T_{stg}		−55 to +150	°C

OPERATING RANGE

Parameter	Symbol	Conditions	Limits	Unit
Power Supply Voltage	V_{DD}	$f_{(OSC)}$ = 0 to 4.2 MHz	4 to 6	V
Operating Temperature	T_{OP}	–	−40 to +85	°C
Fan Out (excluding COM, SEC)	N	MOS Load	15	–
		TTL Load	1	

D.C. CHARACTERISTICS

(V_{DD} = 5V±10%, Ta = −40 to +85°C)

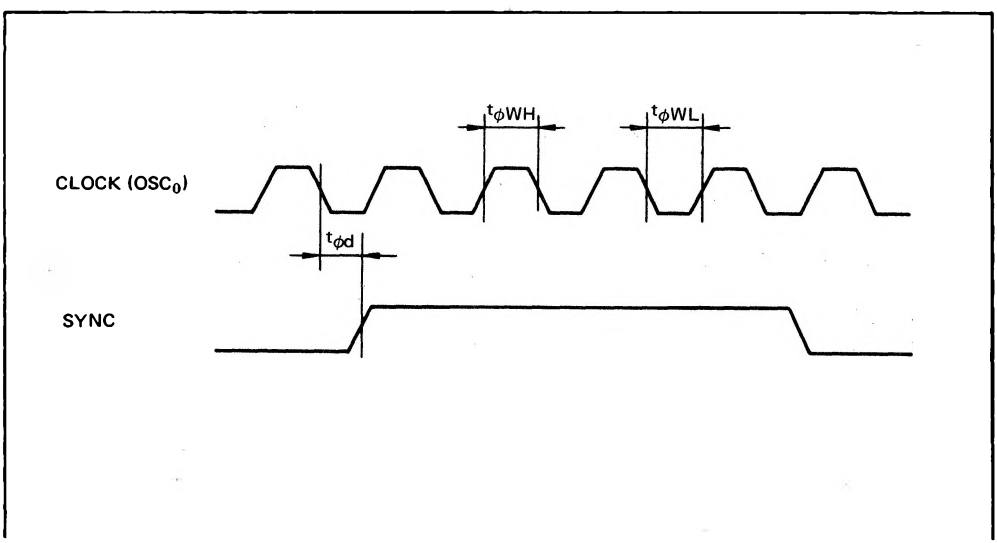
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}		3.6			V
"L" Input Voltage	V_{IL}				0.8	V
"H" Output Voltage(1)	V_{OH}	I_O = −80μA	V_{DD} −0.1			V
"H" Output Voltage(2)	V_{OH}	I_O = −20μA	V_{DD} −0.1			V
"H" Output Voltage(3)	V_{OH}	I_O = −40μA	4.2			V
"H" Output Voltage(4)	V_{OH}	I_O = −15μA	4.2			V
"L" Output Voltage(1)	V_{OL}	I_O = 80μA			0.1	V
"L" Output Voltage(2)	V_{OL}	I_O = 20μA			0.1	V
"L" Output Voltage(5)	V_{OL}	I_O = 1.6mA			0.4	V
OSC_O Input Leak Current	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I$ = 0V			10/−10	μA
Input Current(6)	I_{IH}/I_{IL}	$V_I = V_{DD}/V_I$ = 0V			1/−20	μA
PA PB "H" Output Current	I_{OH}	V_O = 0.4V			−1	mA
"H" Output Current(3)	I_{OH}	V_O = 2.5V	−0.25			mA
"L" Output Current(4)	I_{OL}	V_O = 0.4V	1.6			mA
Input Capacity	C_I	f=1MHz, Ta=25°C		5		pF
Output Capacity	C_O	f=1MHz, Ta=25°C		7		pF
Current Consumption	I_{DD}	f = 4.194304 MHz, at no load		2	5	mA

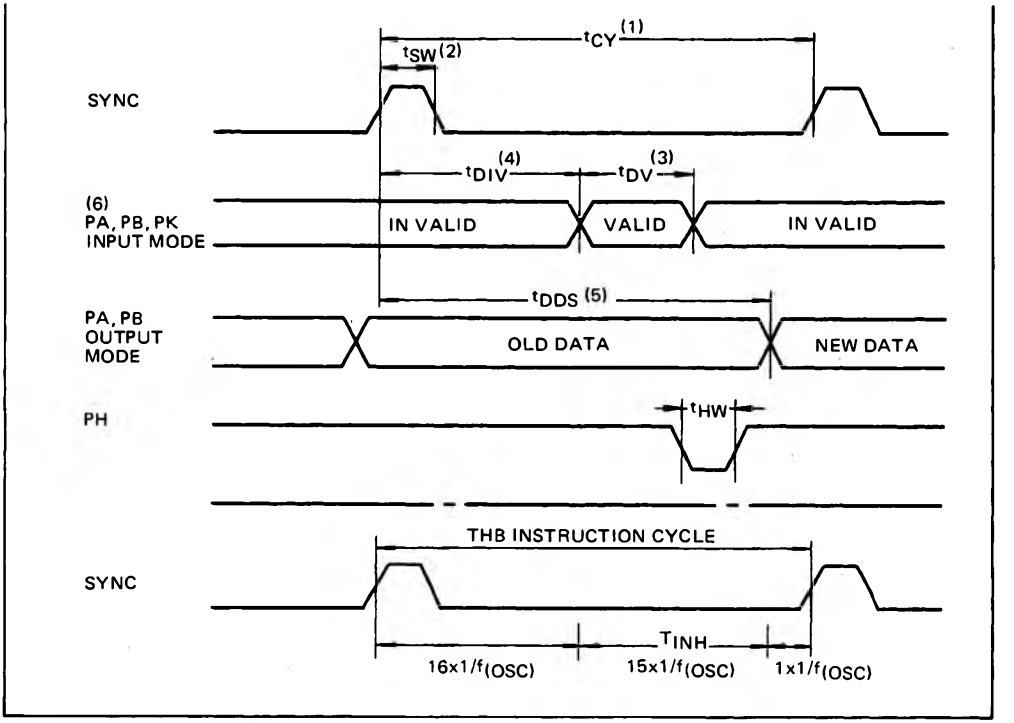
Notes: (1) Applied to COMMON
(2) Applied to SEGMENT
(3) Applied to SYNC
(4) Applied to PA, PB
(5) Applied to SYNC, PA, and PB
(6) Applied to $\overline{\text{RESET}}$, PK, and $\overline{\text{PH}}$

SWITCHING CHARACTERISTIC

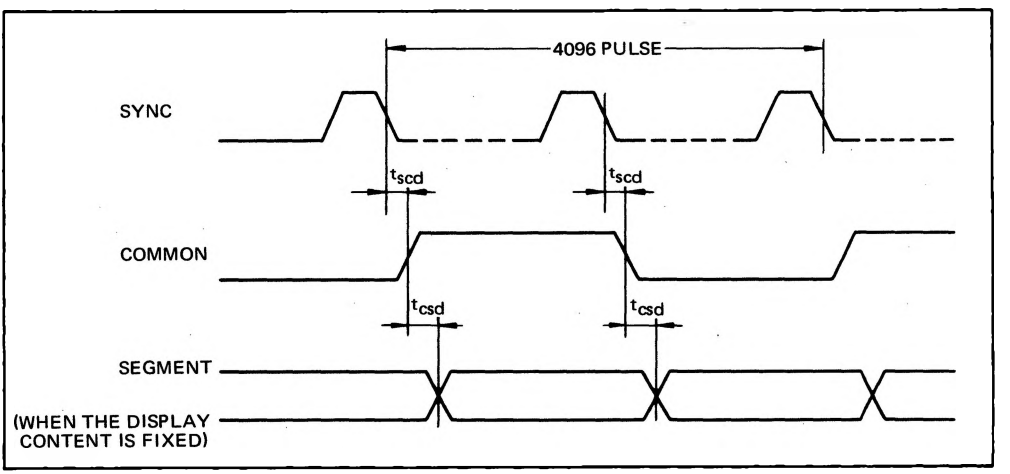
(V_{DD} = 5V±10%, Ta = −40° to +85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SYNC Delay Time from Clock (OSC_0)	$t_{\phi d}$	C_L = 50pF			800	ns
Clock (OSC_0) Pulse Width	$t_{\phi WH}$ $t_{\phi WL}$		115			ns
Cycle Time	t_{CY}		(1)			μs
SYNC Pulse Width	t_{SW}		(2)			μs
PA PB Data Valid Time PK	t_{DV}	C_L = 50pF	(3)			μs
PA PB Data Invalid Time PK	t_{DIV}	C_L = 50pF			(4)	μs
Data Delay Time	t_{DDS}	C_L = 50pF	500			ns
Port H Set Pulse Width(7)	t_{HW}		500			ns
COMMON Delay Time from SYNC	t_{SCd}	C_L = 50pF			2	μs
SEGMENT Delay Time from COMMON	t_{CSd}	C_L = 50pF			1	μs





Notes: (1) $t_{CY} = 32 \times 1/f_{(OSC)}$
(2) $t_{SW} = 4 \times 1/f_{(OSC)}$
(3) $t_{DV} = 8 \times 1/f_{(OSC)}$
(4) $t_{DIV} = 16 \times 1/f_{(OSC)} + 0.5\,\mu s$
(5) $t_{DDS} = 26 \times 1/f_{(OSC)} + 1\,\mu s$
(6) When data is input from PA or PB, set the contents of PA or PB to "1" prior to reading instruction.
(7) At execution of the THB instruction, any input made during a period of T_{INH} ($15 \times 1/f_{(OSC)}$) shown in the above figure may be neglected.



DESCRIPTION OF TERMINALS

GND (Pin 33)
Circuit grounding potential

V_{DD} (Pin 23)
Main power supply

OSC_0 (Pin 17)
Input of internal oscillation circuit at one side of crystal resonator and ceramic vibrator.

$\overline{OSC_1}$ (Pin 16)
Output of internal oscillation circuit at the other side of crystal resonator and ceramic vibrator (not TTL compatible)

PA, PB (Pins 19 ~ 22 and 24 ~ 27)
These are quasi-bidirectional ports for 4-bit parallel I/O. To input data from these ports, it is necessary to write "1" to them beforehand. When nothing is applied to their terminals, the content of output ports is written in them, so they can also be used as registers. In addition, it is possible to use them to make an 8-bit parallel output depending on instructions.

PK (Pins 28 ~ 31)
Input ports for 4-bit parallel input with no latching function.

$\overline{PH}$ (Pin 14)
Input port with latching function to be set by negative logical signal.

This terminal is set at the time when the negative logical signal is applied to it from the outside. It is reset automatically after execution of the test instruction of this port.

$\overline{RESET}$ (Pin 18)
Reset must be active for greater than 1 machine cycle.

The RESET signal, when input, has priority over all of other signals and performs the following functions:

(1) Resets all bits of the program counter;
(2) Resets the timer counter and timer flag;
(3) Resets the port pointer;
(4) Resets the accumulator;
(5) Resets I/O ports PA and PB;
(6) Resets the input port PH flag;
(7) Initializes the output port PLCD for LCD; and
(8) Resets the machine cycle to M_1.

Since the $\overline{RESET}$ terminal is pulled up to V_{DD} by an internal resistor (approx. 800kΩ), it is possible to activate power ON/reset by connecting it to an external capacitor.

SYNC (Pin 15)
This is a general-purpose synchronizing signal output. The signal is output at the beginning of each machine cycle. Output constantly, this signal is used also as clock pulse to external units.

The cycle of SYNC becomes 32 times that of the original oscillation (8μs when the clock pulse is 4MHz).

PLCD 1 ~ 6 (Pins 1 ~ 13 and 34 ~ 60)
These are 7-bit and 5-bit parallel output ports, respectively. They are used to directly drive an LCD (static type). Specification of each port is done by the port pointer (PP) as shown in the table below;

Content of PP				Port Specified
b_3	b_2	b_1	b_0	
x	0	0	0	PLCD1
x	0	0	1	PLCD2
x	0	1	0	PLCD3
x	0	1	1	PLCD4
x	1	0	0	PLCD5
x	1	0	1	PLCD6 ~ 4
x	1	1	0	PLCD6 5 and BI
x	1	1	1	—

X: Don't Care
BI: 7 Segment Decoder PLA Blank Input
The data of b_0, of the internal 4-bit bus is written to 5 of PLCD6, and that of b_3 to BI.

COMMON (Pin 32)
This is a COMMON output terminal. This output signal is connected to the common electrode of static type LCD. The frequency of the COMMON signal output is given with the following equation:

$$f_{(COM)} = f_{(OSC)}/2^{17}$$

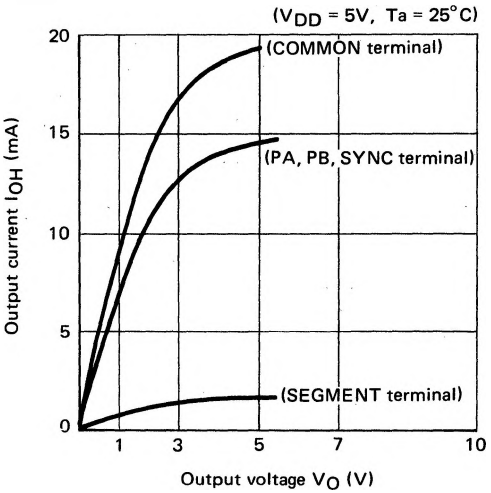
Where the basic clock $f_{(OSC)}$ is 4.19304 MHz, $f_{(COM)}$ becomes 32 Hz (duty ratio: 50%).

INSTRUCTIONS LIST

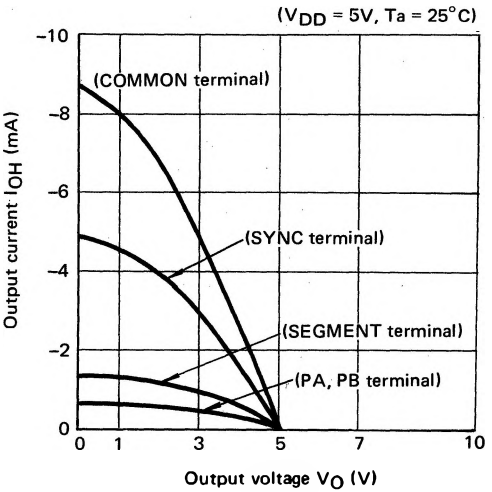
Mnemonic	Description	Instruction Code								Byte	Cycle
		7	6	5	4	3	2	1	0		
CLA	Clear Accumulator	0	0	0	1	0	0	0	0	1	1
CLL	Clear DP_L	0	0	1	0	0	0	0	0	1	1
CLH	Clear DP_H	0	1	1	0	0	0	0	0	1	1
LAI	Load Accumulator with Immediate	0	0	0	1	I_3	I_2	I_1	I_0	1	1
LLI	Load DP_L with Immediate	0	0	1	0	I_3	I_2	I_1	I_0	1	1
LHI	Load DP_H with Immediate	0	1	1	0	0	I_0	I_1	I_0	1	1
L	Load Accumulator with Memory	1	0	0	1	0	1	0	0	1	1
LAL	Load Accumulator with DP_L	0	1	0	1	0	1	0	1	1	1
LLA	Load DP_L with Accumulator	0	1	0	1	0	1	0	0	1	1
LAW	Load Accumulator with W Register	1	0	0	0	0	1	0	0	1	1
SI	Store Accumulator to Memory then Increment DP_L	1	0	0	1	0	0	0	0	1	1
LWA	Load W Register with Accumulator	1	0	0	0	0	0	0	0	1	1
LPA	Load Port Pointer with Accumulator	0	1	0	1	1	0	0	0	1	1
LTI	Load Timer with Immediate "0" (Clear Timer & TMF)	0	1	1	0	1	0	0	0	1	1
X	Exchange Accumulator with Memory	1	0	0	1	1	0	0	0	1	1
INA	Increment Accumulator	0	0	0	0	0	0	0	1	1	1
INL	Increment DP_L	0	1	0	1	0	1	1	1	1	1
INM	Increment Memory	0	1	0	1	1	1	0	1	1	1
INW	Increment W Register	1	0	0	0	1	0	0	0	1	1
DCA	Decrement Accumulator	0	0	0	0	1	1	1	1	1	1
DCL	Decrement DP_L	0	1	0	1	0	1	1	0	1	1
DCM	Decrement Memory	0	1	0	1	1	1	0	0	1	1
CAO	Complement Accumulator of One	0	1	0	1	0	0	0	0	1	1
RAL	Rotate Accumulator Left through Carry	0	1	0	0	0	1	1	1	1	1
AC	Add Memory to Accumulator with Carry	0	1	0	0	1	1	0	0	1	1
AS	Add Memory to Accumulator, Skip if Carry	0	1	0	0	1	1	1	0	1	1
AIS	Add Immediate to Accumulator, Skip if Carry	0	0	0	0	I_3	I_2	I_1	I_0	1	1
DAS	Decimal adjust Accumulator in Subtraction	0	1	0	1	1	0	1	0	1	1
CM	Compare Accumulator with Memory	0	1	0	1	1	1	1	0	1	1
SMB	Set Memory Bit	1	0	1	1	1	0	I_1	I_0	1	1
RMB	Reset Memory Bit	1	0	1	1	1	1	I_1	I_0	1	1
TAB	Test Accoumulator Bit	1	0	1	0	0	0	I_1	I_0	1	1
TMB	Test Memory Bit	1	0	1	0	0	1	I_1	I_0	1	1
THB	Test H Port Bit	1	0	1	0	1	1	0	0	1	1
TTM	Test Time flag	1	0	1	0	1	1	1	0	1	1
TC	Test Carry flag	0	1	0	0	0	0	1	0	1	1
SC	Set Carry flag	0	1	0	0	0	0	0	0	1	1
RC	Reset Carry flag	0	1	0	0	0	0	0	1	1	1
J	Jump	0	0	1	1	0	I_{10}	I_9	I_8	2	2
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
JC	Jump in Current Page	1	1	I_5	I_4	I_3	I_2	I_1	I_0	1	1
JA	Jump with Accumulator	0	1	0	0	0	0	1	1	1	1
CAL	Call Subroutine	0	0	1	1	1	I_{10}	I_9	I_8	2	2
		I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0		
RT	Return from Subroutine	0	1	0	1	1	0	0	1	1	1
OTD	Output Table Data	0	1	1	1	0	0	0	1	1~15	2
OA	Output Accumulator to Port A	0	1	1	1	0	0	1	0	1	1
OB	Output Accumulator to Port B	0	1	1	1	0	0	1	1	1	1
OP	Output Accumulator to Port designated Port Pointer	0	1	1	1	0	1	0	0	1	1
OPM	Output Memory to Port P designated Port Pointer	0	1	1	1	0	1	1	0	1	1
IA	Input Port A in Accumulator	0	1	1	1	1	0	1	0	1	1
IB	Input Port B in Accumulator	0	1	1	1	1	0	1	1	1	1
IK	Input Port K in Accumulator	0	1	1	1	1	1	0	0	1	1
NOP	No Operation	0	0	0	0	0	0	0	0	1	1

TYPICAL PERFORMANCE CURVES

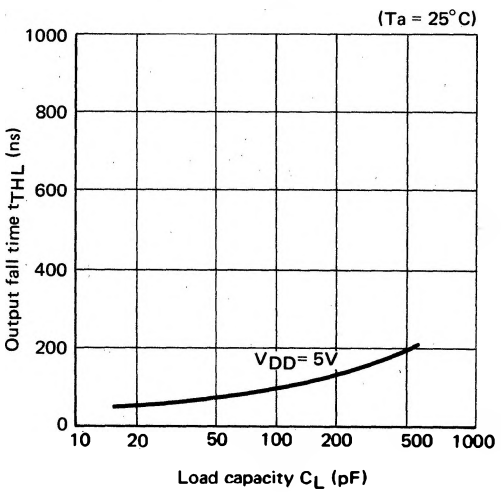
Output Current (I_{OL}) TYP



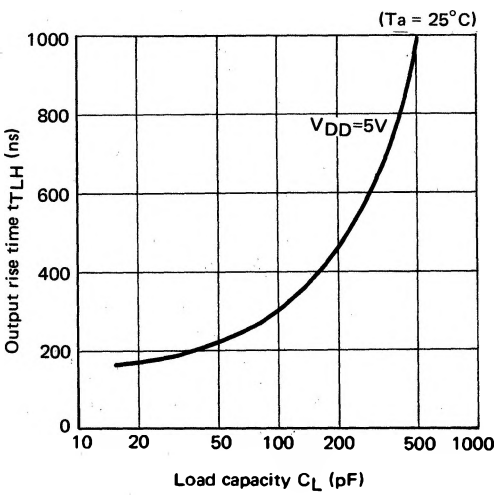
Output Current (I_{OH}) TYP



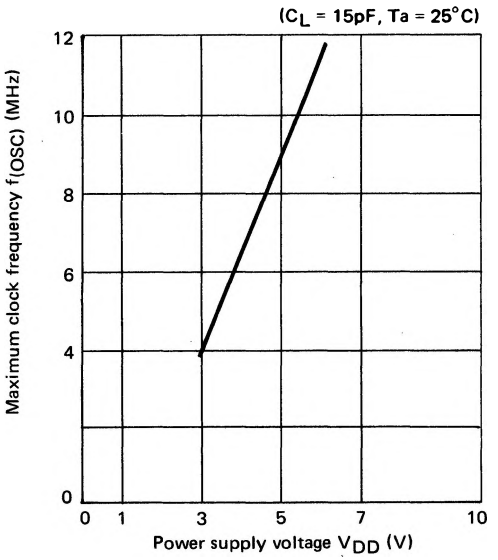
t_{THL} – C_L Characteristic TYP



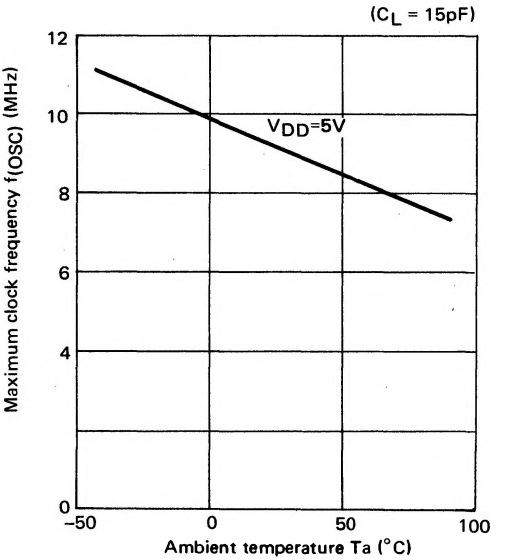
t_{TLH} – C_L Characteristic TYP



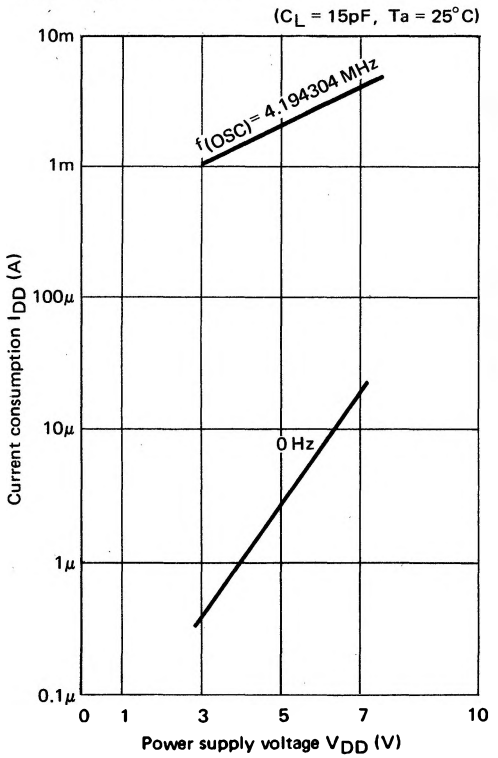
$f_{(OSC)}$ – V_{DD} Characteristic TYP



$f_{(OSC)}$ – Ta Characteristic TYP



I_{DD} – V_{DD} Characteristic TYP



I_{DD} – $f_{(OSC)}$ Characteristic TYP