

MSM5165LRS/JS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

GENERAL DESCRIPTION

The MSM5165LRS/JS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165LRS/JS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100 μ A) when there is no chip selection.

A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, CE₁, CE₂ and OE signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

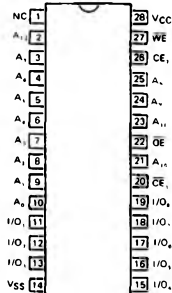
FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
 - Standby; 0.55 mW MAX
 - Operation; 248 mW MAX
- High Speed (Equal Access and Cycle Time)
 - 120 – 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
 - 64K EPROM (MSM2764)
 - 28-pin DIP PKG
 - 32-pin PLCC

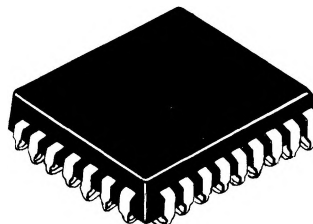


PIN CONFIGURATION

(Top View)

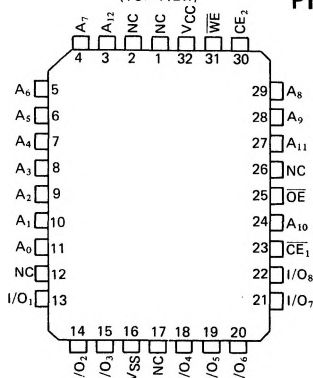


A₀ ~ A₁₂ : Address INPUTS
 I/O₁ ~ I/O₈ : Data Input/Output
 CE₁, CE₂ : Chip Select
 WE : Write Enable
 OE : Output Enable
 VCC, VSS : Supply Voltage



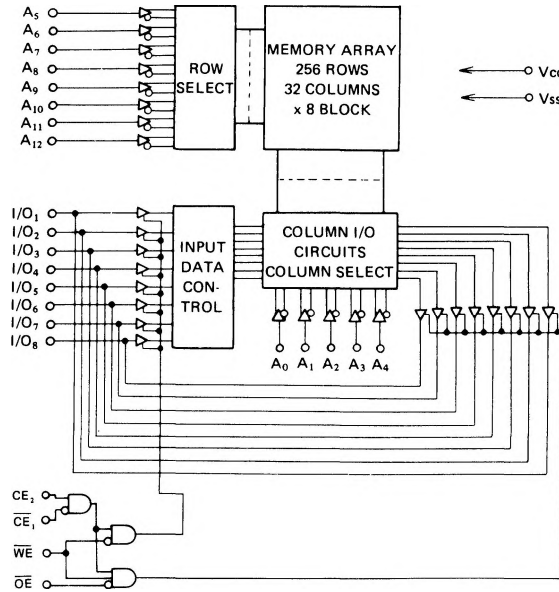
PIN CONFIGURATION

(TOP VIEW)



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FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	CE ₁	CE ₂	WE	OE	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	DOUT
Write	L	H	L	X	DIN

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V _{CC}	-0.3 to 7.0	V	Respect to GND
Input Voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V	
Operating Temperature	T _{opr}	0 to 70	°C	
Storage Temperature	T _{stg}	-55 to 150	°C	
Power Dissipation	P _D	1.0	W	T _a = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V _{CC}	4.5	5	5.5	V	5V ± 10%
	V _{SS}		0		V	
Data Retention Voltage	V _{CCH}	2	5	5.5	V	
Input Voltage	V _{IH}	2.2		V _{CC} + 0.3	V	5V ± 10%
	V _{IL}	-0.3		0.8	V	
Output Load	C _L			100	pF	
	TTL			1		

DC CHARACTERISTICS

($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $+70^\circ C$)

Parameter	Symbol	MSM5165L			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	-1		1	μA	$V_{IN} = 0$ to V_{CC}
Output Leakage Current	I_{LO}	-1		1	μA	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = 0$ to V_{CC}
Output Voltage	V_{OH}	2.4			V	$I_{OH} = -1$ mA
	V_{OL}			0.4	V	$I_{OL} = 2.1$ mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$ or $V_{IN} = 0$ to V_{CC} $CE_2 \leq 0.2V$ $V_{IN} = 0$ to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1 = V_{IH}$, $CE_2 = V_{IL}$ $t_{CYC} = \text{Min, cycle}$
Operating Supply Current	I_{CCA}			①	mA	$T_{CYC} = \text{Min, cycle}$
				15		$T_{CYC} = 1 \mu s$

AC CHARACTERISTICS

Test Condition

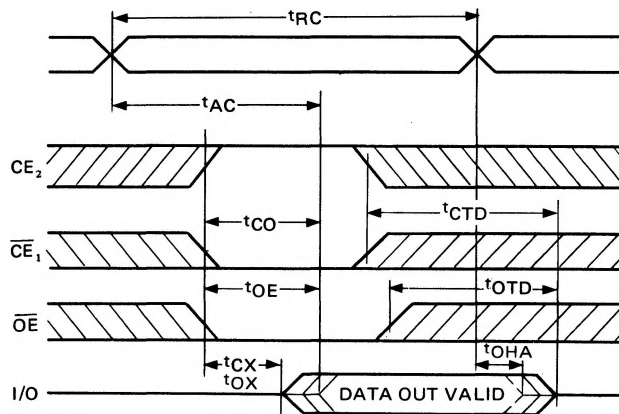
Parameter	Conditions
Input Pulse Level	$V_{IH}=2.4V$, $V_{IL}=0.6V$
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	$C_L=100$ pF, 1 TTL Gate

READ CYCLE

($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	MSM5165-12		MSM5165-15		MSM5165-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Enable Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		60		70		90	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	40	0	50	0	60	ns
Output 3-state from Chip Deselection	t_{CTD}	0	60	0	70	0	80	ns

READ CYCLE



- Notes:**
1. A Read occurs during the overlap of a low $\overline{CE}_1$, a high CE_2 , a low $\overline{OE}$ and a high $\overline{WE}$.
 2. t_{CX} is specified from $\overline{CE}_1$, CE_2 or $\overline{OE}$, whichever occurs last.
 3. t_{OTD} is specified from $\overline{CE}_1$, CE_2 or $\overline{OE}$, whichever occurs first.
 4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

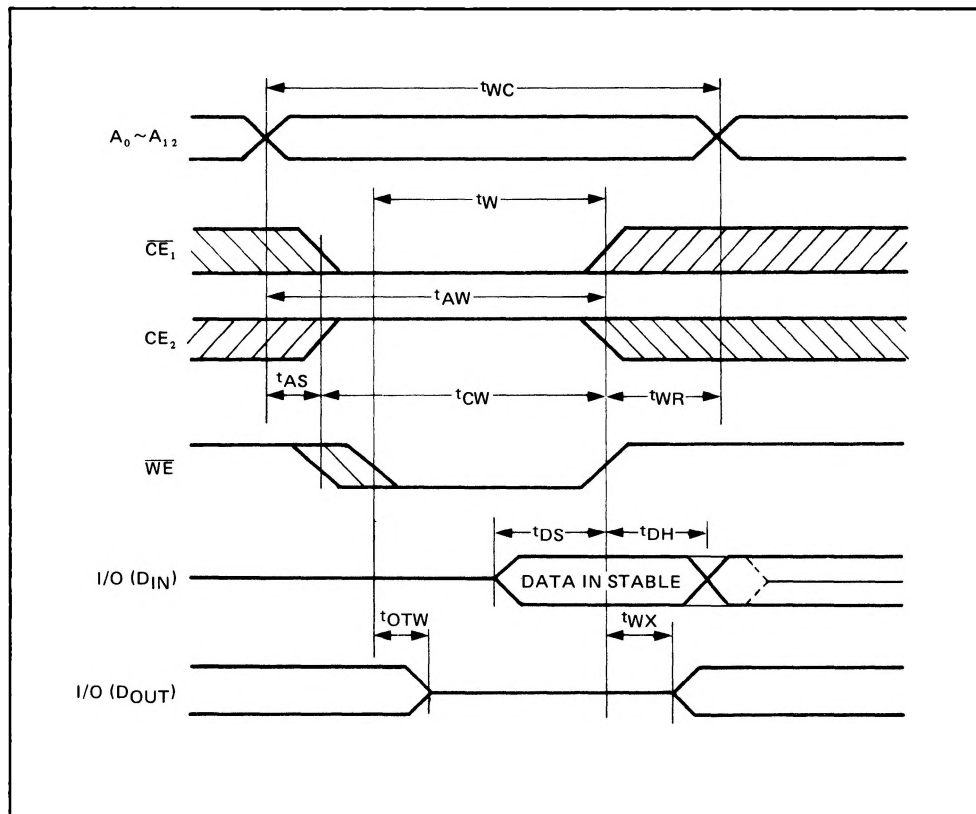
WRITE CYCLE

($V_{CC} = 5V \pm 10\%$, $T_a = 0^\circ C$ to $+70^\circ C$)

Item	Symbol	MSM5165L-12		MSM5165L-15		MSM5165L-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	100		120		150		ns
Address Valid to End of Write	t_{AW}	100		120		150		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

- Notes:**
1. A Write Cycle occurs during the overlap of a low $\overline{CE}_1$, a high CE_2 and a low $\overline{WE}$.
 2. $\overline{OE}$ may be both high and low in a Write Cycle.
 3. t_{AS} is specified from $\overline{CE}_1$, CE_2 or $\overline{WE}$, whichever occurs last.
 4. t_W is an overlap time of a low $\overline{CE}_1$, a high CE_2 and a low $\overline{WE}$.
 5. t_{WR} , t_{DS} and t_{DH} are specified from $\overline{CE}_1$, CE_2 or $\overline{WE}$, whichever occurs first.
 6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
 7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

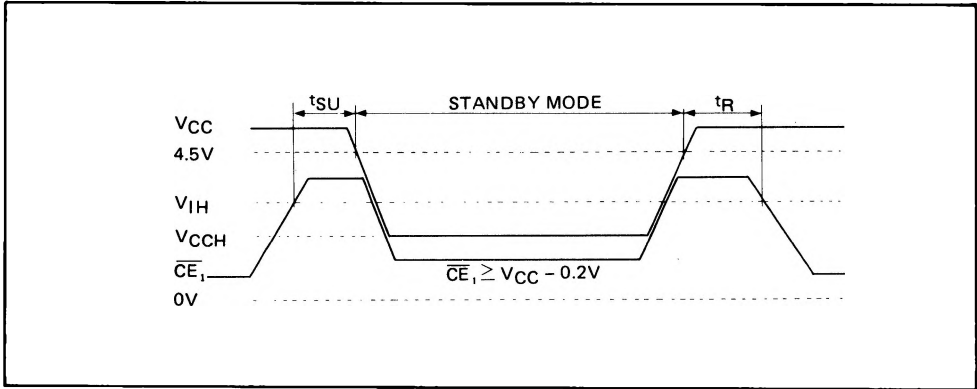


LOW V_{CC} DATA RETENTION CHARACTERISTICS

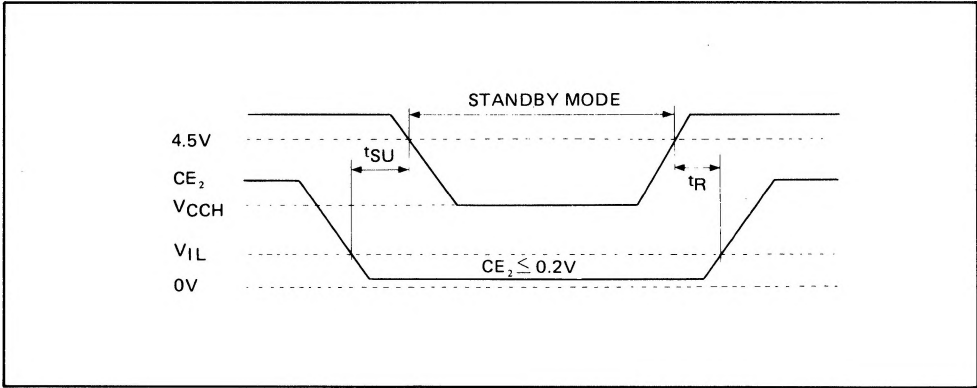
($T_a = 0^\circ\text{C}$ to $+70^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CE}_1 \geq V_{CC} - 0.2V, CE_2 \geq V_{CC} - 0.2V$
						$CE_2 \leq 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	$V_{CC} = 3V, \overline{CE}_1 \geq V_{CC} - 0.2V, CE_2 \geq V_{CC} - 0.2V$
						$V_{CC} = 3V, CE_2 \leq 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CE}_1$ CONTROL



CE_2 CONTROL



CAPACITANCE

($T_a = 25^\circ C$, $f = 1MHz$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.