OKI semiconductor

MSM5056

CMOS 4BIT SINGLE CHIP VERY LOW POWER MICROCONTROLLER WITH LCD DRIVER

GENERAL DESCRIPTION

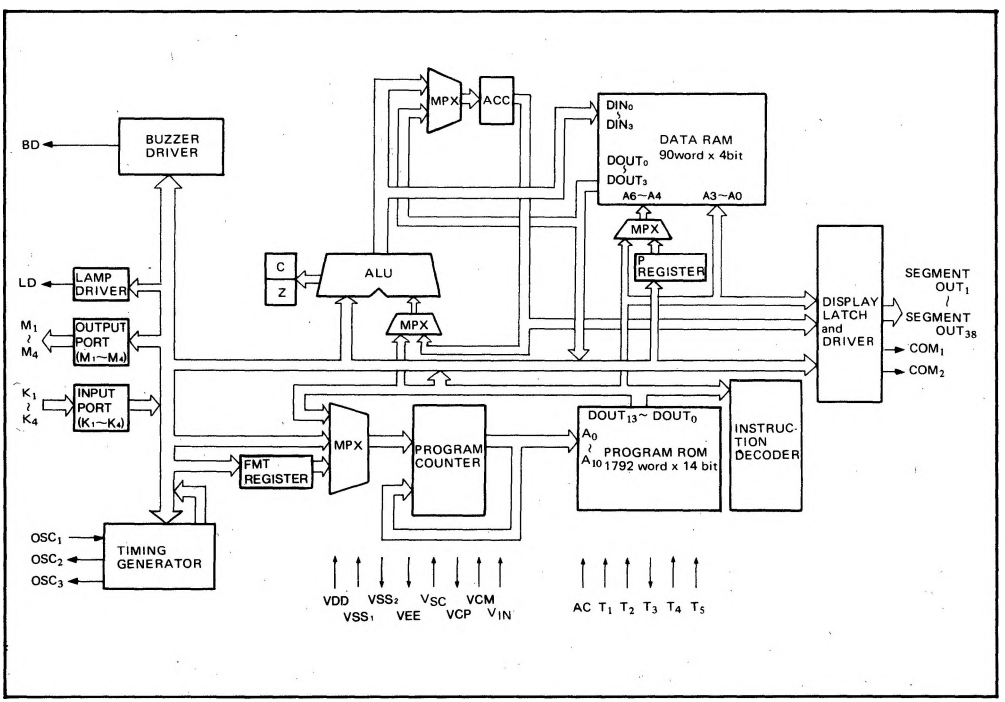
The OKI MSM5056 is a low-power, high-performance single-chip microcontroller employing complementary metal oxide semiconductor technology. Integrated onto a single chip are a 4-bit ALU, 25K bits of mask programmable ROM, 360 bits of data RAM, crystal oscillator, voltage doubler, timer, LCD driver, input port, output port and overcharge protection circuit for connection to a solar cell.

The MSM5056 is widely used in electronic products requiring low power operation, for example, solar calculator watches and games.

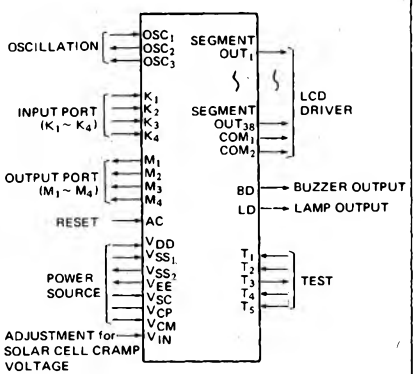
FEATURES

- Low Power Consumption 3 μA Typical
- 1792 × 14 Internal ROM
- 90 × 4 Internal RAM
- 4 Input Port
- 4 Output Port
- 4 × 4 Key Matrix Input (K_1~K_4, M_1~M_4)
- 38 LCD Driver (1/2 Duty, 1/2 Bias, 88 Segment)
- 42 Instructions
- 1.5 V Operating Voltage (The solar cell can be connected.)
- 32.768 kHz Crystal Oscillator
- 122.1 μs Instruction Cycle
- −20 to 75°C Operating Temperature
- 68 pad die

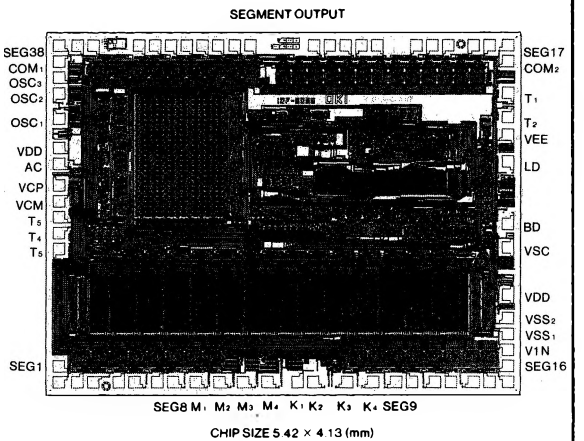
FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL



CHIP PAD LAYOUT



PIN DESCRIPTION

Designation	Function
V_{DD}	Circuit ground potential
V_{SS_1}	Power source (−1.5 V)
V_{SC}	Solar cell connection terminal
V_{SS_2}	Power source for LCD driver (−3.0 V) This terminal is connected to V_{DD} terminal through a 0.1 μF capacitor.
V_{EE}	Power source for internal logic (−1.5 to −3.0 V) This terminal is connected to V_{DD} terminal through a 0.1 μF capacitor.
V_{CP}, V_{CM}	Booster capacitor connection terminals V_{CP} terminal is connected to V_{CM} terminal through a 0.1 μF capacitor.
XT, $\overline{XT}$	Input and output terminals of oscillator inverter, 32.768 kHz crystal is connected to these terminals.
$T_1 \sim T_5$	Terminals to test internal logic, $T_1 \sim T_3$ and T_5 are pulled down to V_{SS_1}. T_4 is output. Test pins must be normaly open.
AC	Terminal to clear internal logic pulled down to V_{SS_1}. After power is turned on, the MSM5056 must be reset by this terminal.
BD	Buzzer output
LD	Lamp output
V_{IN}	Adjustment for solar cell cramp voltage This terminal is connected to V_{SS_1} terminal through 50 ~ 200 kΩ resistor.

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5056 is given on page 111. Each block of logic will be briefly discussed. For more information, please refer to the MSM5056 user's manual.

Program ROM

The MSM5056 will address up to 1.75 K words of internal mask programmable ROM. Each word consists of 14 bits and all instructions are one word. The instructions are routed to a programmed logic array which generates the signals necessary for control of logic.

Data RAM

Data is organized in 4 bit nibbles. Internal data RAM consists of 90 nibbles.

The RAM is addressed by page address and column address. Normally page address is specified with the page register, but direct addressing is available at Page 0.

Column address is directly addressed by the operands of various instructions.

ALU

The ALU performs 4-bit parallel operation of RAM and AC contents, or RAM contents and an immediate digit. It sets or resets the flags (Z, C) depending on the condition.

Program Counter (PC)

The program counter is an 11-bit wide counter and specifies the address of the program ROM.

The PC is incremented by one at every execution of an instruction, and then specifies the next instruction to be executed. However, the contents of the PC are rewritten by the execution of a Jump or Branch instruction.

There is no boundary in the ROM, so a Jump or Branch instruction can be put anywhere in the ROM.

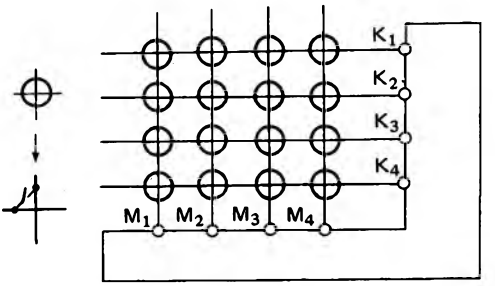
Input/Output Port

Input Port (K1 ~ K2)

The input port (K1 ~ K4) is a 4-bit parallel input port. Each pin of the port is pulled down to V_{SS1} by an internal resistor, and the status of the port can be fetched by an input instruction.

Output Port (M1 ~ M4)

The output port (M1 ~ M4) is a 4-bit parallel output port. This port consists of data latches and buffers. The contents of data latches are rewritten by an output instruction. A key matrix is used in combination with K1 to K4.



Display Function

The MSM5056 is provided with a segment output terminal which can directly drive a 1/2 bias, 1/2 duty LCD and common drive output terminals. COM1 and COM2. The segment drive circuit consists of the display data latch, multiplexer and driver. If the data is sent to the display data latch with the display instruction, the LCD drive waveform is output to the segment drive output terminal.

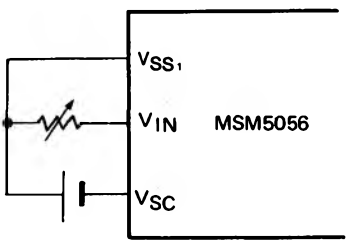
Time Base

Time base of the CPU is provided by connecting a 32.768 kHz crystal to the OSC1 and OSC3 pin. One machine cycle is 122.1μs.

A hardware divider up to 1 Hz is provided enabling programs to implement and a clock function by counting signals between 16 and 1 Hz.

Solar Cell Overcharge Protection Circuit

When a solar cell is connected to prolong the usefull life of the battery, a resistor is inserted between the V_{IN} pin and V_{SS1} to adjust the overcharge protection voltage.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits	Unit
Supply Voltage 1	$V_{DD} - V_{SS_1}$	Ta = 25°C	−0.3 to +3.0	V
Supply Voltage 2	$V_{DD} - V_{SC}$	Ta = 25°C	−0.3 to +3.5	V
Supply Voltage 3	$V_{DD} - V_{SS_2}$	Ta = 25°C	−0.3 to +6.0	V
Supply Voltage 4	$V_{DD} - V_{EE}$	Ta = 25°C	−0.3 to +6.0	V
Input Voltage	V_{IN_1}	Ta = 25°C	V_{SS_1}, −0.3 to +0.3	V
Storage Temperature	Tstg		−55 to 125	°C

OPERATING CONDITIONS

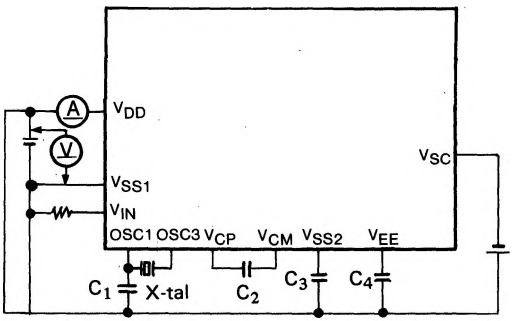
Parameter	Symbol	Limits	Unit
Operating Voltage	$V_{DD} - V_{SS_1}$	1.25 to 1.65	V
Operating Temperature	Topr	−20 to 75	°C

DC CHARACTERISTICS

(V_{DD} =0V, V_{SS_1}, V_{EE} = −1.55V, V_{SS_2} = −3.0V, C_I = 30kΩ, C_G = 30pF, Ta = 25°C)

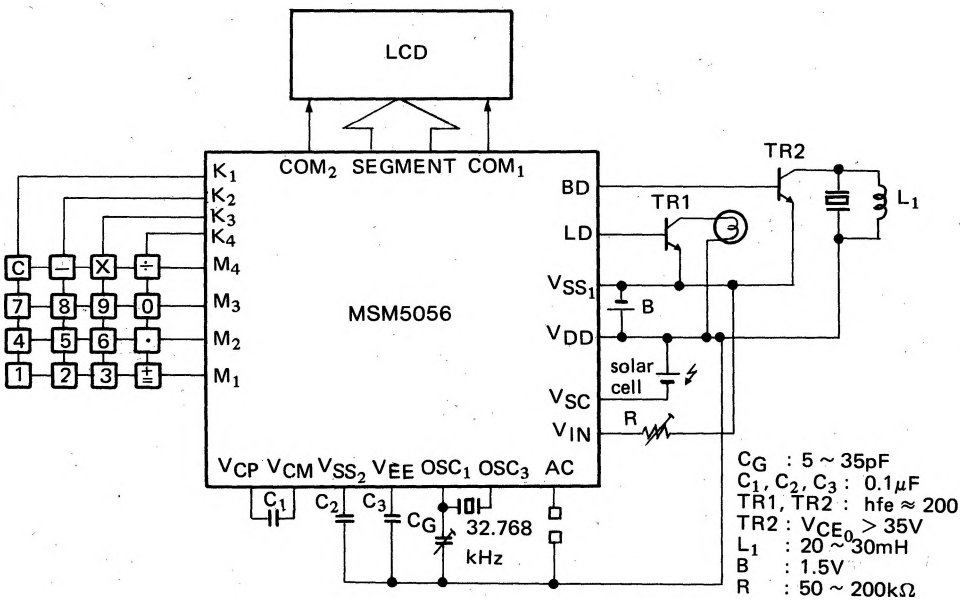
Parameter	Symbol	Condition		Limits Min.	Limits Typ.	Limits Max.	Unit
Operating voltage 1	$-V_{SS_1}$	V_{SS_1} terminal		1.25	1.55	2.0	V
Operating voltage 2	$-V_{SC}$	V_{SC} terminal		0	2.0	3.0	V
Power supply current	I_{DD}	V_{SS_1} terminal		−	3.0	−	μA
Oscillation start voltage	$-V_{OSC}$	Within 10 seconds V_{SS_1} terminal		1.45	−	−	V
Output current 1 COM	I_{OH_1}	$V_{OH_1} = -0.2V$		−4	−	−	μA
	I_{OM_1}	$V_{OM_1} = V_{SS_1} \pm 0.2V$		4/−4	−	−	
	I_{OL_1}	$V_{OL_1} = -2.8V$		4	−	−	
Output current 2 SEGMENT	I_{OH_2}	$V_{OH_2} = -0.2V$		−0.4	−	−	μA
	I_{OL_2}	$V_{OL_2} = -2.8V$		0.4	−	−	
Output current 3 $M_1 \sim M_4$	I_{OH_3}	V_{SS_1}, V_{EE} −1.25V	V_{OH_3} −0.4 V	−100	−	−	μA
	I_{OL_3}	V_{SS_2} −2.3V	V_{OL_3} −0.85V	3	−	8	
Output current 4 BD	I_{OH_4}	$V_{OH_4} = -0.4V$		−50	−100	−200	μA
	I_{OL_4}	$V_{OL_4} = -1.15V$		3	10	30	
Input current $K_1 \sim K_4$	I_{IH_1}	$V_{IN} = -0V$		5	10	15	μA
	I_{IL_1}	$V_{IN} = -1.55V$		−	−	−0.2	
Oscillator built-in capacitor	CD			−	20	−	pF
Solar battery cramp resistor	R_{IN}	$V_{SS_1} = -1.8V$ V_{IN} terminal		50	−	200	kΩ

MEASURING CIRCUIT



C_1 : 30pF
C_2, C_3, C_4 : 0.1μF
X-tal : 32.768kHz

TYPICAL APPLICATION



C_G : 5 ~ 35pF
C_1, C_2, C_3 : 0.1μF
TR1, TR2 : hfe ≈ 200
TR2 : V_{CE_0} > 35V
L_1 : 20 ~ 30mH
B : 1.5V
R : 50 ~ 200kΩ

DESCRIPTION OF INSTRUCTIONS

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Arithmetic operation	ADD ACC, AP	0	0	0	0	0	P	0	1	0	0	A				AP ← (AP) + (ACC)
	ADD #D, AP	0	1	1	0	0	P	D				A				AP ← (AP) − D
	ADC AP	0	0	0	0	0	P	0	1	0	1	A				AP ← Decimal adjust {(AP) + (ACC) + (C)}
	SUB ACC, AP	0	0	0	0	1	P	0	1	0	0	A				AP ← (AP) − (ACC)
	SUB #D, AP	0	1	1	0	1	P	D				A				AP ← (AP) − D
	SBC AP	0	0	0	0	1	P	0	1	0	1	A				AP ← Decimal adjust {(AP) − (ACC) − (C)}
	CMP ACC, AP	0	0	0	0	1	P	1	1	1	0	A				(AP) − (ACC)
	CMP #D, AP	0	1	0	1	1	P	D				A				(AP) − D
	INC AP	0	1	1	0	0	P	0	0	0	1	A				AP ← (AP) + 1
	DEC AP	0	1	1	0	1	P	0	0	0	1	A				A ← (AP) − 1
	XOR ACC, AP	0	0	0	0	0	P	0	1	1	1	A				AP ← (AP) ∀ (ACC)
	XOR #D, AP	0	1	1	1	1	P	D				A				AP ← (AP) V D
Bit operation	BIT ACC, AP	0	0	0	0	0	P	1	1	1	0	A				(AP) V $\overline{(ACC)}$
	BIT #D, AP	0	1	0	1	0	P	D				A				(AP) V $\overline{D}$
	BIS ACC, AP	0	0	0	0	0	P	0	1	1	0	A				AP ← (AP) V (ACC)
	BIS #D, AP	0	1	0	0	0	P	D				A				AP ← (AP) V D
	BIC ACC, AP	0	0	0	0	1	P	0	1	1	0	A				AP ← (AP) Λ $\overline{(ACC)}$
	BIC #D, AP	0	1	0	0	1	P	D				A				AP ← (AP) Λ $\overline{D}$
Shift	ASR AP	0	0	0	0	0	P	0	0	1	1	A				(C) 0 → (AP)
	ASL AP	0	0	0	0	1	P	0	0	1	1	A				(C) ← (AP) ← 0
Flag operation	CLZ	0	0	0	0	0	0	1	0	1	0	0	0	0	0	Z ← 0
	CLC	0	0	0	0	0	0	1	0	0	1	0	0	0	0	C ← 0
	CLA	0	0	0	0	0	0	1	0	1	1	0	0	0	0	Z ← 0, C ← 0
	SEZ	0	0	0	0	1	0	1	0	1	0	0	0	0	0	Z ← 1
	SEC	0	0	0	0	1	0	1	0	0	1	0	0	0	0	C ← 1
	SEA	0	0	0	0	1	0	1	0	1	1	0	0	0	0	Z ← 1, C ← 1
Data transfer	MOV ACC, AP	1	1	1	1	0	P	0	0	0	0	A				AP ← (ACC)
	MOV ACC, AX	1	1	1	1	0	0	0	X			A				AX ← (ACC)
	MOV #D, AP	0	1	1	1	0	P	D				A				AP ← D
	MOV AP, ACC	1	1	1	1	1	P	0	0	0	0	A				ACC ← (AP)
	MOV AX, ACC	1	1	1	1	1	0	0	X			A				ACC ← (AX)
	CHG AP	1	1	1	0	0	P	0	0	0	0	A				(ACC) ⟷ (AP)
	CHG AX	1	1	1	0	0	0	0	X			A				(ACC) ⟷ (AX)

DESCRIPTION OF INSTRUCTIONS (CONT.)

	Mnemonic	Instruction Code														Operation
		13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Jump	JMP adrs	1	0	0	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	PC ← adrs
	JMP @AP	0	0	0	0	0	P	1	1	0	1	A				PC ← (PC) + (AP) + 1
	JMPIO @AP	0	0	0	0	1	P	1	1	0	1	A				PC ← (PC) + {(AP)∧7H} + +1
	BEQ +n BZE +n	0	0	0	1	1	0	0	1	0	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if Z=1
	BNE +n BNZ +n	0	0	0	1	1	0	1	1	0	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if Z=0
	BCS +n BLT +n	0	0	0	1	1	0	0	0	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if C=1
	BCC +n BGE +n	0	0	0	1	1	0	1	0	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if C=0
	BGT +n	0	0	0	1	1	0	1	1	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if Z=0 and C=0
	BLE +n	0	0	0	1	1	0	0	1	1	n_4	n_3	n_2	n_1	n_0	PC ← (PC) +n+1, if Z=1 or C=1
Input/ Output	INP Port, AP	1	1	0	1	0	P	Port				A				AP ← (Port)
	OUT AP, Port	1	1	0	1	1	P	Port				A				Port ← (AP)
	OUT #D, Port	0	0	0	1	0	0	Port				D				Port ← D
Display	DSP digit, AP	0	0	1	0	0	P	digit				A				digit ← (AP), (ACC)
	DSPF digit, AP	0	0	1	1	0	P	digit				A				digit ← (AP) via table
CPU control	HALT	0	0	0	1	0	0	0	0	0	0	0	0	0	0	Halt CPU
	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	No Operation