# OKI semiconductor

# MSM41256AAS/RS

## 262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Page Mode Type>

## GENERAL DESCRIPTION

The Oki MSM41256A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

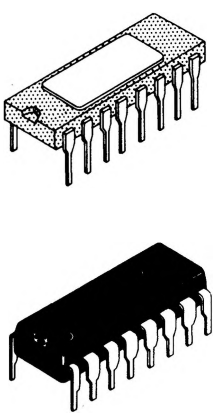
Multiplexed row and column address inputs permit the MSM41256A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41256A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$" refresh provides an on-chip refresh capability.

The MSM41256A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

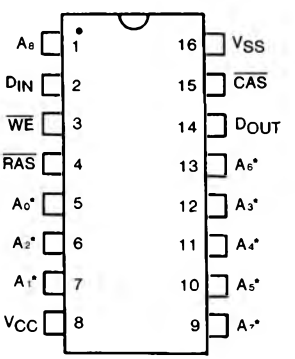
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

## FEATURES

- 262,144 × 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41256A-10AS/RS)
  - 120 ns max (MSM41256A-12AS/RS)
  - 150 ns max (MSM41256A-15AS/RS)
- Cycle time:
  - 200 ns min (MSM41256A-10AS/RS)
  - 220 ns min (MSM41256A-12AS/RS)
  - 260 ns min (MSM41256A-15AS/RS)
- Low power:
  - 385 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{\text{CAS}}$
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- "Page Mode" capability



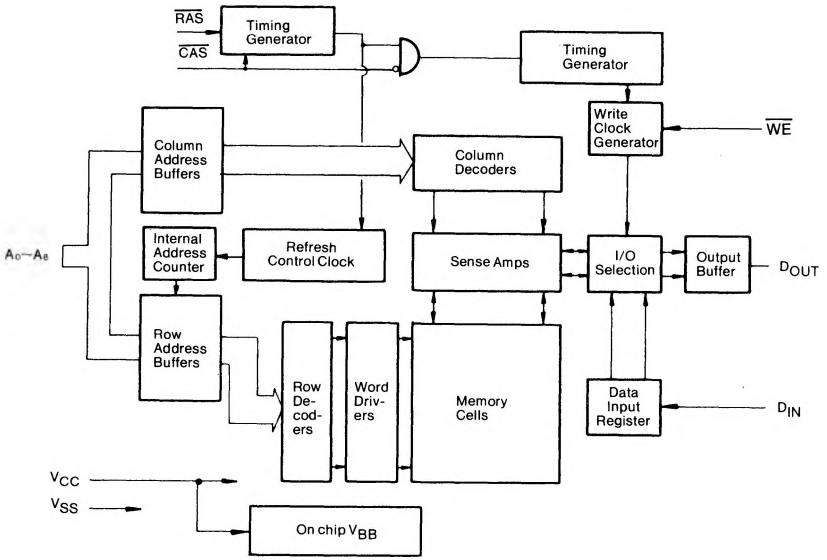
### PIN CONFIGURATION (TOP VIEW)




| Pin Names | Function |
|---|---|
| $A_0 \sim A_8$ | Address Inputs |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| $\overline{\text{WE}}$ | Write Enable |
| $D_{IN}$ | Data Input |
| $D_{OUT}$ | Data Output |
| $V_{CC}$ | Power Supply (+5V) |
| $V_{SS}$ | Ground (0V) |

* Refresh Address

## FUNCTIONAL BLOCK DIAGRAM




## ELECTRICAL CHARACTERISTICS

**ABSOLUTE MAXIMUM RATINGS** (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | −1 to +7 | V |
| Voltage on $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | −1 to +7 | V |
| Operating temperature | Topr | 0 to 70 | °C |
| Storage temperature | Tstg | −55 to +150 | °C |
| Power dissipation | $P_D$ | 1.0 | W |
| Short circuit output current | | 50 | mA |

**Note:** Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**
(Referenced to $V_{SS}$)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Operating Temperature |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 0°C to +70°C |
| | $V_{SS}$ | 0 | 0 | 0 | V | |
| Input High Voltage, all inputs | $V_{IH}$ | 2.4 | | 6.5 | V | |
| Input Low Voltage, all inputs | $V_{IL}$ | −1.0 | | 0.8 | V | |

**DC CHARACTERISTICS**
(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| OPERATING CURRENT*<br>Average power supply current<br>($\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC}$ = min.) | $I_{CC1}$ | | 70 | mA | |
| STANDBY CURRENT<br>Power supply current<br>($\overline{RAS} = \overline{CAS} = V_{IH}$) | $I_{CC2}$ | | 5.0 | mA | |
| REFRESH CURRENT 1*<br>Average power supply current<br>($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; $t_{RC}$ = min.) | $I_{CC3}$ | | 60 | mA | |
| PAGE MODE CURRENT*<br>Average power supply current<br>($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; $t_{PC}$ = min.) | $I_{CC4}$ | | 40 | mA | |
| REFRESH CURRENT 2*<br>Average power supply current<br>($\overline{CAS}$ before $\overline{RAS}$; $t_{RC}$ = min.) | $I_{CC5}$ | | 65 | mA | |
| INPUT LEAKAGE CURRENT<br>Input leakage current, any input<br>($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V) | $I_{LI}$ | −10 | 10 | μA | |
| OUTPUT LEAKAGE CURRENT<br>(Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$) | $I_{LO}$ | −10 | 10 | μA | |
| OUTPUT LEVELS<br>Output high voltage ($I_{OH}$ = −5 mA)<br>Output low voltage ($I_{OL}$ = 4.2 mA) | $V_{OH}$<br>$V_{OL}$ | 2.4 | <br>0.4 | V<br>V | |

**Note*:** $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with the output open.

**CAPACITANCE**
(Ta = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input capacitance ($A_0 \sim A_8$, $D_{IN}$) | $C_{IN1}$ | – | 7 | pF |
| Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | $C_{IN2}$ | – | 10 | pF |
| Output capacitance ($D_{OUT}$) | $C_{OUT}$ | – | 7 | pF |

Capacitance measured with Boonton Meter.

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

| Parameter | Symbol | Unit | MSM41256A-10 | | MSM41256A-12 | | MSM41256A-15 | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Refresh period | $t_{REF}$ | ms | | 4 | | 4 | | 4 | |
| Random read or write cycle time | $t_{RC}$ | ns | 200 | | 220 | | 260 | | |
| Read-write cycle time | $t_{RWC}$ | ns | 200 | | 220 | | 260 | | |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | ns | | 100 | | 120 | | 150 | 4, 6 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | ns | | 50 | | 60 | | 75 | 5, 6 |
| Output buffer turn-off delay | $t_{OFF}$ | ns | 0 | 30 | 0 | 30 | 0 | 30 | |
| Transition time | $t_T$ | ns | 3 | 50 | 3 | 50 | 3 | 50 | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | ns | 85 | | 90 | | 100 | | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | ns | 105 | 10μs | 120 | 10μs | 150 | 10μs | |
| $\overline{RAS}$ hold time | $t_{RSH}$ | ns | 55 | | 60 | | 75 | | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | ns | 55 | 10μs | 60 | 10μs | 75 | 10μs | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | ns | 105 | | 120 | | 150 | | |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | ns | 25 | 50 | 25 | 60 | 25 | 75 | 7 |
| $\overline{CAS}$ to $\overline{RAS}$ set-up time | $t_{CRS}$ | ns | 20 | | 20 | | 20 | | |
| Row address set-up time | $t_{ASR}$ | ns | 0 | | 0 | | 0 | | |
| Row address hold time | $t_{RAH}$ | ns | 15 | | 15 | | 15 | | |
| Column address set-up time | $t_{ASC}$ | ns | 0 | | 0 | | 0 | | |
| Column address hold time | $t_{CAH}$ | ns | 20 | | 20 | | 25 | | |
| Read command set-up time | $t_{RCS}$ | ns | 0 | | 0 | | 0 | | |
| Read command hold time referenced to $\overline{CAS}$ | $t_{RCH}$ | ns | 0 | | 0 | | 0 | | |
| Read command hold time referenced to $\overline{RAS}$ | $t_{RRH}$ | ns | 20 | | 20 | | 20 | | |
| Write command set-up time | $t_{WCS}$ | ns | 0 | | 0 | | 0 | | 8 |

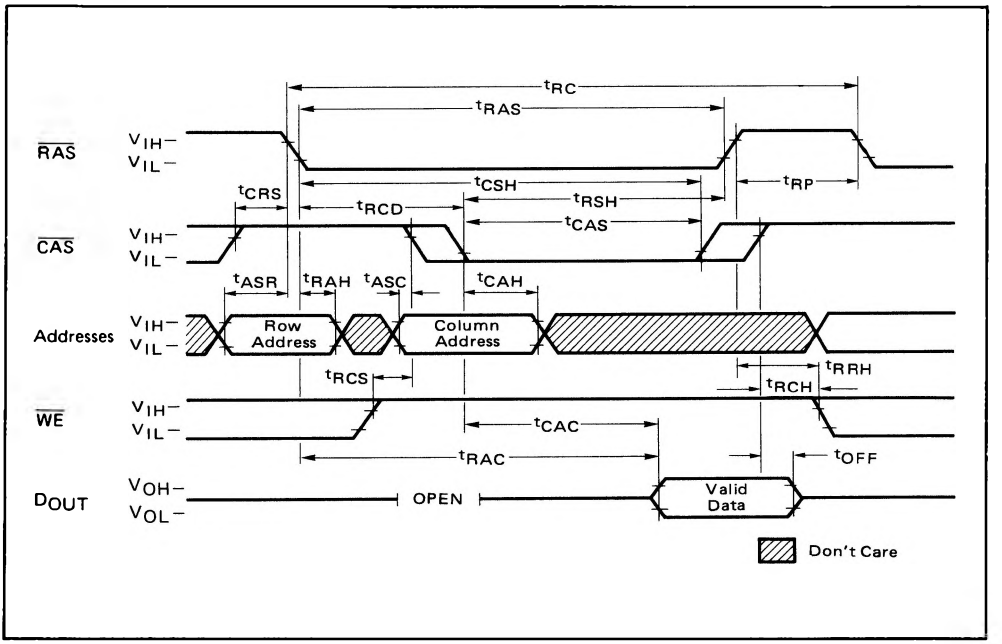
**AC CHARACTERISTICS (Continued)**
(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | Unit | MSM41256A-10 | | MSM41256A-12 | | MSM41256A-15 | | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Write command pulse width | $t_{WP}$ | ns | 15 | | 20 | | 25 | | |
| Write command hold time | $t_{WCH}$ | ns | 15 | | 20 | | 25 | | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | ns | 35 | | 40 | | 45 | | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | ns | 35 | | 40 | | 45 | | |
| Data-in set-up time | $t_{DS}$ | ns | 0 | | 0 | | 0 | | |
| Data-in hold time | $t_{DH}$ | ns | 20 | | 20 | | 25 | | |
| $\overline{CAS}$ to WE delay time | $t_{CWD}$ | ns | 15 | | 20 | | 25 | | 8 |
| Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$ | $t_{FCS}$ | ns | 20 | | 25 | | 30 | | |
| Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ | $t_{FCH}$ | ns | 20 | | 25 | | 30 | | |
| $\overline{CAS}$ precharge time (C before R cycle) | $t_{CPR}$ | ns | 20 | | 25 | | 30 | | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ active time | $t_{RPC}$ | ns | 20 | | 20 | | 20 | | |
| Page mode cycle time | $t_{PC}$ | ns | 100 | | 120 | | 150 | | 9 |
| Page mode read write cycle time | $t_{PRWC}$ | ns | 100 | | 120 | | 150 | | 9 |
| Page mode $\overline{CAS}$ precharge time | $t_{CP}$ | ns | 40 | | 50 | | 65 | | 9 |
| Refresh counter test cycle time | $t_{RTC}$ | ns | 340 | | 375 | | 430 | | 10 |
| Refresh counter test $\overline{RAS}$ pulse width | $t_{TRAS}$ | ns | 230 | 10$\mu$s | 265 | 10$\mu$ | 320 | 10$\mu$s | 10 |
| Refresh counter test $\overline{CAS}$ precharge time | $t_{CPT}$ | ns | 50 | | 60 | | 70 | | 10 |

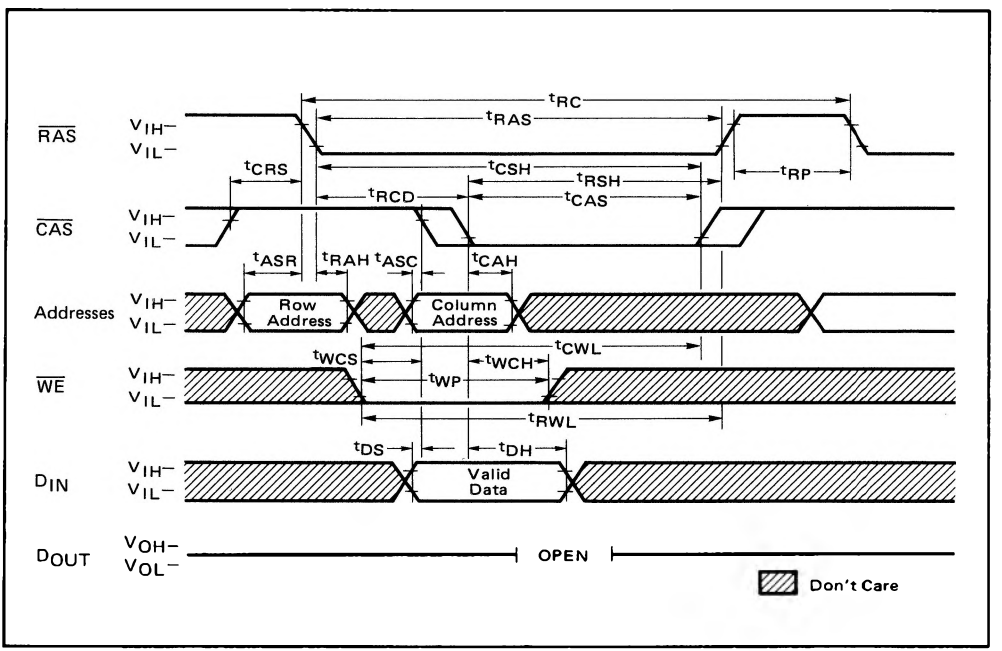
**Notes:**

1. An initial pause of 100 $\mu$s is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. $V_{IH}$ (Min.) and $V_{IL}$ (Max.) are reference levels for measuring of input signals. Also transition times are measured between $V_{IH}$ and $V_{IL}$.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the $t_{RCD}$ (Max.) limit insures that $t_{RAC}$ (Max.) can be met. $t_{RCD}$ (Max.) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (Max.) limit, then access time is controlled exclusively by $t_{CAC}$.
8. $t_{WCS}$ and $t_{CWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Page mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

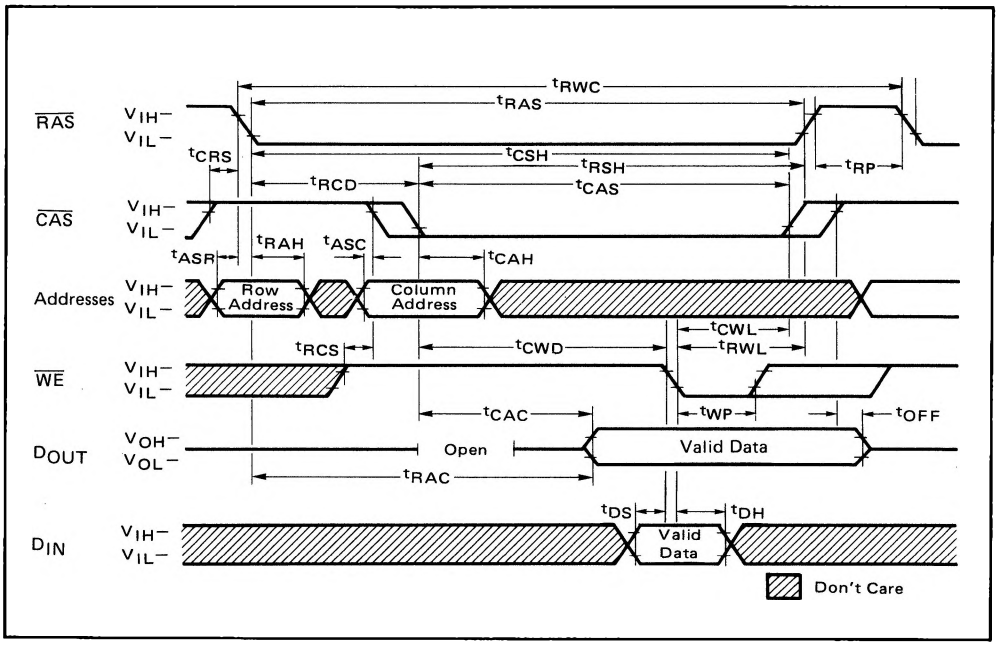
## READ CYCLE



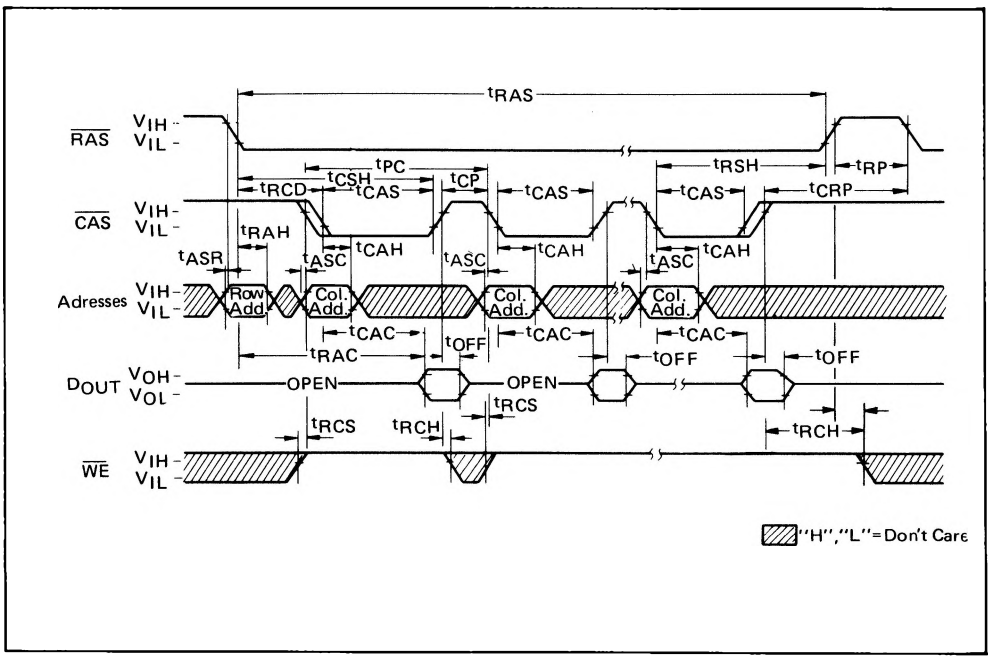

## WRITE CYCLE (EARLY WRITE)



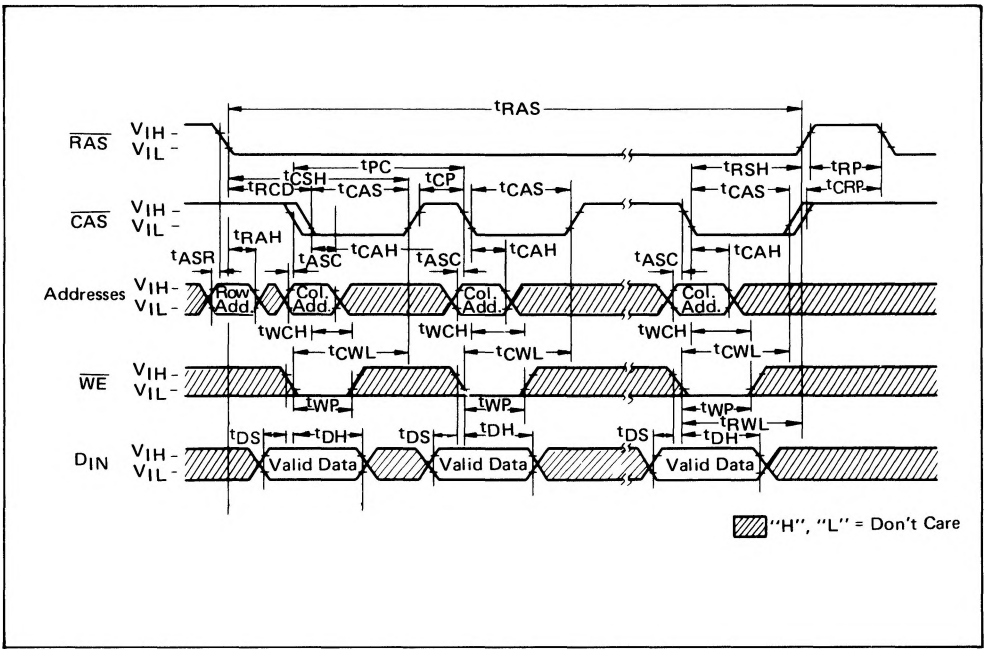
## READ/WRITE/READ-MODIFY-WRITE CYCLE



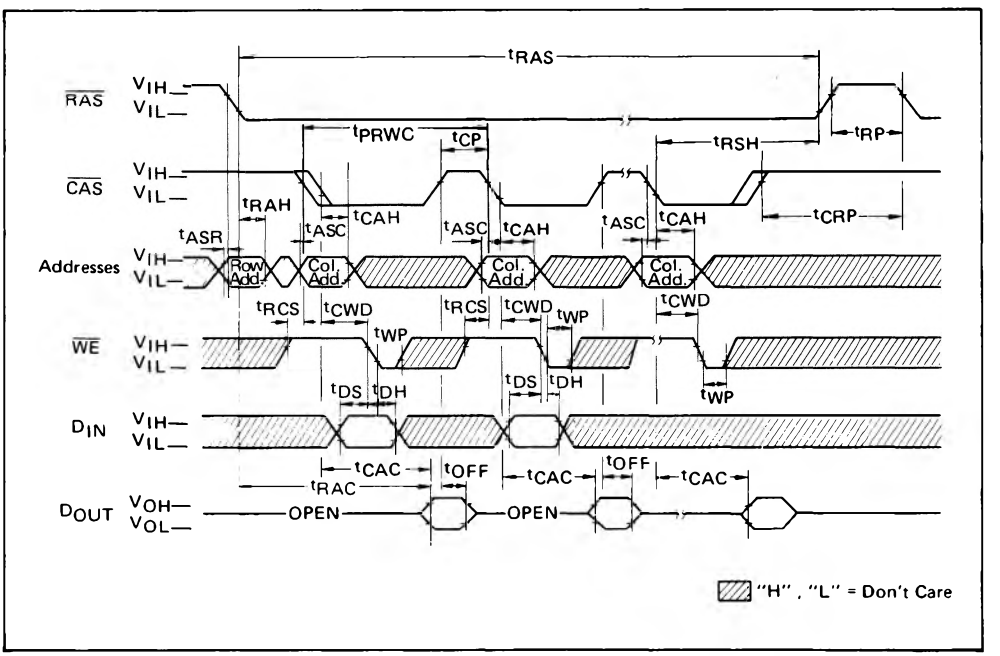

## PAGE MODE READ CYCLE



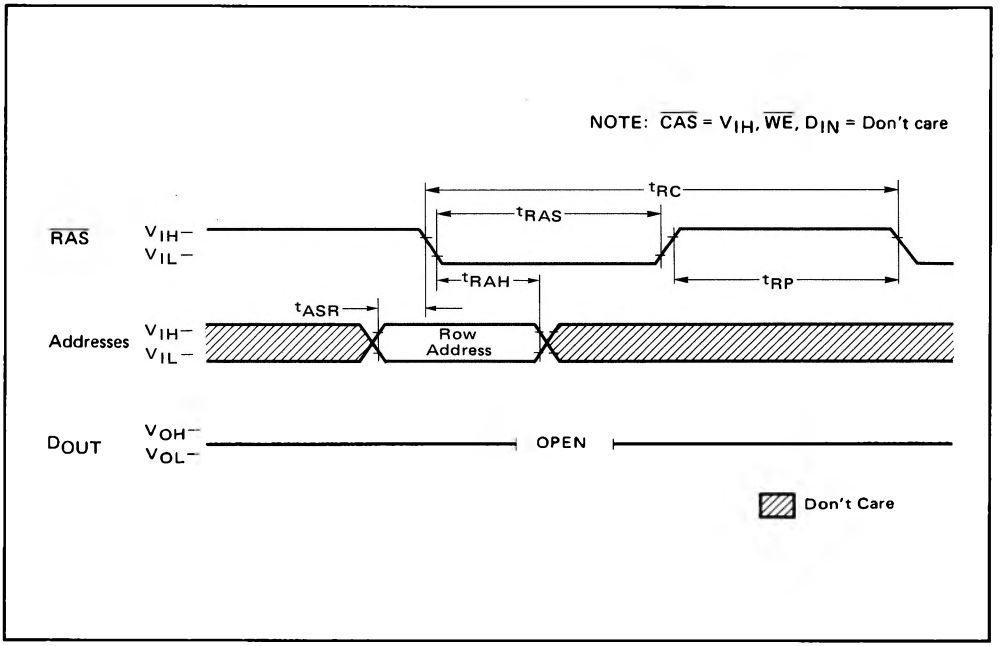
## PAGE MODE WRITE CYCLE



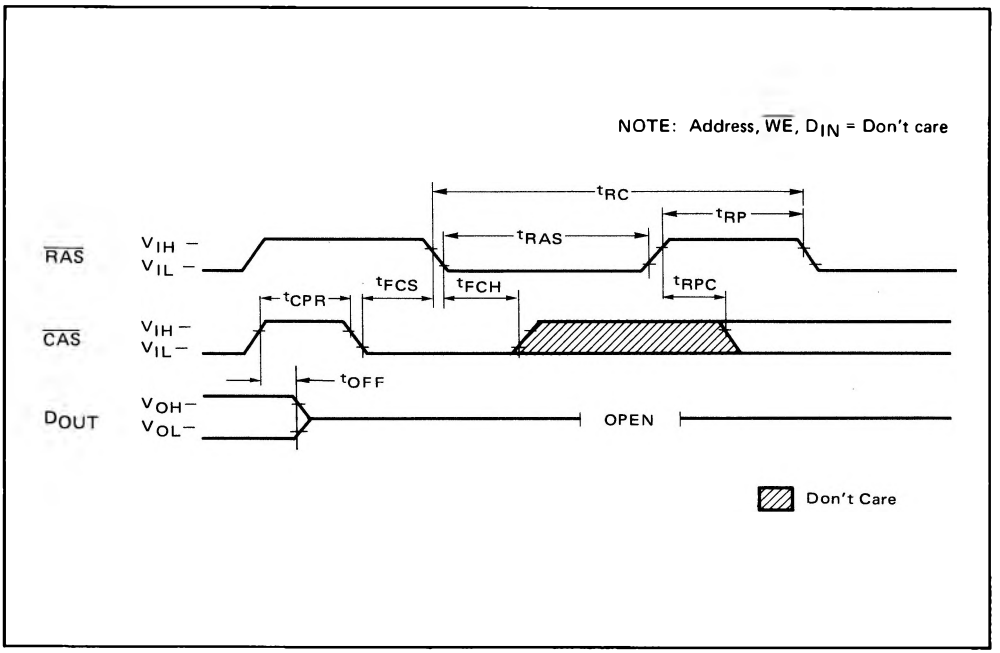

## PAGE MODE, READ-MODIFY-WRITE CYCLE



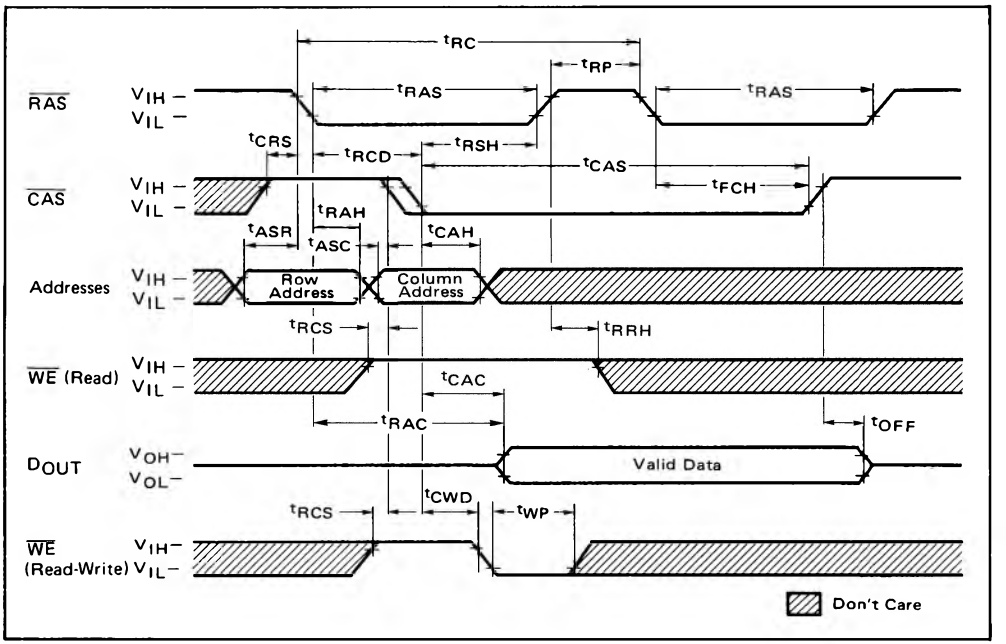
## $\overline{RAS}$ ONLY REFRESH CYCLE



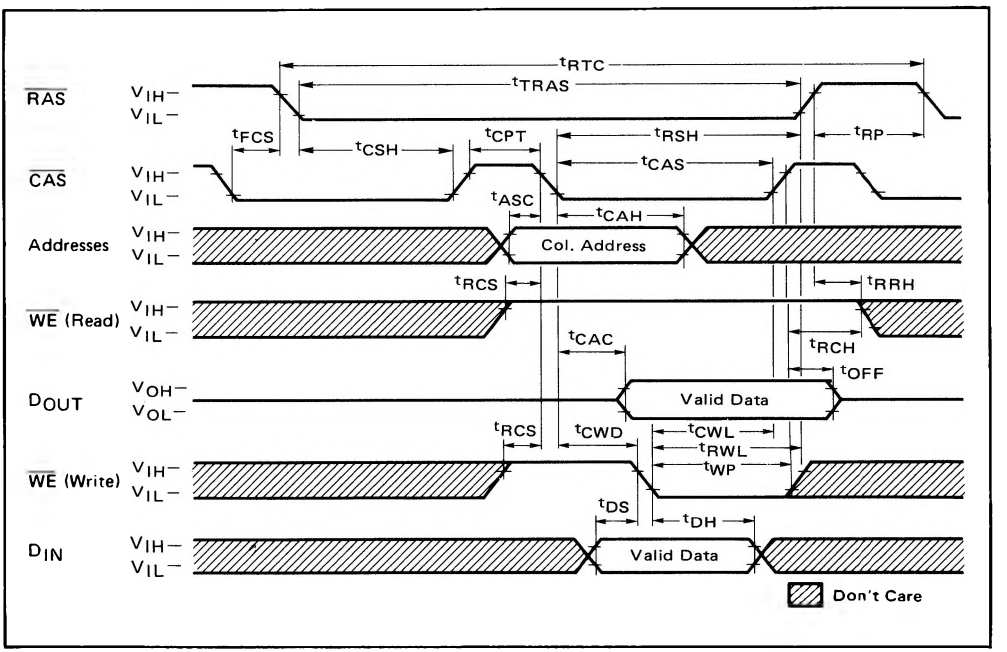

## $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



## HIDDEN REFRESH CYCLE




## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



## FUNCTIONAL DESCRIPTION

**Simple Timing Requirements:**

The MSM41256A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256A can operate under the condition of $t_{RCD}$ (max) = $t_{CAC}$ which provides an optimal time space for address multiplexing. In addition, the MSM41256A has the minimal hold time of Address ($t_{CAH}$), $\overline{WE}$ ($t_{WCH}$) and $D_{IN}$ ($t_{DH}$). And the MSM41256A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes $t_{AR}$, $t_{WCR}$, $t_{DHR}$ and $t_{RWD}$. Therefore, the hold times of the Column Address $D_{IN}$ and $\overline{WE}$ as well as $t_{CWD}$ ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by $t_{RCD}$.

**Fast Read- While-Write Cycle:**

The MSM41256A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41256A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after $t_{CWD}$ following $\overline{CAS}$ transition to low, the MSM41256A goes to delayed write mode where the output contains the data from the cell selected and the data from $D_{IN}$ is written into the cell selected. Therefore, very fast read write cycle becomes available.

**Address Inputs:**

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41256A. Nine row-address bits are established on the input pins ($A_0$ through $A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time ($t_{RAH}$) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

**Write Enable:**

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

**Data Input:**

Data is written into the MSM41256A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in ($D_{IN}$) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, $D_{IN}$ is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus $D_{IN}$ is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

**Data Output:**

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after $t_{RAC}$ from transition of $\overline{RAS}$ when $t_{RCD}$ (max) is satisfied, or after $t_{CAC}$ from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD}$ (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

**Page Mode:**

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

**$\overline{RAS}$ Only Refresh:**

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0$ to $A_7$) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses ($A_0$ to $A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

**$\overline{CAS}$ Before $\overline{RAS}$ Refresh:**

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period ($t_{FCS}$) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

**Hidden Refresh:**

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41256A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

**$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:**

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits $A_0$ through $A_7$ are defined by the refresh counter. The other bit $A_8$ is set "high" internally.
* A COLUMN ADDRESS
  - All the bits $A_0$ through $A_8$ are defined by latching levels on $A_0$ through $A_8$ at the second falling edge of CAS.

**Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:**

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

## MSM41256A Bit Map (Physical-Decimal)

□ Pin 16

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 256 | 256 | 256 | 256 | | 256 | 256 | 256 | 256 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 257 | 257 | 257 | 257 | | 257 | 257 | 257 | 257 |
| | | | | | | | | |
| | | | | | | | | |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 126 | 126 | 126 | 126 | | 126 | 126 | 126 | 126 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 382 | 382 | 382 | 382 | | 382 | 382 | 382 | 382 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 127 | 127 | 127 | 127 | | 127 | 127 | 127 | 127 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 383 | 383 | 383 | 383 | | 383 | 383 | 383 | 383 |

COLUMN DECODER

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 256 | 256 | 256 | 256 | | 256 | 256 | 256 | 256 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 1 | 1 | 1 | 1 | | 1 | 1 | 1 | 1 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 257 | 257 | 257 | 257 | | 257 | 257 | 257 | 257 |
| | | | | | | | | |
| | | | | | | | | |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 126 | 126 | 126 | 126 | | 126 | 126 | 126 | 126 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 382 | 382 | 382 | 382 | | 382 | 382 | 382 | 382 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 127 | 127 | 127 | 127 | | 127 | 127 | 127 | 127 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 383 | 383 | 383 | 383 | | 383 | 383 | 383 | 383 |

ROW DECODER

ROW DECODER

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 511 | 511 | 511 | 511 | | 511 | 511 | 511 | 511 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 255 | 255 | 255 | 255 | | 255 | 255 | 255 | 255 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 510 | 510 | 510 | 510 | | 510 | 510 | 510 | 510 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 254 | 254 | 254 | 254 | | 254 | 254 | 254 | 254 |
| | | | | | | | | |
| | | | | | | | | |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 385 | 385 | 385 | 385 | | 385 | 385 | 385 | 385 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 129 | 129 | 129 | 129 | | 129 | 129 | 129 | 129 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 384 | 384 | 384 | 384 | | 384 | 384 | 384 | 384 |
| 252 | 253 | 254 | 255 | | 3 | 2 | 1 | 0 |
| 128 | 128 | 128 | 128 | | 128 | 128 | 128 | 128 |

COLUMN DECODER

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 511 | 511 | 511 | 511 | | 511 | 511 | 511 | 511 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 255 | 255 | 255 | 255 | | 255 | 255 | 255 | 255 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 510 | 510 | 510 | 510 | | 510 | 510 | 510 | 510 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 254 | 254 | 254 | 254 | | 254 | 254 | 254 | 254 |
| | | | | | | | | |
| | | | | | | | | |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 385 | 385 | 385 | 385 | | 385 | 385 | 385 | 385 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 129 | 129 | 129 | 129 | | 129 | 129 | 129 | 129 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 384 | 384 | 384 | 384 | | 384 | 384 | 384 | 384 |
| 256 | 257 | 258 | 259 | | 511 | 510 | 509 | 508 |
| 128 | 128 | 128 | 128 | | 128 | 128 | 128 | 128 |

A8 ROW = "L"
REFRESH ADDRESS

(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS

(0 – 255)

□
Pin 8

| |
|---|
| A |
| B |

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)