OKI semiconductor

MSM2816ARS

2K x 8 BIT ELECTRICALLY ERASABLE PROM

GENERAL DESCRIPTION

The MSM2816A is a 2,048 word x 8 bit electrically erasable programmable read-only memory (E^2 PROM). The MSM2816A operates from a single 5V power supply, has a static standby mode, and features easiest programming. Though the MSM2816A requires no high voltage during reading or writing, it is still operable in the high-voltage mode as well.

The process of updating byte data in the 5V programming mode is initiated by setting the write signal at the TTL low (L) level for 200 ns. Address and data bus information is latched within the IC, and the system is made available to other tasks during the write cycle.
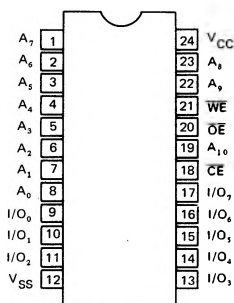
The MSM2816A erases a selected byte automatically before writing new information to it. The erase/write cycle completes within a maximum period of 10 ms. In addition to the byte erase/write function, the MSM2816A supports a mode permitting the entire chip to be cleared at 10 ms or less.

The MSM2816A is ideally suited for applications involving the use of a nonvolatile memory to make modifications to a system. Typical applications include self-controllable equipments, memorizing ratio of tariffs at terminals on the sales counter, storing keywords for encoding data, programmable character generators, and storing map information in air navigation systems.
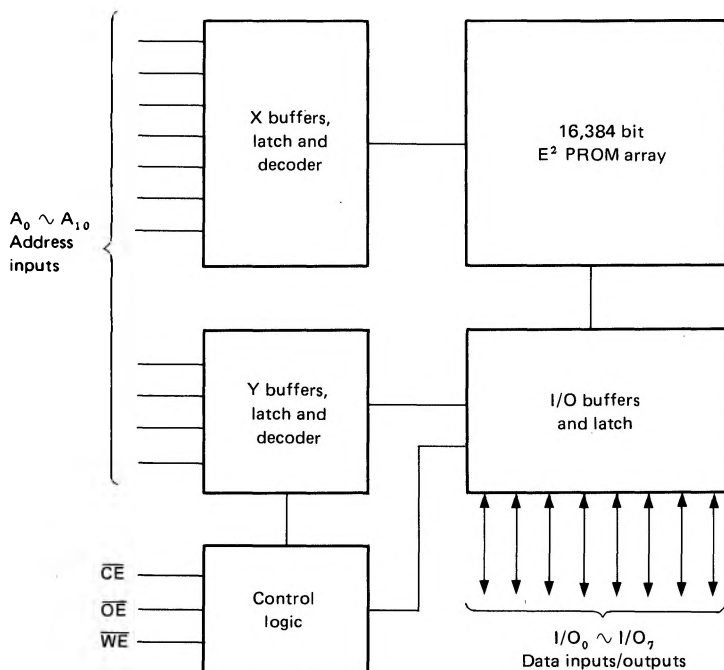
FEATURES

- Single 5V power supply
- High-speed access time . . . . 250 ns MAX.
  - 300 ns MAX.
  - 350 ns MAX.
  - 450 ns MAX.
- TTL level byte write . . . . 10 ms MAX.
- Internally latched address data during write

- Automatic erase before write
- Automatic completion of write
- Inadvertent write protection
- Input and output TTL compatible
- JEDEC-compliance pin configuration
- Pin compatible to Xicor 2816A, Intel 2816/2816A

PIN CONFIGURATION (Top View)

	24-pin DIP	
A_7	1	24 V_{CC}
A_6	2	23 A_8
A_5	3	22 A_9
A_4	4	21 $\overline{WE}$
A_3	5	20 $\overline{OE}$
A_2	6	19 A_{10}
A_1	7	18 $\overline{CE}$
A_0	8	17 I/O_7
I/O_0	9	16 I/O_6
I/O_1	10	15 I/O_5
I/O_2	11	14 I/O_4
V_{SS}	12	13 I/O_3

Pin names	Function
$A_0 \sim A_{10}$	Address inputs
$I/O_0 \sim I/O_7$	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM

```
                                    ┌──────────────────┐
         ┌────────────────┐         │                  │
         │  X buffers,    │         │   16,384 bit     │
         │  latch and     │─────────│   E² PROM array  │
         │  decoder       │         │                  │
         └────────────────┘         └──────────────────┘
A₀ ∿ A₁₀
Address
inputs
         ┌────────────────┐         ┌──────────────────┐
         │  Y buffers,    │         │                  │
         │  latch and     │─────────│   I/O buffers    │
         │  decoder       │         │   and latch      │
         └────────────────┘         └──────────────────┘

CE ───┐  ┌────────────────┐
OE ───┼──│  Control       │            I/O₀ ∿ I/O₇
WE ───┘  │  logic         │         Data inputs/outputs
         └────────────────┘
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$A_0 \sim A_{10}$ Address inputs

$\overline{CE}$ $\overline{OE}$ $\overline{WE}$

16,384 bit E^2 PROM array

$I/O_0 \sim I/O_7$ Data inputs/outputs

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power	
V_{IH}	X	X	Standby	High Z	Standby	
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active	
V_{IL}	V_{IH}	⎍	5V byte write	D_{IN}	Active	
V_{IL}	V_{IH}	V_{IH}	Program (READ AND WRITE) inhibit	High Z	Active	
V_{IL}	V_{IH}	V_{PP}	Byte erase	$D_{IN}=V_{IH}$	Active	High-voltage program-ming mode
V_{IL}	V_{IH}	V_{PP}	Byte write	D_{IN}	Active	
V_{IL}	V_{OE}	V_{PP}	Chip erase	$D_{IN}=V_{IH}$	Active	

Note: X; Don't care (V_{IH} or V_{IL})

DEVICE OPERATION

Read Mode

Data in the MSM2816A can be read by applying a TTL high signal to $\overline{WE}$, and a low signal to $\overline{CE}$ and $\overline{OE}$. The data for t_{AA} time from address inputs, for t_{CE} time from a low on $\overline{OE}$, and for t_{OE} from a low on $\overline{OE}$, whichever occurs last, is valid. Once a TTL high signal is applied to $\overline{OE}$ or $\overline{CE}$, the I/O pins are in a high impedance state to prevent data bus contention within the system.

Write Mode

The MSM2816A has two write modes:

● 5V programming mode (standard)

In this mode, a write cycle is initiated by applying a TTL low signal to $\overline{WE}$ and $\overline{CE}$ and a high signal to $\overline{OE}$. Address inputs are latched on the trailing edge of $\overline{WE}$ or $\overline{CE}$ whichever is the slower. Data on the I/O pins is latched on the leading edge of $\overline{WE}$ or $\overline{CE}$. The address and data are latched for 200 ns by using TTL level write signal. Once the data is latched, the MSM2816A erases the byte that is selected within 10 ms automatically and writes new data to it.

In the meantime, the system is available to other tasks, but the I/O pins are in a high impedance state while writing is in progress. The system recognizes the completion of a write operation by comparing the data last written against previous data. When this method of verification is to be used, the output may be pulled up to V_{CC} with a resistor so that all read data prior to the completion of the write operation should be '1'.

● High-voltage programming mode

While the MSM2816A merely requires a single 5V power supply to write, it is also operable in the high-voltage mode to remain compatible with existing E^2 PROMs. In this mode, all selected bytes must be erased before new data can be written to them. The byte erase operation can be initiated the same way as a high-voltage write operation, except that a TTL

high level is applied to every I/O pin. To be able to write new data to a byte in the high-voltage mode, it is necessary to apply a TTL high level to $\overline{OE}$ and a TTL low level to $\overline{CE}$ before $\overline{WE}$ is raised to a voltage (Vpp) between 12V and 22V. The MSM2816A has no constrain on Vpp rising or falling edges, and data present on the I/O pins is written to memory within a maximum period of 9 ms from address inputs.

High-voltage Chip Erase

The data in all memory cells is erased within 9 ms when $\overline{OE}$ is initially raised to 12-22V, then $\overline{WE}$ is raised to 12-22V while applying a TTL high signal to every I/O pin. After the erasure, all data bits in the device are set to TTL high level (logic '1').

Standby Mode

The 2816A has a standby mode which reduces the active power dissipation by about 55% when a TTL high level is applied to $\overline{CE}$.

● Number of repetitive write cycles

The MSM2816A is designed to support applications requiring up to 10,000 write cycles per byte.

● Inadvertent write protection

The MSM2816A has following four functions to prevent inadvert write during power up, power down, and during line noise occurrence.

(1) V_{CC} level detection

Writing to the device is automatically inhibited when V_{CC} has fallen to 3.0V or below.

(2) Time delay

Any write operation is automatically inhibited while V_{CC} is 5-20 ms in the Vwl state when the MSM2816A is being powered up.

This features allows sufficient time for the system to apply a TTL high signal to $\overline{WE}$ or $\overline{CE}$ before write occurs.

(3) $\overline{OE}$ gating

The MSM2816A inhibits all write operations while $\overline{OE}$ is low.

(4) $\overline{WE}$ noise protection

No write cycle may be initiated by write pulses for 20 ns or shorter.

ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings (Note 1)

Ambient temperature under bias	$-10°C \sim +85°C$
Storage temperature	$-65°C \sim +125°C$
Voltage on any pin with respect to ground (Note 2)	$-0.5V \sim +6V$
DC output current	5 mA
$\overline{OE}$ and $\overline{WE}$ voltage in high-voltage mode	22.5V

Notes: 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. The device incorporates a special circuit to safeguard it against electrostatic damage. For added assurance, avoid operating the device above the maximum ratings indicated.

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C $\sim$ 70°C)

Parameter	Symbol	Condition	Limits		Unit
			MIN	MAX	
Input low voltage	V_{IL}		—	0.8	V
Input high voltage	V_{IH}		2.0	—	V
Output low voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	V
Output high voltage	V_{OH}	I_{OH} = –400 μA	2.4	—	V
Write inhibit V_{CC} voltage	V_{WI}		3.0	3.5	V
$\overline{WE}$ voltage (erase/write) (Note 1)	V_{PP}		12	22	V
$\overline{OE}$ voltage (chip erase) (Note 1)	V_{OE}		12	22	V
Vpp current (byte erase/write) (Note 1)	$I_{PP(W)}$	$\overline{CE}$ = V_{IL}	—	10	μA
Vpp current (inhibit) (Note 1)	$I_{PP(I)}$	V_{PP} = 22V, CE = V_{IH}	—	10	μA
Vpp current (chip erase) (Note 1)	$I_{PP(C)}$		—	10	μA
V_{OE} current (chip erase) (Note 1)	I_{OE}	V_{OE} = V_{PP} = 22V	—	10	μA
Input leakage current	I_{LI}	V_{IN} = 0 $\sim$ 5.25V	—	10	μA
Output leakage current	I_{LO}	V_{OUT} = 0 $\sim$ 5.25V	—	±10	μA
Operating supply current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O S = OPEN Other pins = 5.25V	—	110	mA
Standby supply current	I_{SB}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O S = OPEN Other pins = 5.25V	—	40	mA

Note 1:   These parameters apply only in the high-voltage programming mode.

CAPACITANCE
(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)
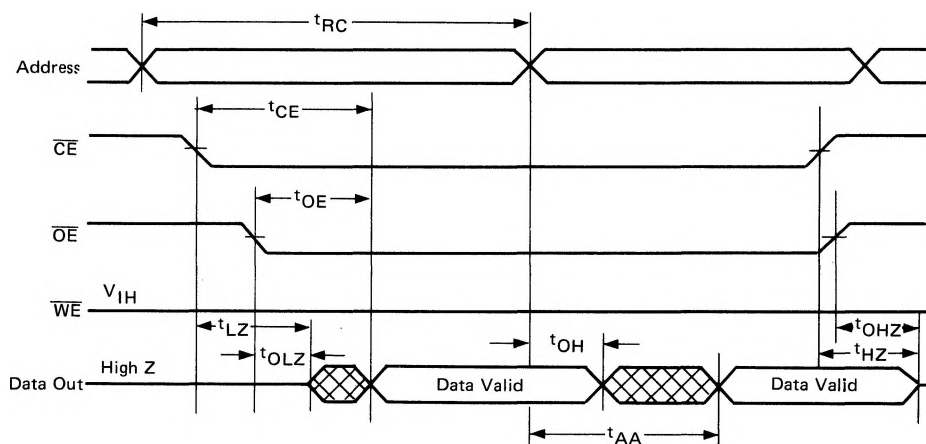
Parameter	Symbol	Conditions	MAX	Unit
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF
Input capacitance	C_{IN}	V_{IN} = 0V	6	pF

AC CHARACTERISTICS (Note 1)

(1) Read cycle

(V_{CC} = 5V ±5%, Ta = 0°C ∿ 70°C)

| Parameter	Symbol	MSM2816A -250		MSM2816A -300		MSM2816A -350		MSM2816A -450		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read cycle time	t_{RC}	250	—	300	—	350	—	450	—	ns
Chip enable access time	t_{CE}	—	250	—	300	—	350	—	450	ns
Address access time	t_{AA}	—	250	—	300	—	350	—	450	ns
Output enable access time	t_{OE}	—	100	—	120	—	135	—	150	ns
Output set time ($\overline{CE}$)	t_{LZ}	10	—	10	—	10	—	10	—	ns
Output disable time ($\overline{CE}$)	t_{HZ}	10	100	10	100	10	100	10	100	ns
Output set time ($\overline{OE}$)	t_{OLZ}	10	—	10	—	10	—	10	—	ns
Output disable time ($\overline{OE}$)	t_{OHZ}	10	70	10	80	10	100	10	100	ns
Output hold time	t_{OH}	20	—	20	—	20	—	20	—	ns

Note 1: AC test conditions

Input pulse voltage level : 0 ∿ 3V
Pulse rise/fall time : 10 ns
Input/output timing level : 1.5V
Load conditions : 1 TTL, CL = 100 pF.

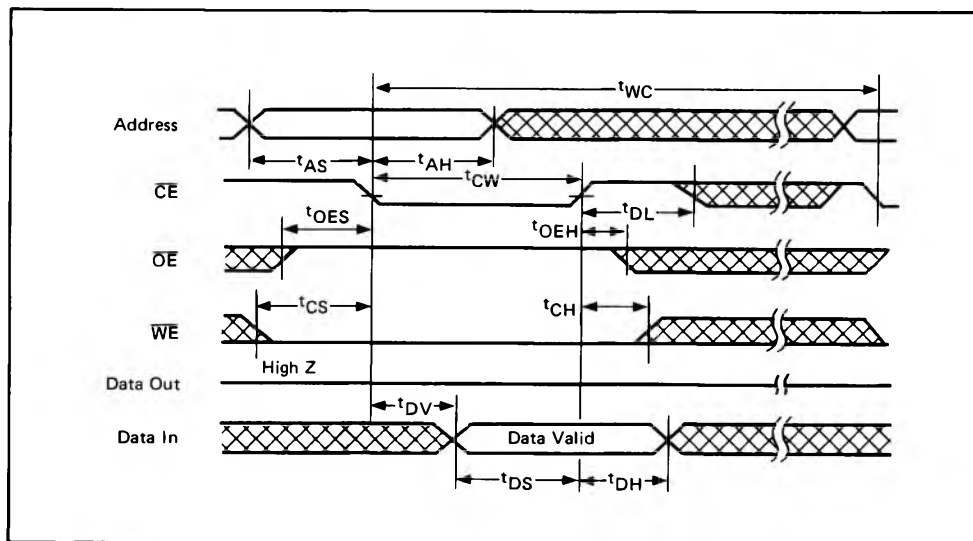## (2) Write cycle (5V programming mode)

(V_{CC} = 5V ±5%, Ta = 0°C $\sim$ 70°C)

Parameter	Symbol	Limits		Unit
		MIN	MAX	
Write cycle time	t_{WC}	10	–	ms
Address setup time	t_{AS}	10	–	ns
Address hold time	t_{AH}	70	–	ns
Write setup time	t_{CS}	0	–	ns
Write hold time	t_{CH}	0	–	ns
Write pulse width ($\overline{CE}$)	t_{CW}	150	–	ns
Output enable setup time	t_{OES}	10	–	ns
Output enable hold time	t_{OEH}	10	–	ns
Write pulse width ($\overline{WE}$) (Note 1)	t_{WP}	150	–	ns
Data latch time	t_{DL}	50	–	ns
Data valid time (Note 2)	t_{DV}	–	1	μs
Data setup time	t_{DS}	50	–	ns
Data hold time	t_{DH}	10	–	ns
Write inhibit time during power-up	t_{INIT}	5	20	ms

● $\overline{WE}$ control write cycle
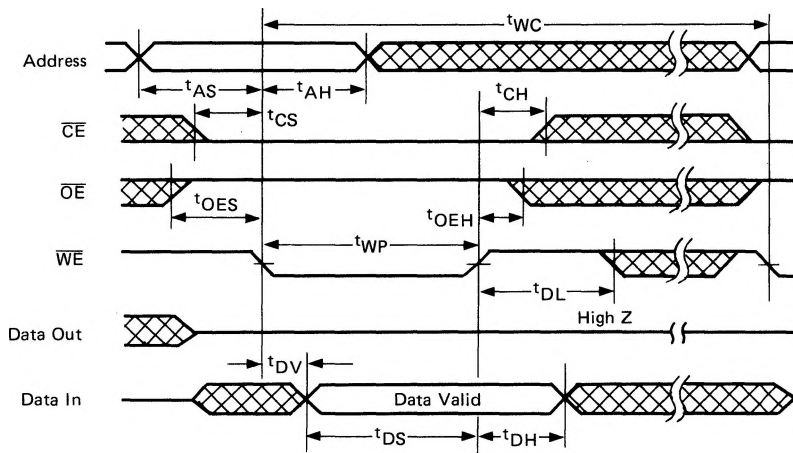
● CE control write cycle


Notes: 1. WE is noise protected. No write cycle may be initiated by write pulses for 20 ns or shorter.
       2. Data must be set valid within 1 μs after the start of a write cycle.

## (3) Write/erase cycle (High-voltage programming mode)

(V_{CC} = 5V ±5%, Ta = 0°C $\sim$ 70°C)

Parameter	Symbol	Conditions	Limits		Unit
			MIN	MAX	
Vpp address setup time	t_{AS}		10	—	ns
Vpp CE setup time	t_{CS}		10	—	ns
Vpp data setup time	t_{DS}		0	—	ns
Data hold time	t_{CH}	V_{PP} = 6V	50	—	ns
Write pulse width	t_{WP}	V_{PP} = 12V	9	70	ms
Write recovery time	t_{WR}	V_{PP} = 6V	50	—	ns
Chip erase setup time	t_{OS}	V_{PP} = 6V, V_{OE} = 12V	10	—	ns
Chip erase hold time	t_{OH}	V_{PP} = 6V, V_{OE} = 12V	10	—	ns
Vpp OE setup time	t_{BOS}	V_{PP} = 6V	10	—	ns
Vpp OE hold time	t_{BOH}	V_{PP} = 6V	10	—	ns
Write inhibit time during power-up	t_{INIT}	$V_{CC} > V_{WI}$	5	20	ms

● Byte erase/write cycle
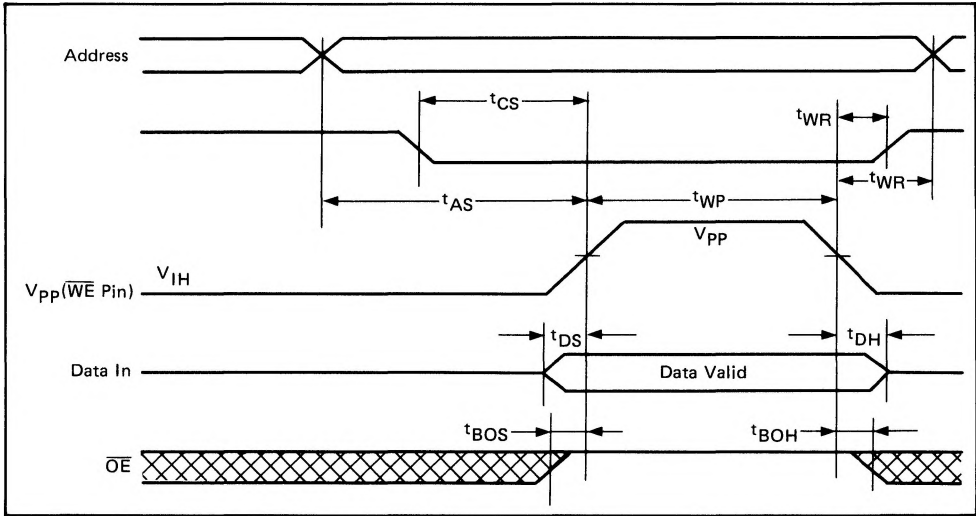
● Chip erase cycle
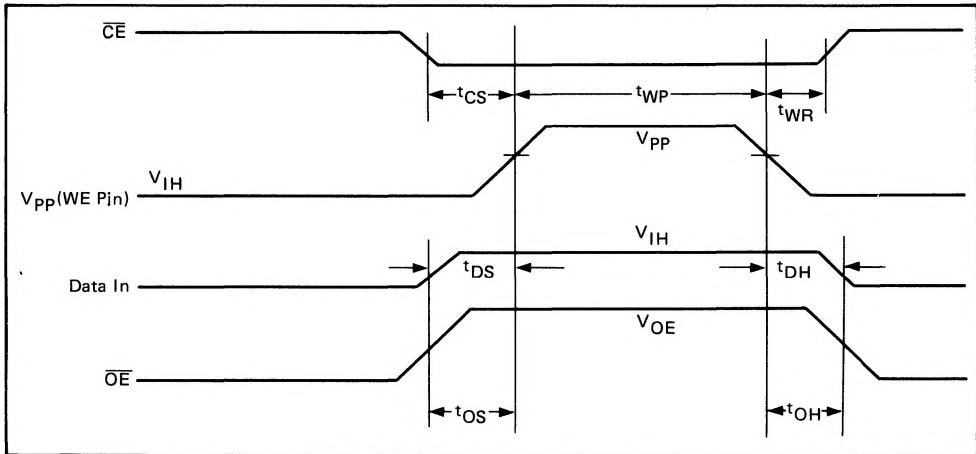
PRODUCT INFORMATION

Model name	Access time	Operating temperature	Package
MSM2816A AS-250	250		
MSM2816A AS-300	300	0 ∿ 70°C	Cerdip
MSM2816A AS-350	350		
MSM2816A AS-450	450		
MSM2816A RS-250	250		
MSM2816A RS-300	300	0 ∿ 70°C	Plastic
MSM2816A RS-350	350		
MSM2816A RS-450	450		