Advance Information

MPC755EC/D
Rev. 6, 9/2002

MPC755
RISC Microprocessor
Hardware Specifications

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This document is primarily concerned with the MPC755; however, unless otherwise noted, all information here also applies to the MPC745. The MPC755 and MPC745 are reduced instruction set computing (RISC) microprocessors that implement the PowerPC instruction set architecture. This document describes pertinent physical characteristics of the MPC755. For functional characteristics of the processor, refer to the *MPC750 RISC Microprocessor Family User's Manual*.

This document contains the following topics:

To locate any published errata or updates for this document, refer to the website at http://www.motorola.com/semiconductors.

1.1 Overview

The MPC755 is targeted for low-cost, low-power systems and supports the following power management features—doze, nap, sleep, and dynamic power management. The MPC755 consists of a processor core and an internal L2 tag combined with a dedicated L2 cache interface and a 60x bus. The MPC745 is identical to the MPC755 except it does not support the L2 cache interface.

Figure 1 shows a block diagram of the MPC755.

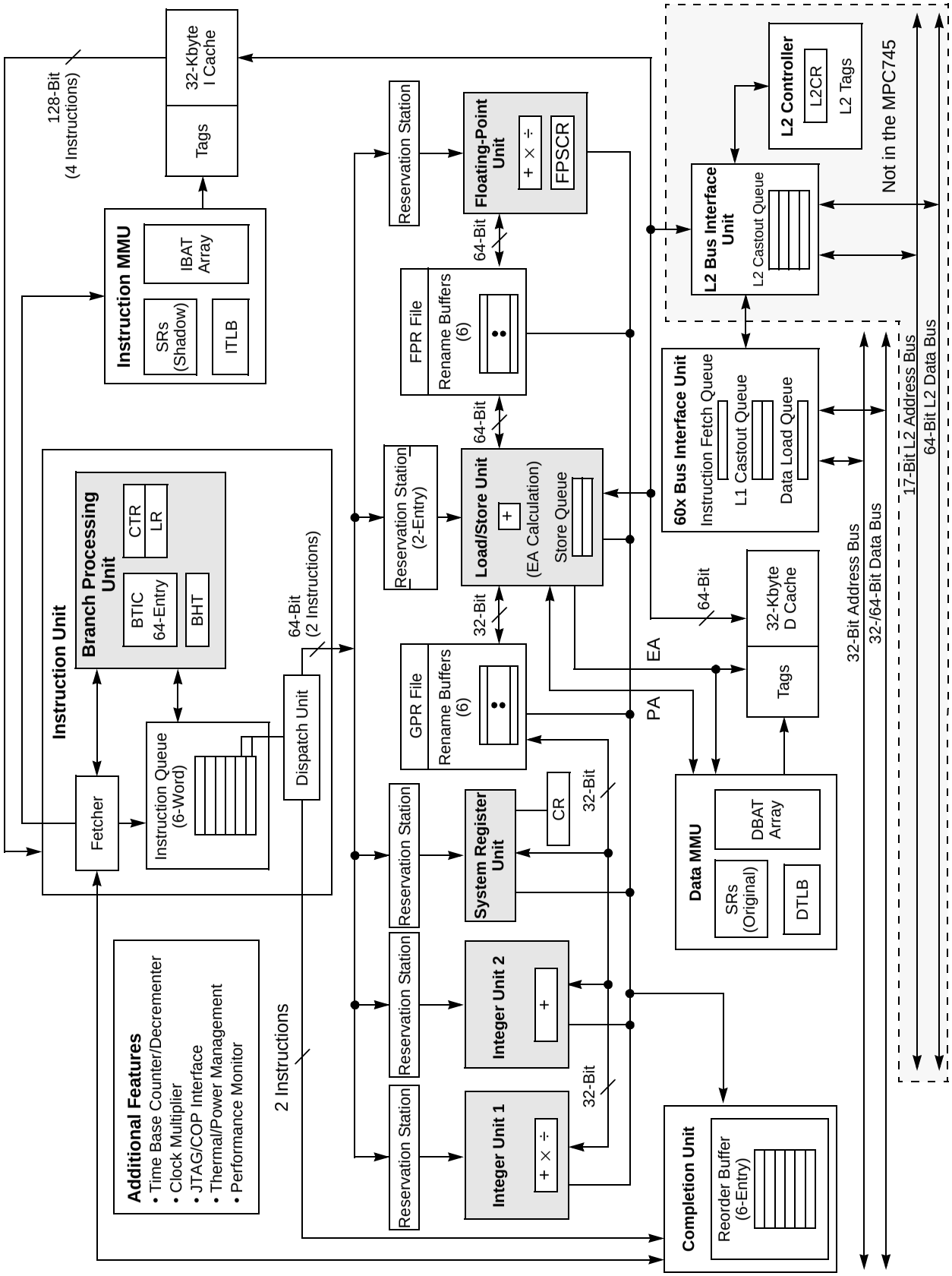


Figure 1. MPC755 Block Diagram

1.2 Features

This section summarizes features of the MPC755 implementation of the PowerPC architecture. Major features of the MPC755 are as follows:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, four-way set-associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - Six-entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization, and all instruction flow changes
- Fixed point units (FXUs) that share 32 GPRs for integer operands
  - Fixed Point Unit 1 (FXU1)—multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)—shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point unit and a 32-entry FPR file
  - Support for IEEE standard 754 single- and double-precision floating-point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
  - Three-cycle latency, one-cycle throughput, single-precision multiply-add

  - Three-cycle latency, one-cycle throughput, double-precision add
  - Four-cycle latency, two-cycle throughput, double-precision multiply-add
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/store unit
  - One-cycle load or store cache access (byte, half-word, word, double word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big- and little-endian byte addressing supported
- Level 1 cache structure
  - 32K, 32-byte line, eight-way set-associative instruction cache (iL1)
  - 32K, 32-byte line, eight-way set-associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently-used (PLRU) replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - MEI data cache coherency maintained in hardware
  - Nonblocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) cache interface (not implemented on MPC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1 Mbyte two-way set-associative L2 cache support
  - Copy-back or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode
  - 64-byte (256K/512K) or 128-byte (1M) sectored line size
  - Supports flow through (register-buffer) synchronous BurstRAMs, pipelined (register-register) synchronous BurstRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late write synchronous BurstRAMs
  - L2 configurable to cache, private memory, or split cache/private memory
  - Core-to-L2 frequency divisors of ÷1, ÷1.5, ÷2, ÷2.5, and ÷3 supported
  - 64-bit data bus

  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both L2 address and data
- Memory management unit
  - 128-entry, two-way set-associative instruction TLB
  - 128-entry, two-way set-associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - Eight instruction BATs and eight data BATs
  - Eight SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 exabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus interface
  - Compatible with 60x processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5 and 3.3 V
  - Parity checking on both address and data buses
- Power management
  - Low-power design with thermal requirements very similar to MPC740/MPC750
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Integrated thermal management assist unit
  - On-chip thermal sensor and control logic
  - Thermal management interrupt for software regulation of junction temperature
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface

1.3 General Parameters

The following list provides a summary of the general parameters of the MPC755:

Technology	0.22 µm CMOS, six-layer metal
Die size	6.61 mm × 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static

Packages	MPC745: Surface mount 255 plastic ball grid array (PBGA) MPC755: Surface mount 360 ceramic ball grid array (CBGA) Surface mount 360 plastic ball grid array (PBGA)
Core power supply	2.0 V ± 100 mV DC (nominal; some parts support core voltages down to 1.8 V; see Table 3 for recommended operating conditions)
I/O power supply	2.5 V ± 100 mV DC or 3.3 V ± 165 mV DC (input thresholds are configuration pin selectable)

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC755.

1.4.1 DC Electrical Characteristics

Table 1 through Table 7 describe the MPC755 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic		Symbol	Maximum Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 2.5	V	4
PLL supply voltage		AV_{DD}	–0.3 to 2.5	V	4
L2 DLL supply voltage		$L2AV_{DD}$	–0.3 to 2.5	V	4
Processor bus supply voltage		OV_{DD}	–0.3 to 3.6	V	3
L2 bus supply voltage		$L2OV_{DD}$	–0.3 to 3.6	V	3
Input voltage	Processor bus	V_{in}	–0.3 to OV_{DD} + 0.3 V	V	2, 5
	L2 bus	V_{in}	–0.3 to $L2OV_{DD}$ + 0.3 V	V	2, 5
	JTAG signals	V_{in}	–0.3 to 3.6	V	
Storage temperature range		T_{stg}	–55 to 150	°C	

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{in} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3 V at any time including during power-on reset.
3. **Caution:** $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6 V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3 V for up to 20 ms, or by 2.5 V for up to 40 ms. Excursions beyond 3.3 V or 40 ms are not supported.
4. **Caution:** $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4 V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0 V for up to 20 ms, or by 0.7 V for up to 40 ms. Excursions beyond 1.0 V or 40 ms are not supported.
5. This is a DC specifications only. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

Figure 2 shows the allowable undershoot and overshoot voltage on the MPC755.

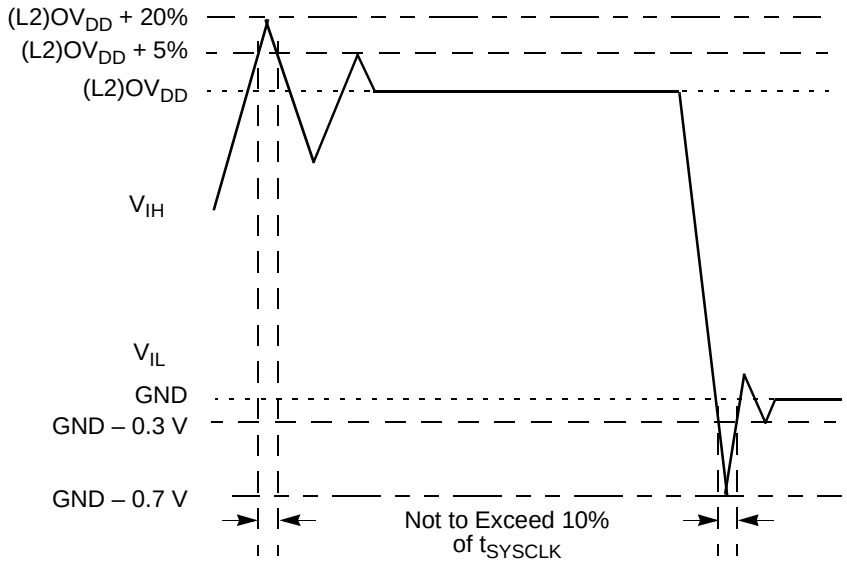


Figure 2. Overshoot/Undershoot Voltage

The MPC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The MPC755 core voltage must always be provided at nominal 2.0 V (see Table 3 for actual recommended core voltage). Voltage to the L2 I/Os and processor interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 2. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 2 describes the input threshold voltage setting.

Table 2. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5 V/3.3 V	1	2.5 V/3.3 V

Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
Note: The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, refer to Section 1.10.2, “Part Numbers Not Fully Addressed by This Document.”

Table 3 provides the recommended operating conditions for the MPC755.

Table 3. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value				Unit	Notes
			300 MHz, 350 MHz		400 MHz			
			Min	Max	Min	Max		
Core supply voltage		V_{DD}	1.80	2.10	1.90	2.10	V	3
PLL supply voltage		AV_{DD}	1.80	2.10	1.90	2.10	V	3
L2 DLL supply voltage		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V	3
Processor bus supply voltage	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
L2 bus supply voltage	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V	2, 4
			3.135	3.465	3.135	3.465		5
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
	L2 bus	V_{in}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V	
	JTAG signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V	
Die-junction temperature		T_j	0	105	0	105	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support. For more information, refer to Section 1.10.2, “Part Numbers Not Fully Addressed by This Document.”
3. 2.0 V nominal.
4. 2.5 V nominal.
5. 3.3 V nominal.

Table 4 provides the package thermal characteristics for the MPC755 and MPC745. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Motorola recommends use of a PBGA package except where circumstances dictate use of a CBGA package. The MPC745 is offered in a PBGA package only.

Table 4. Package Thermal Characteristics [6]

Characteristic	Symbol	Value			Unit	Notes
		MPC755 CBGA	MPC755 PBGA	MPC745 PBGA		
Junction-to-ambient thermal resistance, natural convection	$R_{\theta JA}$	24	31	34	°C/W	1, 2
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{\theta JMA}$	17	25	26	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, single-layer (1s) board	$R_{\theta JMA}$	18	25	27	°C/W	1, 3
Junction-to-ambient thermal resistance, 200 ft/min airflow, four-layer (2s2p) board	$R_{\theta JMA}$	14	21	22	°C/W	1, 3
Junction-to-board thermal resistance	$R_{\theta JB}$	8	17	17	°C/W	4
Junction-to-case thermal resistance	$R_{\theta JC}$	<0.1	<0.1	<0.1	°C/W	5

Notes:
1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of $R_{\theta JC}$ for the part is less than 0.1°C/W.
6. Refer to Section 1.8.8, “Thermal Management Information,” for more details about thermal management.

The MPC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor Family User’s Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 5. Thermal Sensor Specifications

At recommended operating conditions (see Table 3)

Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	µs	2, 3
Resolution	4	—	°C	3
Accuracy	–12	+12	°C	3

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Motorola Application Note AN1800/D, *Programming the Thermal Assist Unit in the MPC750 Microprocessor.*
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the MPC755.

Table 6. DC Electrical Specifications

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	2.5	V_{IH}	1.6	$(L2)OV_{DD}$ + 0.3	V	2, 3
	3.3	V_{IH}	2.0	$(L2)OV_{DD}$ + 0.3	V	2, 3
Input low voltage (all inputs except SYSCLK)	2.5	V_{IL}	–0.3	0.6	V	2
	3.3	V_{IL}	–0.3	0.8	V	
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V	
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V	
SYSCLK input low voltage	2.5	KV_{IL}	–0.3	0.4	V	
	3.3	KV_{IL}	–0.3	0.4	V	
Input leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$		I_{in}	—	10	µA	2, 3
High-Z (off-state) leakage current, $V_{in} = L2OV_{DD}/OV_{DD}$		I_{TSI}	—	10	µA	2, 3, 5
Output high voltage, I_{OH} = –6 mA	2.5	V_{OH}	1.7	—	V	
	3.3	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	—	0.45	V	
	3.3	V_{OL}	—	0.4	V	

Table 6. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 3)

Characteristic	Nominal Bus Voltage [1]	Symbol	Min	Max	Unit	Notes
Capacitance, V_{in} = 0 V, f = 1 MHz		C_{in}	—	5.0	pF	3, 4

Notes:
1. Nominal voltages; see Table 3 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while $L2OV_{DD}$ is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or –5%).

Table 7 provides the power consumption for the MPC755.

Table 7. Power Consumption for MPC755

	Processor (CPU) Frequency			Unit	Notes
	300 MHz	350 MHz	400 MHz		
Full-Power Mode					
Typical	3.1	3.6	5.4	W	1, 3, 4
Maximum	4.5	5.3	8.0	W	1, 2
Doze Mode					
Maximum	1.8	2.0	2.3	W	1, 2, 4
Nap Mode					
Maximum	1.0	1.0	1.0	W	1, 2, 4
Sleep Mode					
Maximum	550	550	550	mW	1, 2, 4
Sleep Mode (PLL and DLL Disabled)					
Maximum	510	510	510	mW	1, 2

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically <10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 3) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 3) and 65°C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC755. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0:3] signals. Parts are sold by maximum processor core frequency; see Section 1.10, “Ordering Information.”

1.4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 3.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 3)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit	Notes
		300 MHz		350 MHz		400 MHz			
		Min	Max	Min	Max	Min	Max		
Processor frequency	f_{core}	200	300	200	350	200	400	MHz	1
VCO frequency	f_{VCO}	400	600	400	700	400	800	MHz	1
SYSCLK frequency	f_{SYSCLK}	25	100	25	100	25	100	MHz	1
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns	
SYSCLK rise and fall time	t_{KR}, t_{KF}	—	2.0	—	2.0	—	2.0	ns	2
	t_{KR}, t_{KF}	—	1.4	—	1.4	—	1.4	ns	2
SYSCLK duty cycle measured at $OV_{DD}/2$	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%	3
SYSCLK jitter		—	±150	—	±150	—	±150	ps	3, 4
Internal PLL relock time		—	100	—	100	—	100	µs	3, 5

Notes:

1. **Caution:** The SYSCLK frequency and PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 1.8.1, “PLL Configuration,” for valid PLL_CFG[0:3] settings.
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1 V/ns is equivalent to a 2 ns maximum rise/fall time measured at 0.4 and 2.4 V (OV_{DD} = 3.3 V) or a rise/fall time of 1 ns measured at 0.4 and 1.8 V (OV_{DD} = 2.5 V).
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter—short term and long term combined—and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 3 provides the SYSCLK input timing diagram.

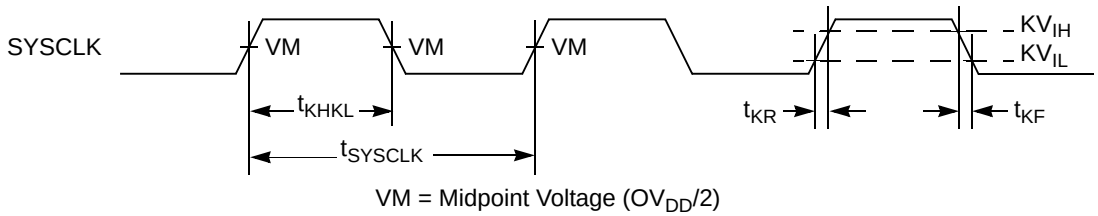


Figure 3. SYSCLK Input Timing Diagram

1.4.2.2 Processor Bus AC Specifications

Table 9 provides the processor bus AC timing specifications for the MPC755 as defined in Figure 4 and Figure 6. Timing specifications for the L2 bus are provided in Section 1.4.2.3, "L2 Clock AC Specifications."

Table 9. Processor Bus Mode Selection AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol [2]	All Speed Grades		Unit	Notes
		Min	Max		
Mode select input setup to $\overline{\text{HRESET}}$	t_{MVRH}	8	—	t_{sysclk}	3, 4, 5, 6, 7
$\overline{\text{HRESET}}$ to mode select input hold	t_{MXRH}	0	—	ns	3, 4, 6, 7, 8

Notes:

1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50-Ω load (see Figure 5). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK (K) going high (H) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH)—note the position of the reference and its state for inputs—and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX).
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
5. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0:3], and $\overline{\text{TLBISYNC}}$.
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 4 provides the mode select input timing diagram for the MPC755.

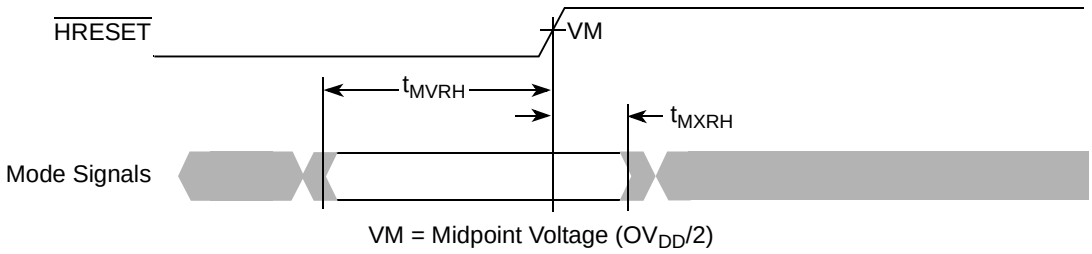


Figure 4. Mode Input Timing Diagram

Figure 5 provides the AC test load for the MPC755.

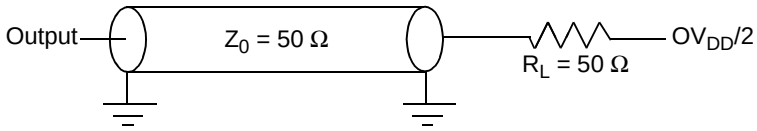


Figure 5. AC Test Load

Table 10. Processor Bus AC Timing Specifications [1]

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
Setup times: All inputs	t_{IVKH}	2.5	—	ns	
Input hold times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	—	ns	6
Input hold times: All inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	—	ns	6
Valid times: All outputs	t_{KHOV}	—	4.1	ns	
Output hold times: All outputs	t_{KHOX}	1.0	—	ns	
SYSCLK to output enable	t_{KHOE}	0.5	—	ns	2
SYSCLK to output high impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)	t_{KHOZ}	—	6.0	ns	2
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ high impedance after precharge	t_{KHABPZ}	—	1.0	t_{sysclk}	2, 3, 4
Maximum delay to $\overline{\text{ARTRY}}$ precharge	t_{KHARP}	—	1	t_{sysclk}	2, 3, 5

Table 10. Processor Bus AC Timing Specifications [1] (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	t_{KHARPZ}	—	2	t_{sysclk}	2, 3, 5

Notes:

1. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 1.10.2, “Part Numbers Not Fully Addressed by This Document.”
2. Guaranteed by design and characterization.
3. t_{sysclk} is the period of the external clock (SYSCLK) in ns. The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$, and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low, then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ is $0.5 \times t_{sysclk}$, that is, less than the minimum t_{sysclk} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following $\overline{\text{AACK}}$ will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is $1.0\ t_{sysclk}$; that is, it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.
6. $\overline{\text{MCP}}$ and $\overline{\text{SRESET}}$ must be held asserted for a minimum of two bus clock cycles; $\overline{\text{INT}}$ and $\overline{\text{SMI}}$ should be held asserted until the exception is taken; $\overline{\text{CKSTP\_IN}}$ must be held asserted until the system has been reset. See the *MPC750 RISC Microprocessor Family User’s Manual* for more information.

Figure 6 provides the input/output timing diagram for the MPC755.

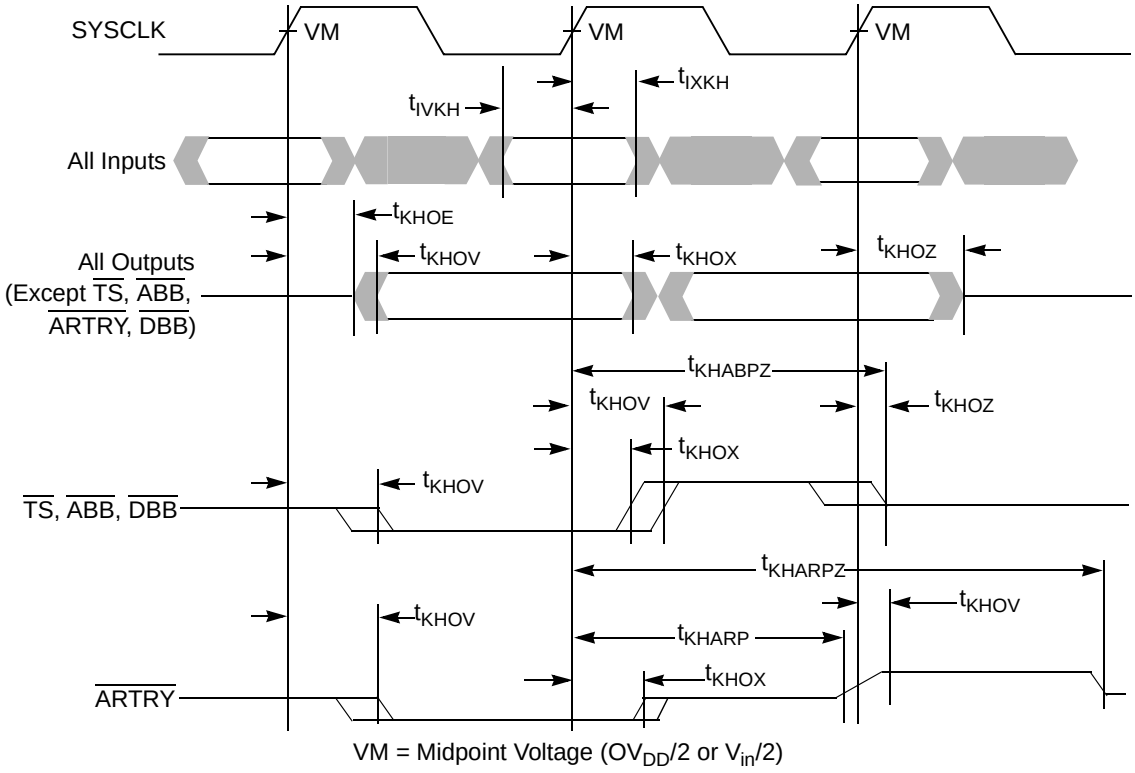


Figure 6. Input/Output Timing Diagram

1.4.2.3 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 configuration register (L2CR[4–6]) core-to-L2 divisor ratio. See Table 17 for example core and L2 frequencies at various divisors. Table 11 provides the potential range of L2CLK output AC timing specifications as defined in Figure 7.

The minimum L2CLK frequency of Table 11 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLK_OUTA, L2CLK_OUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase-aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLK_OUT signals provided for SRAM clocking will not be phase-aligned with the MPC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 11 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode, especially at higher core frequencies. Therefore, most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the MPC755 will be a function of the AC timings of the MPC755, the AC timings for the SRAM, bus loading, and printed-circuit board trace length. The current AC timing of the MPC755 supports up to 200 MHz with typical, similarly-rated SRAM parts, provided careful design practices are observed. Clock trace lengths must be matched and all trace lengths should be as short as possible. Higher frequencies can be achieved by using better performing SRAM. Note that revisions of the MPC755 prior to Rev. 2.8 (Rev. E) were limited in performance, and were typically limited to 175 MHz with similarly-rated SRAM. For more information, see Section 1.10.2, “Part Numbers Not Fully Addressed by This Document.”

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 11. Therefore, functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

L2 input and output signals are latched or enabled, respectively, by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 12 and Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLK_OUTA and L2CLK_OUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 12 and Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the MPC755 to synchronize L2CLK_OUT at the SRAM with the processor's internal clock. L2CLK_OUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN1794/D, *Backside L2 Timing Analysis for PCB Design Engineers*.

The L2CLK_OUTA and L2CLK_OUTB signals should not have more than two loads.

Table 11. L2CLK Output AC Timing Specification

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2CLK frequency	f_{L2CLK}	80	450	MHz	1, 4
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns	
L2CLK duty cycle	t_{CHCL}/t_{L2CLK}	45	55	%	2, 7
Internal DLL-relock time		640	—	L2CLK	3, 7
DLL capture window		0	10	ns	5, 7
L2CLK_OUT output-to-output skew	t_{L2CSKW}	—	50	ps	6, 7
L2CLK_OUT output jitter		—	±150	ps	6, 7

Notes:
1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT, and L2SYNC_OUT pins. The L2CLK frequency-to-core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL-relock time is specified in terms of L2CLK periods. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in ns. Relock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLK_OUT and the L2 address/data/control signals equally and, therefore, is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

The L2CLK_OUT timing diagram is shown in Figure 7.

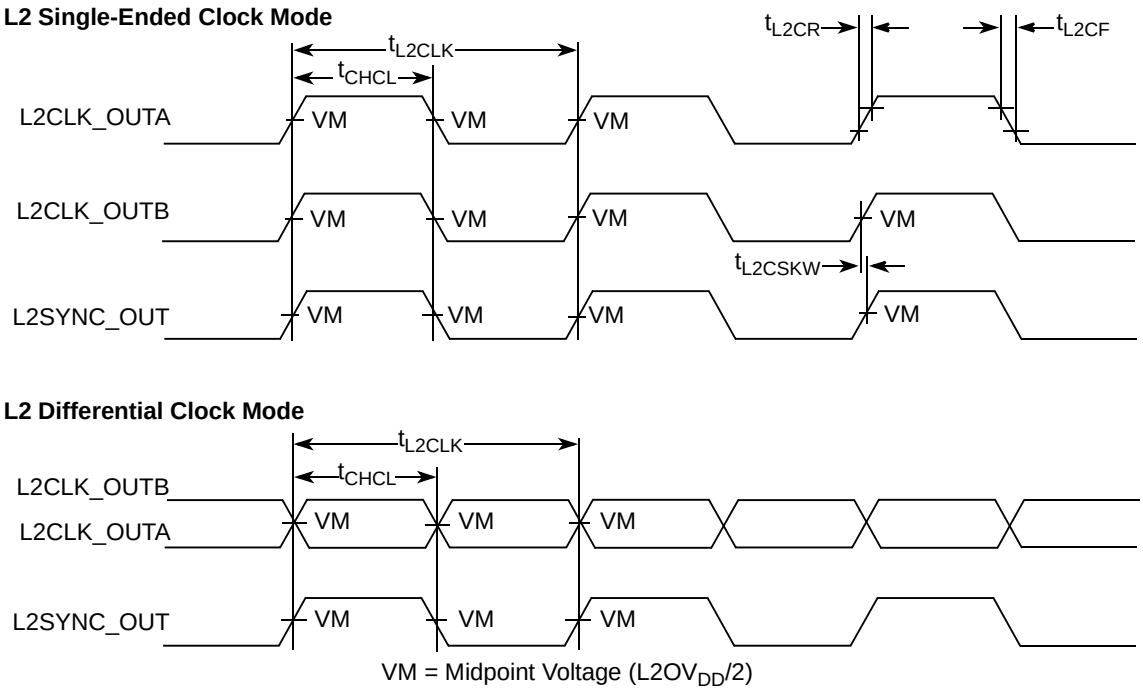


Figure 7. L2CLK_OUT Output Timing Diagram

1.4.2.4 L2 Bus AC Specifications

Table 12 provides the L2 bus interface AC timing specifications for the MPC755 as defined in Figure 8 and Figure 9 for the loading conditions described in Figure 10.

Table 12. L2 Bus Interface AC Timing Specifications

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2SYNC_IN rise and fall time	t_{L2CR}, t_{L2CF}	—	1.0	ns	1
Setup times: Data and parity	t_{DVL2CH}	1.2	—	ns	2
Input hold times: Data and parity	t_{DXL2CH}	0	—	ns	2
Valid times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOV}	 — — — —	 3.1 3.2 3.3 3.7	ns	3, 4
Output hold times: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOX}	 0.5 0.7 0.9 1.1	 — — — —	ns	3

Table 12. L2 Bus Interface AC Timing Specifications (continued)

At recommended operating conditions (see Table 3)

Parameter	Symbol	All Speed Grades		Unit	Notes
		Min	Max		
L2SYNC_IN to high impedance: All outputs when L2CR[14–15] = 00 All outputs when L2CR[14–15] = 01 All outputs when L2CR[14–15] = 10 All outputs when L2CR[14–15] = 11	t_{L2CHOZ}	 — — — —	 2.4 2.6 2.8 3.0	ns	3, 5

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14–15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14–15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev. 2.8 (Rev. E) were limited in performance and did not conform to this specification. For more information, refer to Section 1.10.2, “Part Numbers Not Fully Addressed by This Document.”

Figure 8 shows the L2 bus input timing diagrams for the MPC755.

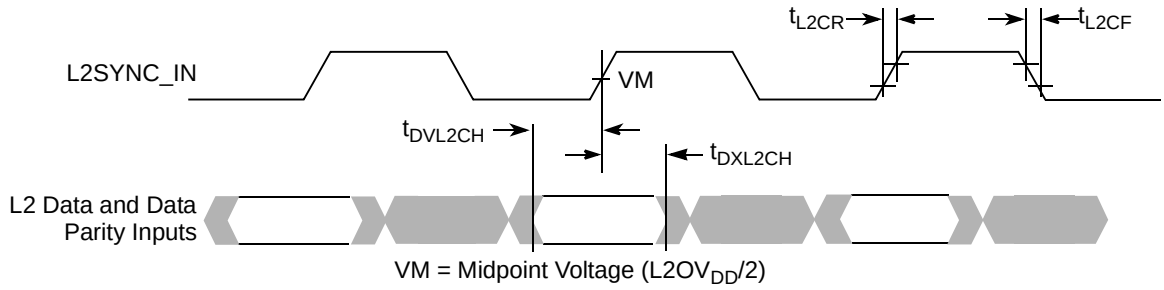


Figure 8. L2 Bus Input Timing Diagrams

Figure 9 shows the L2 bus output timing diagrams for the MPC755.

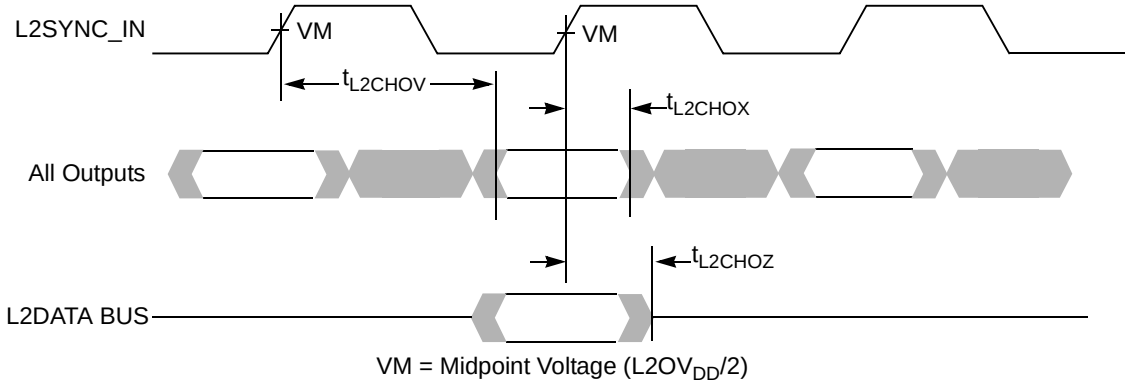


Figure 9. L2 Bus Output Timing Diagrams

Figure 10 provides the AC test load for L2 interface of the MPC755.

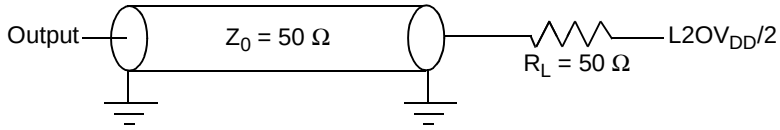


Figure 10. AC Test Load for the L2 Interface

1.4.2.5 IEEE 1149.1 AC Timing Specifications

Table 13 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 12 through Figure 15.

Table 13. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3)

Parameter		Symbol	Min	Max	Unit	Notes
TCK frequency of operation		f_{TCLK}	0	16	MHz	
TCK cycle time		t_{TCLK}	62.5	—	ns	
TCK clock pulse width measured at 1.4 V		t_{JHJL}	31	—	ns	
TCK rise and fall times		t_{JR}, t_{JF}	0	2	ns	
$\overline{\text{TRST}}$ assert time		t_{TRST}	25	—	ns	2
Input setup times:	Boundary-scan data TMS, TDI	t_{DVJH} t_{IVJH}	4 0	— —	ns	3
Input hold times:	Boundary-scan data TMS, TDI	t_{DXJH} t_{IXJH}	15 12	— —	ns	3
Valid times:	Boundary-scan data TDO	t_{JLDV} t_{JLOV}	— —	4 4	ns	4
Output hold times:	Boundary-scan data TDO	t_{JLDH} t_{JLOH}	25 12	— —	ns	4
TCK to output high impedance:	Boundary-scan data TDO	t_{JLDZ} t_{JLOZ}	3 3	19 9	ns	4, 5

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 11). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal which must be asserted for this minimum time to be recognized.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 11 provides the AC test load for TDO and the boundary-scan outputs of the MPC755.

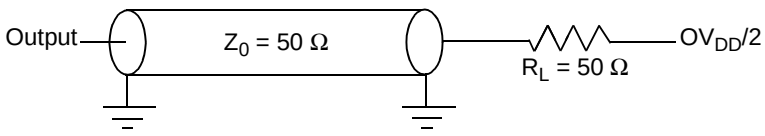


Figure 11. AC Test Load for the JTAG Interface

Figure 12 provides the JTAG clock input timing diagram.

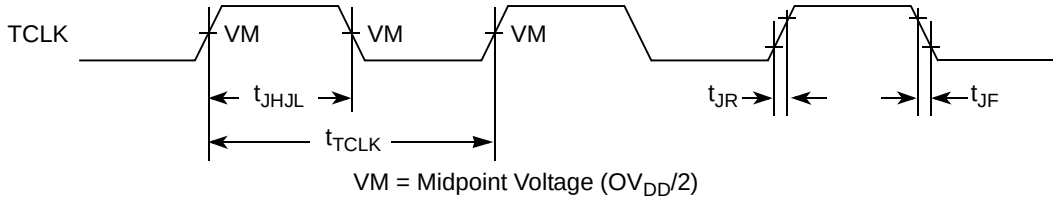


Figure 12. JTAG Clock Input Timing Diagram

Figure 13 provides the $\overline{\text{TRST}}$ timing diagram.

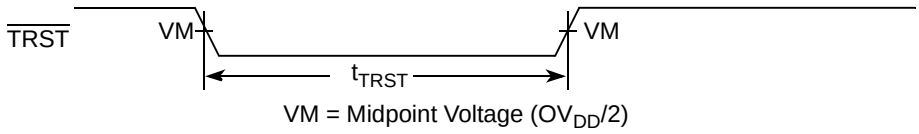


Figure 13. $\overline{\text{TRST}}$ Timing Diagram

Figure 14 provides the boundary-scan timing diagram.

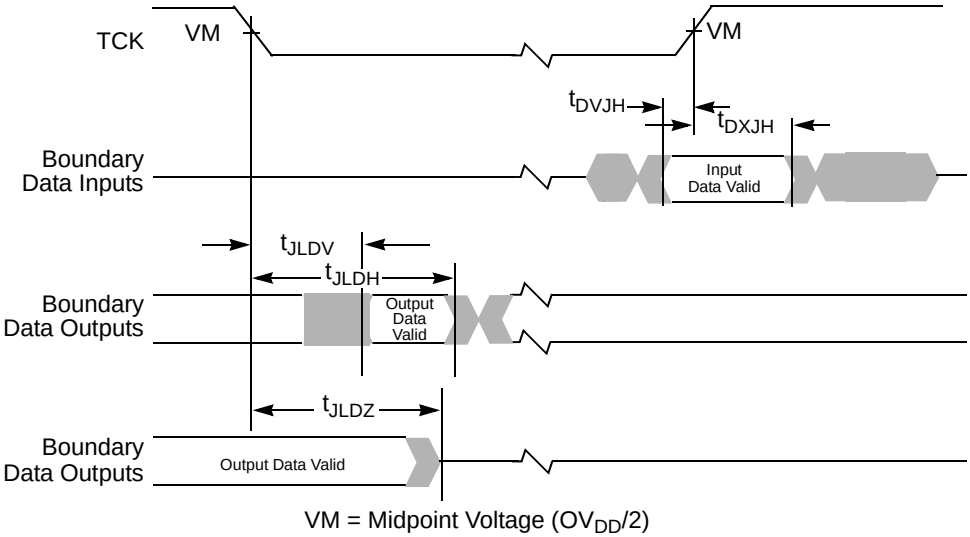


Figure 14. Boundary-Scan Timing Diagram

Figure 15 provides the test access port timing diagram.

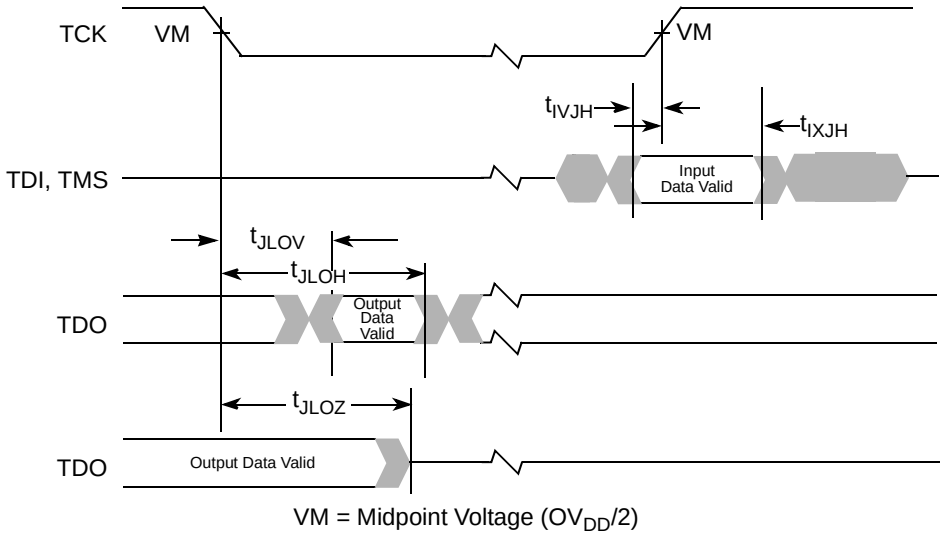
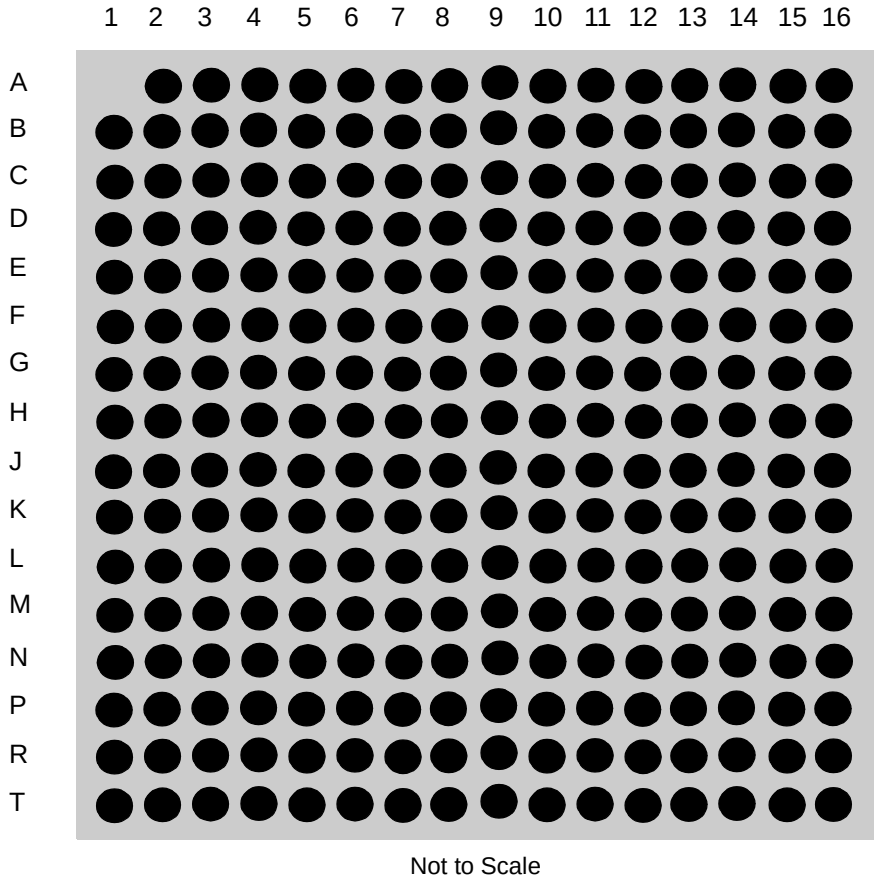


Figure 15. Test Access Port Timing Diagram

1.5 Pin Assignments

Figure 16 (in Part A) shows the pinout of the MPC745, 255 PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Part A



Part B

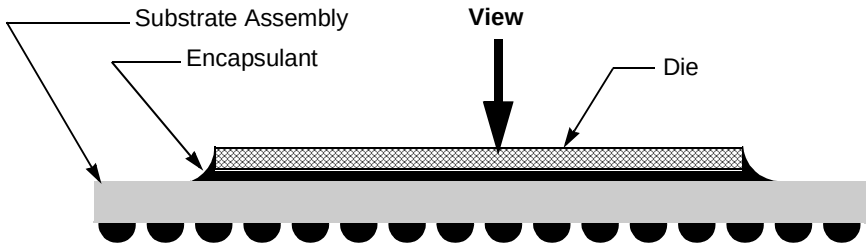
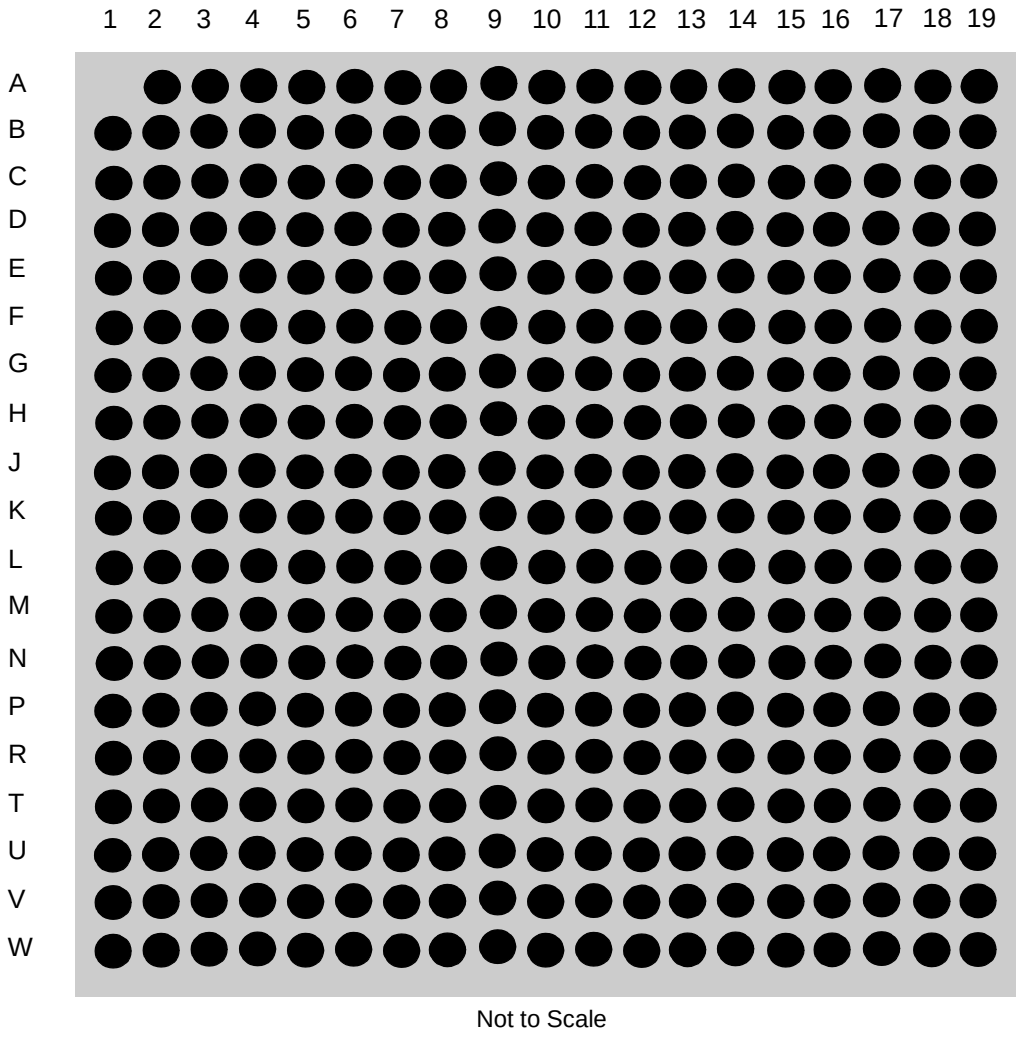


Figure 16. Pinout of the MPC745, 255 PBGA Package as Viewed from the Top Surface

Figure 17 (in Part A) shows the pinout of the MPC755, 360 PBGA and 360 CBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA and CBGA package to indicate the direction of the top surface view.

Part A



Part B

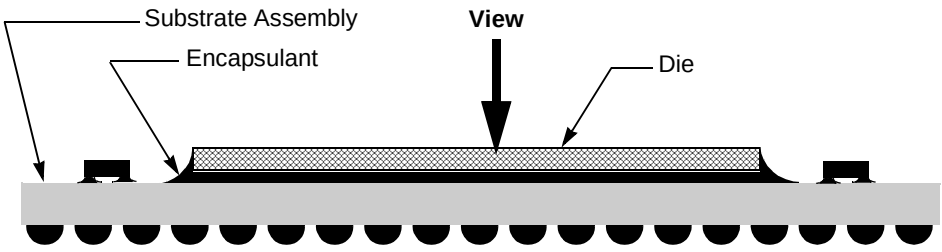


Figure 17. Pinout of the MPC755, 360 PBGA and CBGA Packages as Viewed from the Top Surface

1.6 Pinout Listings

Table 14 provides the pinout listing for the MPC745, 255 PBGA package.

Table 14. Pinout Listing for the MPC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	L2	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	K4	Low	I/O	OV_{DD}	
AP[0:3]	C1, B4, B3, B2	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	J4	Low	I/O	OV_{DD}	
AV_{DD}	A10	—	—	2.0 V	
$\overline{\text{BG}}$	L1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	B6	Low	Output	OV_{DD}	
BVSEL	B1	High	Input	OV_{DD}	3, 4, 5
$\overline{\text{CI}}$	E1	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	D8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	A6	Low	Output	OV_{DD}	
CLK_OUT	D7	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	J14	Low	I/O	OV_{DD}	
$\overline{\text{DBG}}$	N1	Low	Input	OV_{DD}	
$\overline{\text{DBDIS}}$	H15	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	G4	Low	Input	OV_{DD}	
DH[0:31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	OV_{DD}	
DL[0:31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	OV_{DD}	
DP[0:7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	G16	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	F1	Low	I/O	OV_{DD}	
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12	—	—	GND	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
$\overline{\text{HRESET}}$	A7	Low	Input	OV_{DD}	
$\overline{\text{INT}}$	B15	Low	Input	OV_{DD}	
L1_TSTCLK	D11	High	Input	—	2
L2_TSTCLK	D12	High	Input	—	2
$\overline{\text{LSSD\_MODE}}$	B10	Low	Input	—	2
$\overline{\text{MCP}}$	C13	Low	Input	OV_{DD}	
NC (No Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	—	—	—	
OV_{DD}	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	—	—	2.5 V/3.3 V	
PLL_CFG[0:3]	A8, B9, A9, D9	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	D3	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D1	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A16	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	B14	Low	Input	OV_{DD}	
SYSCLK	C9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	H14	Low	Input	OV_{DD}	
TBEN	C2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A14	Low	I/O	OV_{DD}	
TCK	C11	High	Input	OV_{DD}	
TDI	A11	High	Input	OV_{DD}	5
TDO	A12	High	Output	OV_{DD}	
$\overline{\text{TEA}}$	H13	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	C4	Low	Input	OV_{DD}	
TMS	B11	High	Input	OV_{DD}	5
$\overline{\text{TRST}}$	C10	Low	Input	OV_{DD}	5
$\overline{\text{TS}}$	J13	Low	I/O	OV_{DD}	
TSIZ[0:2]	A13, D10, B12	High	Output	OV_{DD}	
TT[0:4]	B13, A15, B16, C14, C15	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	D2	Low	Output	OV_{DD}	
V_{DD}	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	—	—	2.0 V	

Table 14. Pinout Listing for the MPC745, 255 PBGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	F3	High	Output	—	6

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals; and V_{DD} supplies power to the processor core and the PLL (after filtering to become AV_{DD}). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. Uses 1 of 15 existing no connects in the MPC740, 255 BGA package.
5. Internal pull-up on die.
6. Internally tied to GND in the MPC745, 255 BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.
   Caution: This differs from the MPC755, 360 BGA package.

Table 15 provides the pinout listing for the MPC755, 360 PBGA and CBGA packages.

Table 15. Pinout Listing for the MPC755, 360 BGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
A[0:31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	OV_{DD}	
$\overline{\text{AACK}}$	N3	Low	Input	OV_{DD}	
$\overline{\text{ABB}}$	L7	Low	I/O	OV_{DD}	
AP[0:3]	C4, C5, C6, C7	High	I/O	OV_{DD}	
$\overline{\text{ARTRY}}$	L6	Low	I/O	OV_{DD}	
AV_{DD}	A8	—	—	2.0 V	
$\overline{\text{BG}}$	H1	Low	Input	OV_{DD}	
$\overline{\text{BR}}$	E7	Low	Output	OV_{DD}	
BVSEL	W1	High	Input	OV_{DD}	3, 5, 6
$\overline{\text{CI}}$	C2	Low	Output	OV_{DD}	
$\overline{\text{CKSTP\_IN}}$	B8	Low	Input	OV_{DD}	
$\overline{\text{CKSTP\_OUT}}$	D7	Low	Output	OV_{DD}	
CLK_OUT	E3	—	Output	OV_{DD}	
$\overline{\text{DBB}}$	K5	Low	I/O	OV_{DD}	
$\overline{\text{DBDIS}}$	G1	Low	Input	OV_{DD}	
$\overline{\text{DBG}}$	K1	Low	Input	OV_{DD}	
$\overline{\text{DBWO}}$	D1	Low	Input	OV_{DD}	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
DH[0:31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	OV_{DD}	
DL[0:31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	OV_{DD}	
DP[0:7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	OV_{DD}	
$\overline{\text{DRTRY}}$	H6	Low	Input	OV_{DD}	
$\overline{\text{GBL}}$	B1	Low	I/O	OV_{DD}	
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	—	—	GND	
$\overline{\text{HRESET}}$	B6	Low	Input	OV_{DD}	
$\overline{\text{INT}}$	C11	Low	Input	OV_{DD}	
L1_TSTCLK	F8	High	Input	—	2
L2ADDR[16:0]	G18, H19, J13, J14, H17, H18, J16, J17, J18, J19, K15, K17, K18, M19, L19, L18, L17	High	Output	$L2OV_{DD}$	
$L2AV_{DD}$	L13	—	—	2.0 V	
$\overline{\text{L2CE}}$	P17	Low	Output	$L2OV_{DD}$	
L2CLK_OUTA	N15	—	Output	$L2OV_{DD}$	
L2CLK_OUTB	L16	—	Output	$L2OV_{DD}$	
L2DATA[0:63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	$L2OV_{DD}$	
L2DP[0:7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	$L2OV_{DD}$	
$L2OV_{DD}$	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	—	—	$L2OV_{DD}$	
L2SYNC_IN	L14	—	Input	$L2OV_{DD}$	
L2SYNC_OUT	M14	—	Output	$L2OV_{DD}$	
L2_TSTCLK	F7	High	Input	—	2
L2VSEL	A19	High	Input	$L2OV_{DD}$	1, 5, 6, 7

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
$\overline{\text{L2WE}}$	N16	Low	Output	$L2OV_{DD}$	
L2ZZ	G17	High	Output	$L2OV_{DD}$	
$\overline{\text{LSSD\_MODE}}$	F9	Low	Input	—	2
$\overline{\text{MCP}}$	B11	Low	Input	OV_{DD}	
NC (No Connect)	B3, B4, B5, W19, K9, K11 [4], K19 [4]	—	—	—	
OV_{DD}	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	—	—	OV_{DD}	
PLL_CFG[0:3]	A4, A5, A6, A7	High	Input	OV_{DD}	
$\overline{\text{QACK}}$	B2	Low	Input	OV_{DD}	
$\overline{\text{QREQ}}$	J3	Low	Output	OV_{DD}	
$\overline{\text{RSRV}}$	D3	Low	Output	OV_{DD}	
$\overline{\text{SMI}}$	A12	Low	Input	OV_{DD}	
$\overline{\text{SRESET}}$	E10	Low	Input	OV_{DD}	
SYSCLK	H9	—	Input	OV_{DD}	
$\overline{\text{TA}}$	F1	Low	Input	OV_{DD}	
TBEN	A2	High	Input	OV_{DD}	
$\overline{\text{TBST}}$	A11	Low	I/O	OV_{DD}	
TCK	B10	High	Input	OV_{DD}	
TDI	B7	High	Input	OV_{DD}	6
TDO	D9	High	Output	OVdd	
$\overline{\text{TEA}}$	J1	Low	Input	OV_{DD}	
$\overline{\text{TLBISYNC}}$	A3	Low	Input	OV_{DD}	
TMS	C8	High	Input	OV_{DD}	6
$\overline{\text{TRST}}$	A10	Low	Input	OV_{DD}	6
$\overline{\text{TS}}$	K7	Low	I/O	OV_{DD}	
TSIZ[0:2]	A9, B9, C9	High	Output	OV_{DD}	
TT[0:4]	C10, D11, B12, C12, F11	High	I/O	OV_{DD}	
$\overline{\text{WT}}$	C3	Low	Output	OV_{DD}	
V_{DD}	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	—	—	2.0 V	

Table 15. Pinout Listing for the MPC755, 360 BGA Package (continued)

Signal Name	Pin Number	Active	I/O	I/F Voltage [1]	Notes
VOLTDET	K13	High	Output	$L2OV_{DD}$	8

Notes:
1. $\underline{OV_{DD}}$ supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls ($\overline{L2CE}$, $\overline{L2WE}$, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0:16], L2DATA[0:63], L2DP[0:7], and L2SYNC_OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$, respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 2 and the voltage supplied. For actual recommended value of V_{in} or supply voltages, see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. This pin must be pulled up to OV_{DD} for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} or GND.
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of nine existing no connects in the MPC750, 360 BGA package.
6. Internal pull-up on die.
7. This pin must be pulled up to $L2OV_{DD}$ for proper operation of the processor interface. To allow for future I/O voltage changes, provide the option to connect L2VSEL independently to either $L2OV_{DD}$ or GND.
8. Internally tied to $L2OV_{DD}$ in the MPC755, 360 BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
   Caution: This differs from the MPC745, 255 BGA package.

1.7 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC745, 255 PBGA package, as well as the MPC755, 360 CBGA and PBGA packages. While both the MPC755 plastic and ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, see the *Motorola Flip-Chip Plastic Ball Grid Array Presentation*. The MPC755 was initially sampled in a CBGA package, but production units are currently provided in both a CBGA and a PBGA package. Because of the better long-term device-to-board interconnect reliability of the PBGA package, Motorola recommends use of a PBGA package except where circumstances dictate use of a CBGA package.

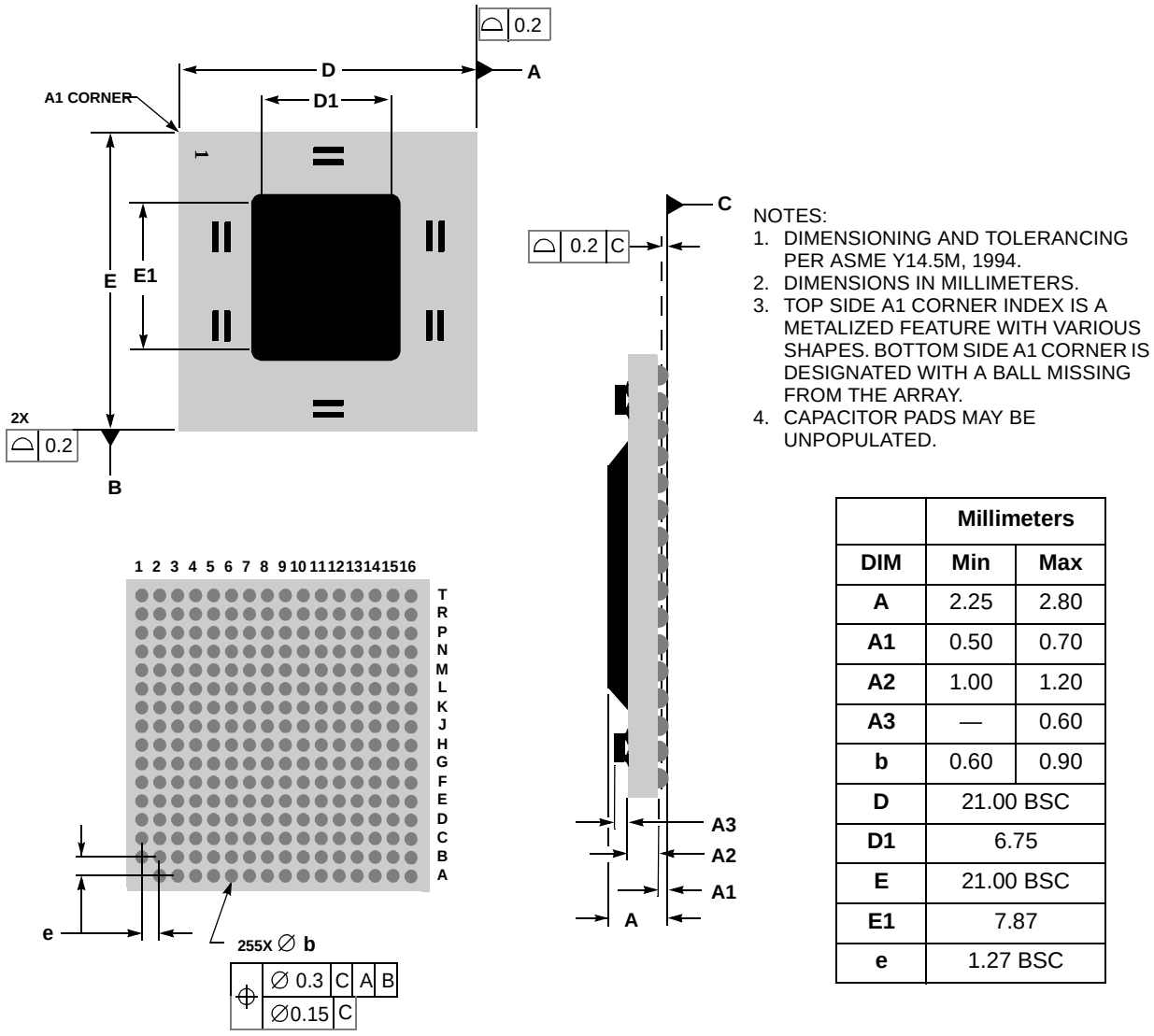
1.7.1 Package Parameters for the MPC745 PBGA

The package parameters are as provided in the following list. The package type is 21 × 21 mm, 255-lead plastic ball grid array (PBGA).

Package outline	21 × 21 mm
Interconnects	255 (16 × 16 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.25 mm
Maximum module height	2.80 mm
Ball diameter (typical)	0.75 mm (29.5 mil)

1.7.2 Mechanical Dimensions for the MPC745 PBGA

Figure 18 provides the mechanical dimensions and bottom surface nomenclature for the MPC745, 255 PBGA package.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.
4. CAPACITOR PADS MAY BE UNPOPULATED.

	Millimeters	
DIM	**Min**	**Max**
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	21.00 BSC	
D1	6.75	
E	21.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC745, 255 PBGA Package

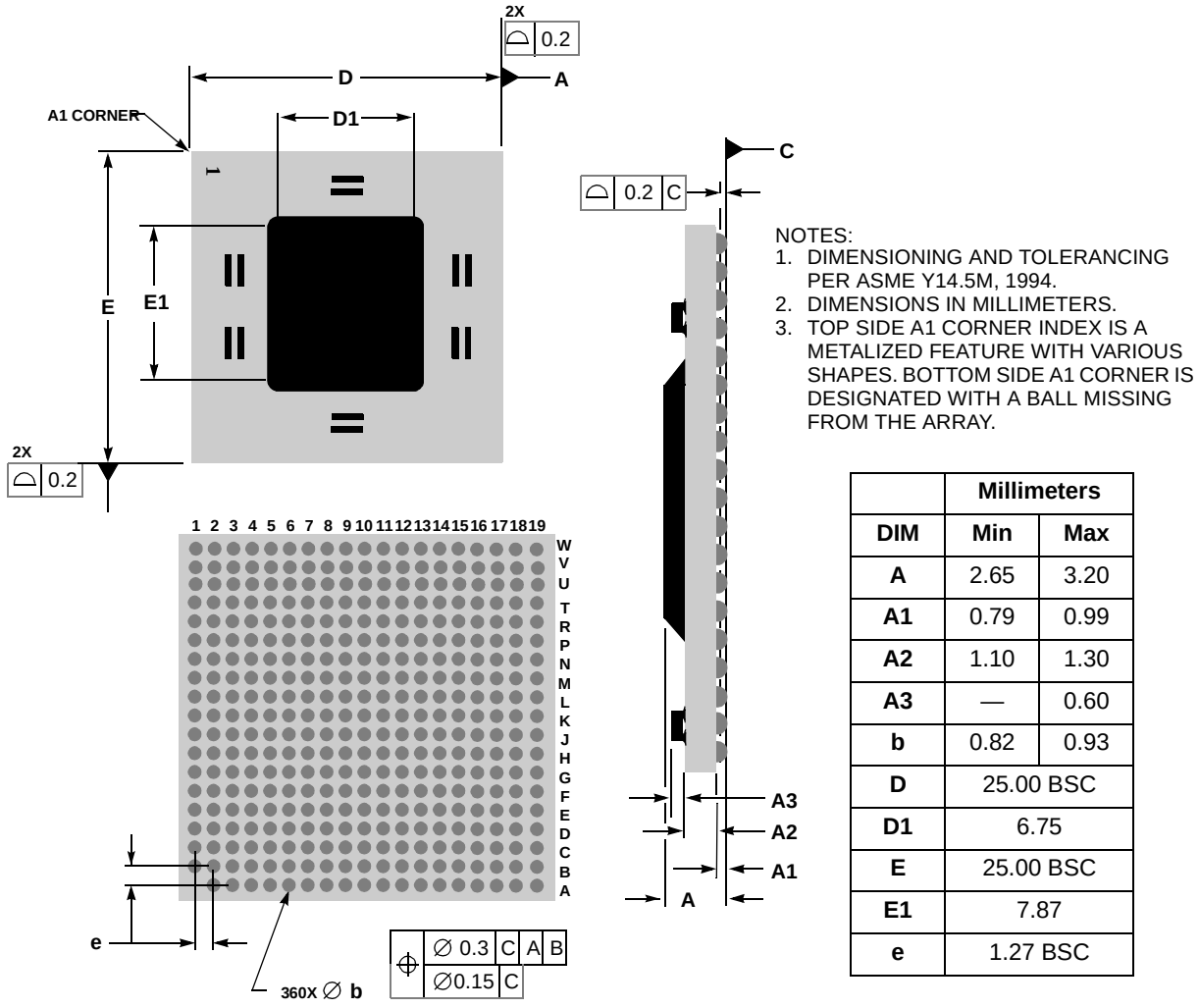
1.7.3 Package Parameters for the MPC755 CBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)

1.7.4 Mechanical Dimensions for the MPC755 CBGA

Figure 19 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 CBGA package.



	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.20
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 19. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 CBGA Package

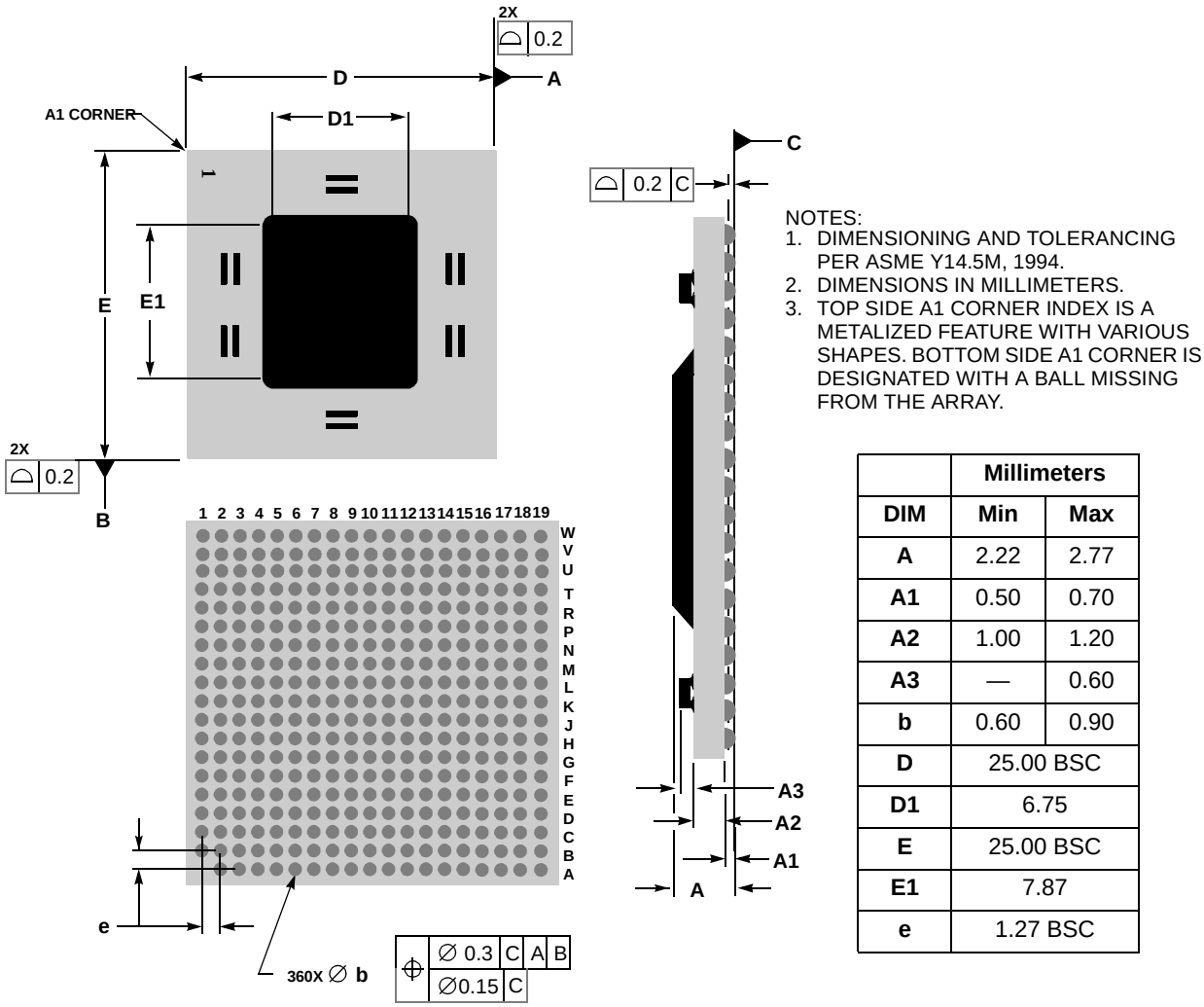
1.7.5 Package Parameters for the MPC755 PBGA

The package parameters are as provided in the following list. The package type is 25 × 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 × 25 mm
Interconnects	360 (19 × 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

1.7.6 Mechanical Dimensions for the MPC755

Figure 20 provides the mechanical dimensions and bottom surface nomenclature for the MPC755, 360 PBGA package.



	Millimeters	
DIM	Min	Max
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
A3	—	0.60
b	0.60	0.90
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Figure 20. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC755, 360 PBGA Package

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC755.

1.8.1 PLL Configuration

The MPC755 PLL is configured by the PLL_CFG[0:3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. These must be chosen such that they comply with Table 8. Table 16 shows the valid configurations of these signals and an example illustrating the core and VCO frequencies resulting from various PLL configurations and example bus frequencies. In this example, shaded cells represent settings that, for a given SYSCLK frequency, result in core and/or VCO frequencies that do not comply with the 400-MHz column in Table 8.

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
0100	2x	2x	—	—	—	—	—	200 (400)
1000	3x	2x	—	—	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	—	—	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	—	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	—	225 (450)	300 (600)	338 (675)	360 (720)	—
1011	5x	2x	—	250 (500)	333 (666)	375 (750)	400 (800)	—
1001	5.5x	2x	—	275 (550)	366 (733)	—	—	—
1101	6x	2x	200 (400)	300 (600)	400 (800)	—	—	—
0101	6.5x	2x	216 (433)	325 (650)	—	—	—	—
0010	7x	2x	233 (466)	350 (700)	—	—	—	—
0001	7.5x	2x	250 (500)	375 (750)	—	—	—	—
1100	8x	2x	266 (533)	400 (800)	—	—	—	—
0110	10x	2x	333 (666)	—	—	—	—	—
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					

Table 16. MPC755 Microprocessor PLL Configuration Example for 400 MHz Parts (continued)

PLL_CFG [0:3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	Core-to-VCO Multiplier	Bus 33 MHz	Bus 50 MHz	Bus 66 MHz	Bus 75 MHz	Bus 80 MHz	Bus 100 MHz
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the MPC755 regardless of the SYSCLK input.

The MPC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the MPC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the MPC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the MPC755 core, and the phase adjustment range that the L2 DLL supports. Table 17 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 17. Sample Core-to-L2 Frequencies

Core Frequency (MHz)	÷1	÷1.5	÷2	÷2.5	÷3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the MPC755; see Section 1.4.2.3, “L2 Clock AC Specifications,” for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

1.8.2 PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the MPC755 to provide power to the clock generation PLL and L2 cache DLL, respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 21 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route, but is proportionately less critical.

Figure 21 shows the PLL power supply filter circuit.

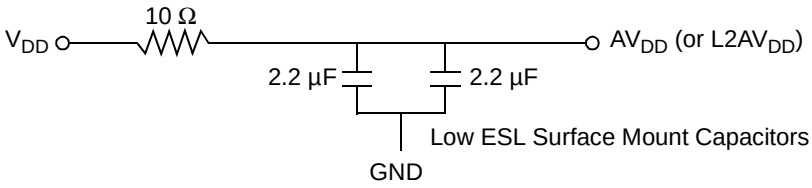


Figure 21. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the MPC755 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC755 system, and the MPC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the MPC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors:100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.8.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the MPC755. Note that power must be supplied to $L2OV_{DD}$ even if the L2 interface of the MPC755 will not be used; it is recommended to connect $L2OV_{DD}$ to OV_{DD} and L2VSEL to BVSEL if the L2 interface is unused. (This requirement does not apply to the MPC745 since it has neither an L2 interface nor $L2OV_{DD}$ pins.)

1.8.5 Output Buffer DC Impedance

The MPC755 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to $(L2)OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $(L2)OV_{DD}/2$ (see Figure 22).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices.

Figure 22 describes the driver impedance measurement circuit described above.

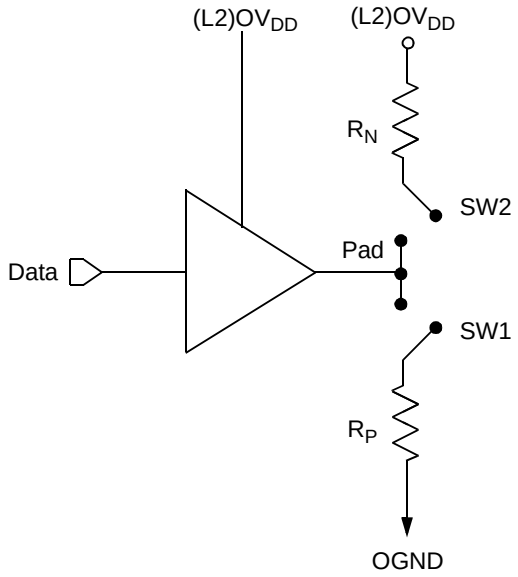


Figure 22. Driver Impedance Measurement Circuit

Alternately, the following is another method to determine the output impedance of the MPC755. A voltage source, V_{force}, is connected to the output of the MPC755 as shown in Figure 23. Data is held low, the voltage source is set to a value that is equal to $(L2)OV_{DD}/2$ and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to $(L2)OV_{DD}/2$, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, $(L2)OV_{DD}/2$, by the current sank by the pull-up when the data is high and V_{force} is equal to $(L2)OV_{DD}/2$. This method can be employed with either empirical data from a test setup or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 23 describes the alternate driver impedance measurement circuit.

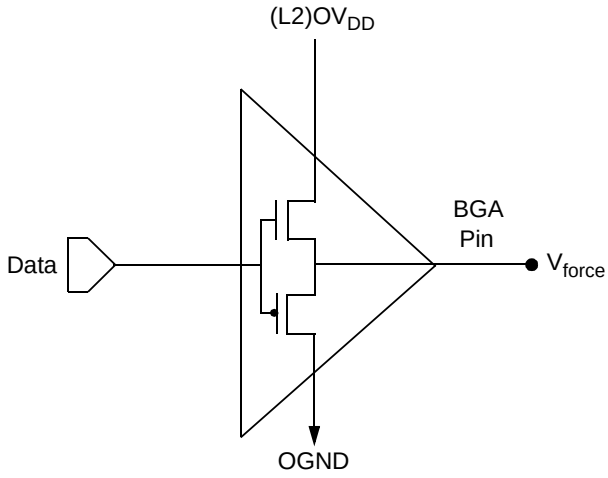


Figure 23. Alternate Driver Impedance Measurement Circuit

Table 18 summarizes the signal impedance results. The driver impedance values were characterized at 0°, 65°, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 18. Impedance Characteristics

V_{DD} = 2.0 V, OV_{DD} = 3.3 V, T_j = 0°–105°C

Impedance	Processor Bus	L2 Bus	Symbol	Unit
R_N	25–36	25–36	Z_0	Ω
R_P	26–39	26–39	Z_0	Ω

1.8.6 Pull-Up Resistor Requirements

The MPC755 requires pull-up resistors (1–5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the MPC755 or other bus masters. These pins are $\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{AACK}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{TEA}}$, and $\overline{\text{DBDIS}}$. $\overline{\text{DRTRY}}$ should also be connected to a pull-up resistor (1–5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{\text{HRESET}}$ to select NO-DRTRY mode (see the *MPC750 RISC Microprocessor Family User's Manual* for more information on this mode).

Three test pins also require pull-up resistors (100 Ω–1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{\text{CKSTP\_OUT}}$ is an open-drain style output that requires a pull-up resistor (1–5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the MPC755 must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the MPC755 or by other receivers in the system. These signals can be pulled up through weak (10-kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not neccessary

for proper device operation. The snooped address and transfer attribute inputs are: A[0:31], AP[0:3], TT[0:4], $\overline{\text{TBST}}$, and $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

The L2 interface does not require pull-up resistors.

1.8.7 JTAG Configuration Signals

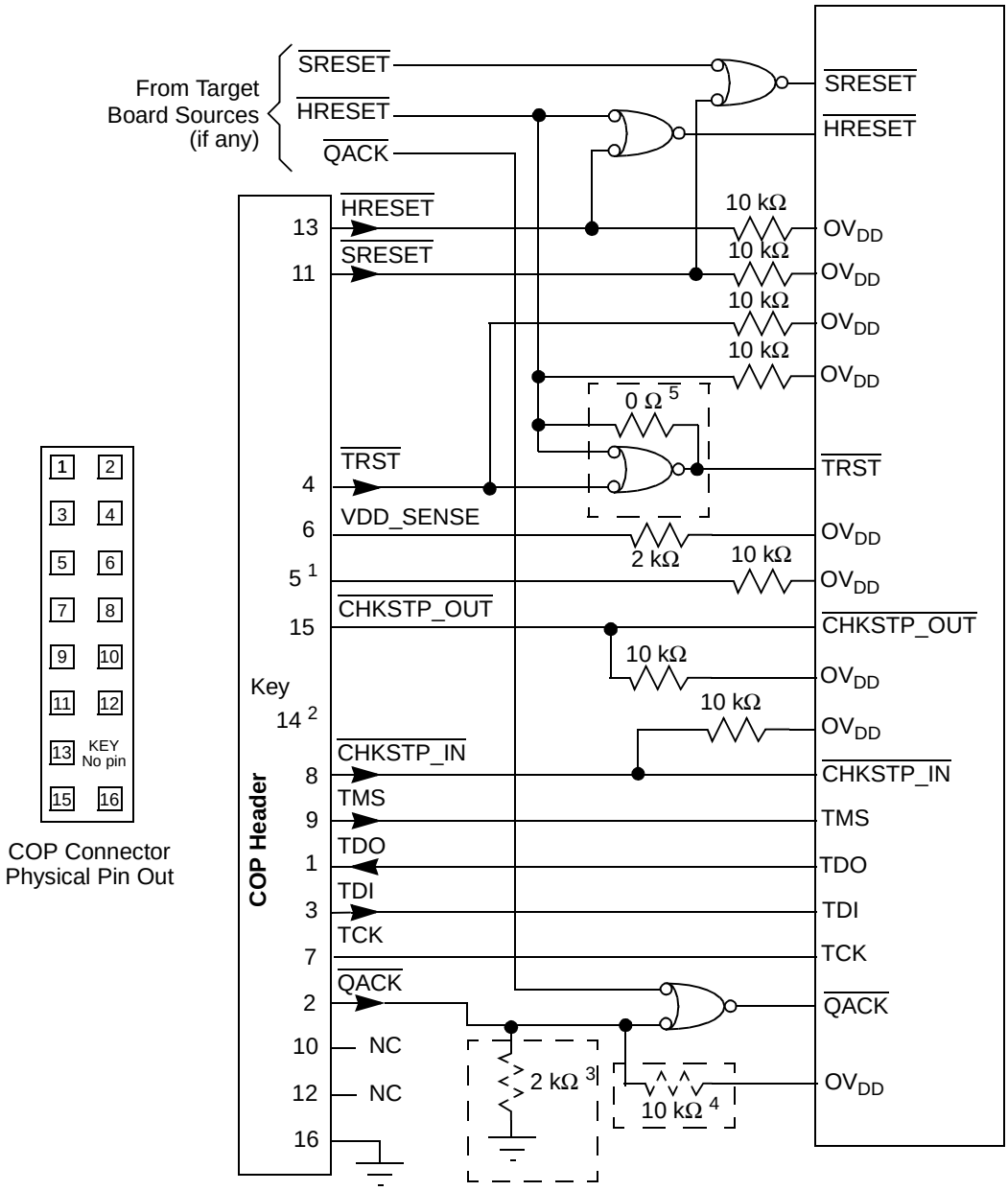
Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 24 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Motorola recommends that the COP header be designed into the system as shown in Figure 24, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the case where a JTAG interface may need to be wired onto the system in debug situations.

The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the MPC755. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ of the part through a 0-Ω isolation reisistor.

Figure 24. JTAG Interface Connection

There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter

clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 25 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Figure 24 is usually connected to the PCI bridge chip in a system and is an input to the MPC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low-power mode selection. In order for COP to work, the MPC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. If the product does not, a pull-down resistor can be populated to assert this signal. Additionally, some emulator products implement open-drain type outputs and can only drive $\overline{\text{QACK}}$ asserted; for these tools, a pull-up resistor can be implemented to ensure this signal is deasserted when it is not being driven by the tool. Note that the pull-up and pull-down resistors on the $\overline{\text{QACK}}$ signal are mutually exclusive and it is never necessary to populate both in a system. To preserve correct power-down operation, $\overline{\text{QACK}}$ should be merged via logic so that it also can be driven by the PCI bridge.

1.8.8 Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 25. This spring force should not exceed 5.5 pounds of force.

Figure 25 describes the package exploded cross-sectional view with several heat sink options.

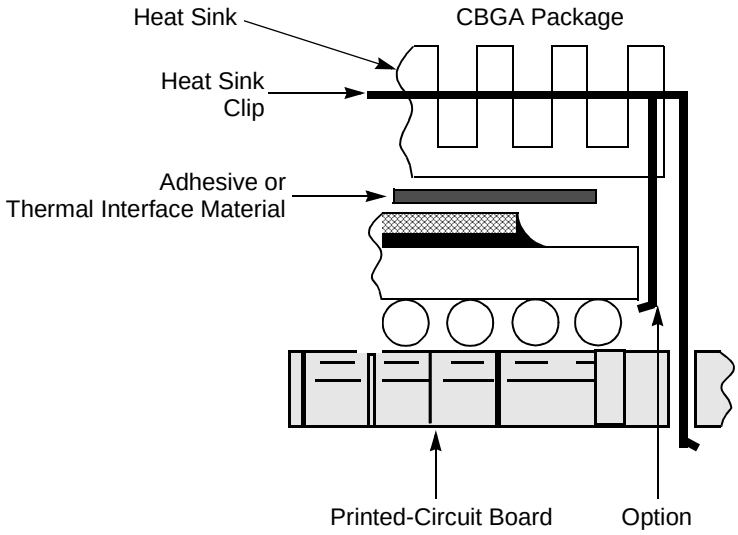


Figure 25. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the MPC755. There are several commercially-available heat sinks for the MPC755 provided by the following vendors:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.8.8.1 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in Table 4, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

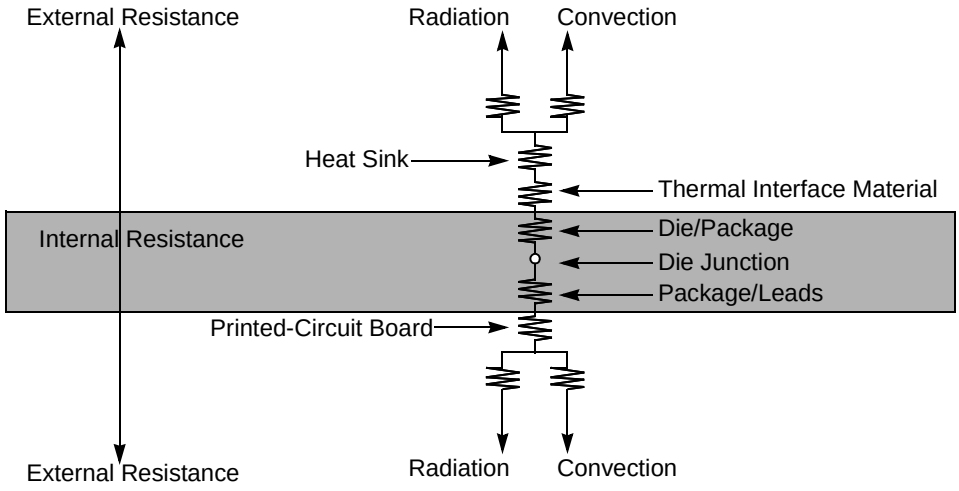


Figure 26. C4 Package with Heat Sink Mounted to a Printed-Circuit Board

1.8.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 27 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 25). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

Figure 27 describes the thermal performance of select thermal interface materials.

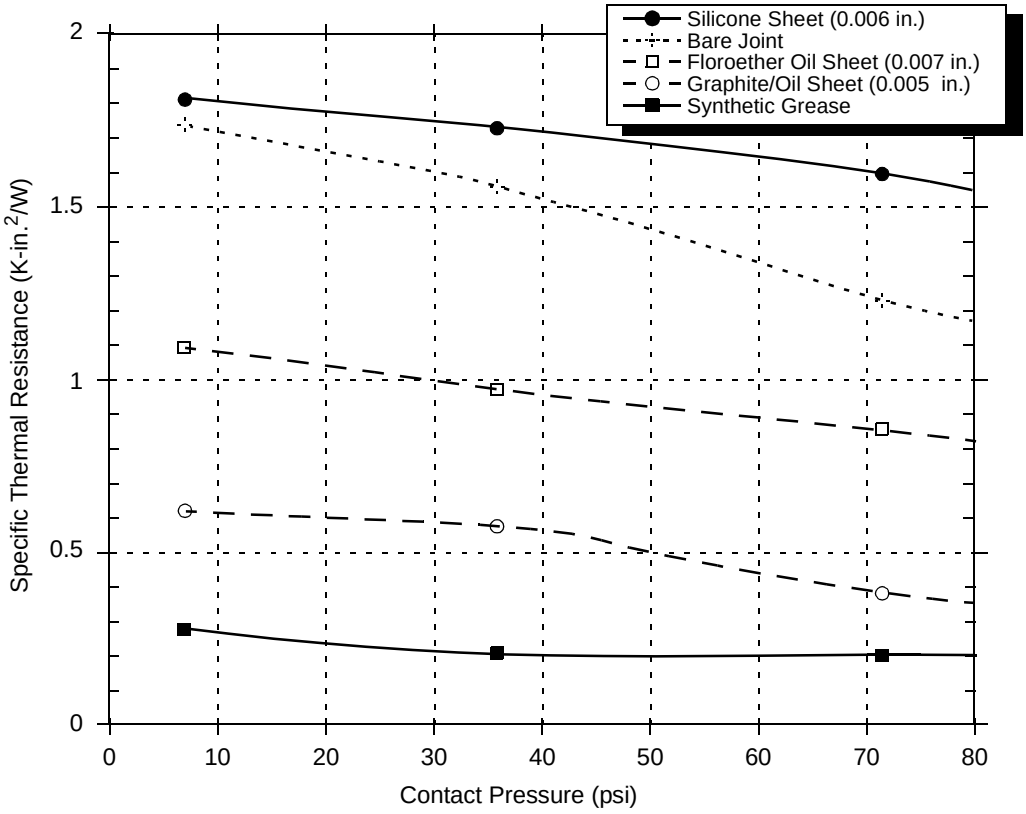


Figure 27. Thermal Performance of Select Thermal Interface Materials

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based on high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

The Bergquist Company — 800-347-4572
18930 West 78th St.
Chanhassen, MN 55317
Internet: www.bergquistcompany.com

Chomerics, Inc. — 781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation — 800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc. — 888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc. 888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

1.8.8.3 Heat Sink Selection Example

This section provides a heat sink selection example using one of the commercially-available heat sinks. For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$$

where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 3. The temperature of air cooling the component greatly depends on the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a T_r of 5°C, a CBGA package $R_{\theta jc} < 0.1$, and a power consumption (P_d) of 5.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{sa}) \times 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 28.

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$$T_j = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 7°C/W) \times 5.0\ W,$$

resulting in a die-junction temperature of approximately 76°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

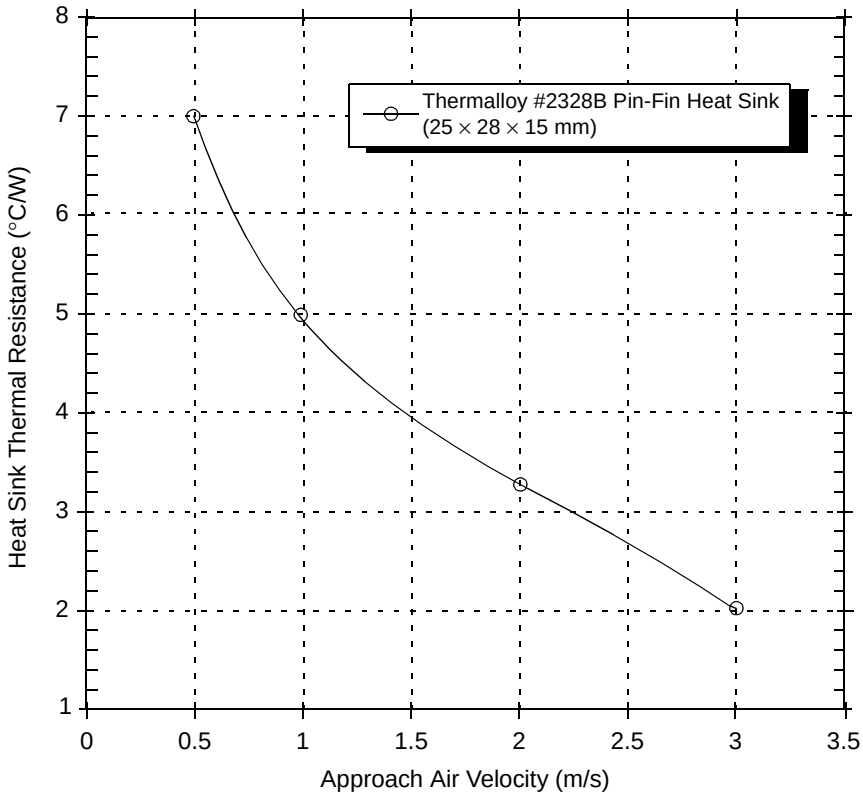


Figure 28. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection, and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs.

1.9 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Document Revision History

Rev. No.	Substantive Change(s)
0	Product announced. Documentation made publicly available.
1	Corrected errors in Section 1.2.
	Removed references to MPC745 CBGA package in Sections 1.3 and 1.4.
	Added airflow values for θ_{JA} to Table 5.
	Corrected V_{IH} maximum for 1.8 V mode in Table 6.
	Power consumption values added to Table 7.
	Corrected t_{MXRH} in Table 9, deleted Note 2 application note reference.
	Added Max f_{L2CLK} and Min t_{L2CLK} values to Table 11.
	Updated timing values in Table 12.
	Corrected Note 2 of Table 13.
	Changed Table 14 to reflect I/F voltages supported.
	Removed 133 and 150 MHz columns from Table 16.
	Added document reference to Section 1.7.
	Added $\overline{\text{DBB}}$ to list of signals requiring pull-ups in Section 1.8.7.
	Removed log entries from Table 20 for revisions prior to public release.
2	1.8 V/2.0 V mode no longer supported; added 2.5 V support.
	Removed 1.8 V/2.0 V mode data from Tables 2, 3, and 6.
	Added 2.5 V mode data to Tables 2, 3, and 6.
	Extended recommended operating voltage (down to 1.8 V) for V_{DD}, AV_{DD}, and $L2AV_{DD}$ for 300 and 350 MHz parts in Table 3.
	Updated Table 7 and test conditions for power consumption specifications.
	Corrected Note 6 of Table 9 to include $\overline{\text{TLBISYNC}}$ as a mode-select signal.
	Updated AC timing specifications in Table 10.
	Updated AC timing specifications in Table 12.
	Corrected AC timing specifications in Table 13.
	Added L1_TSTCLK, L2_TSTCLK, and $\overline{\text{LSSD\_MODE}}$ pull-up requirements to Section 1.8.6.
	Corrected Figure 22.

Table 19. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3	Updated format and thermal resistance specifications of Table 4.
	Reformatted Tables 9, 10, 11, and 12.
	Added dimensions A3, D1, and E1 to Figures 18, 19, and 20.
	Revised Section 1.8.7 and Figure 25, removed Figure 26 and Table 19 (information now included in Figure 25).
	Reformatted Section 1.10.
	Clarified address bus and address attribute pull-up recommendations in Section 1.8.7.
	Clarified Table 2.
	Updated voltage sequencing requirements in Table 1 and removed Section 1.8.3.
4	Added 450 MHz speed bin.
	Changed Table 16 to show 450 MHz part in example.
	Added row for 433 and 450 MHz core frequencies to Table 17.
	In Section 1.8.8, revised the heat sink vendor list.
	In Section 1.8.8.2, revised the interface vendor list.
5	Added Note 6 to Table 10; clarification only as this information is already documented in the *MPC750 RISC Microprocessor Family User's Manual*.
	Revised Figure 24 and Section 1.8.7.
	Corrected Process Identifier for 450 MHz part in Table 20.
	Added XPC755BRX*nnn*T*x* series to Table 21.
6	Removed 450 MHz speed grade throughout document. These devices are no longer supported for new designs; see Section 1.10.2 for more information.
	Relaxed voltage sequencing requirements in Notes 3 and 4 of Table 1.
	Corrected Note 2 of Table 7.
	Changed processor descriptor from 'B' to 'C' for 400 MHz devices and increased power specifications for full-power mode in Table 7. XPC755Bxx400LE devices are no longer produced and are documented in a separate part number specification; see Section 1.10.2 for more information.
	Increased power specifications for sleep mode for all speed grades in Table 7.
	Removed 'Sleep Mode (PLL and DLL Disabled)—Typical' specification from Table 7; this is no longer tested or characterized.
	Added Note 4 to Table 7.
	Revised L2 clock duty cycle specification in Table 11 and changed Note 7.
	Corrected Note 3 in Table 20.
	Replaced Table 21 and added Tables 22 and 23.

1.10 Ordering Information

Ordering information for the devices fully covered by this specification document is provided in Section 1.10.1, “Part Numbers Fully Addressed by This Document.” Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number. Section 1.10.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.10.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Motorola part numbering nomenclature for the MPC755 and MPC745 devices fully addressed by this document.

Table 20. Part Numbering Nomenclature

XPC	***xxx***	***x***	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency**	**Application Modifier**	**Revision Level**
XPC [2]	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.8; PVR = 0008 3203
	755	C = HiP4DP		400		

Notes:
1. See Section 1.7, “Package Description,” for more information on available package types.
2. The X prefix in a Motorola part number designates a “Pilot Production Prototype” as defined by Motorola SOP 3-13. These are from a limited production volume of prototypes manufactured, tested, and Q.A. inspected on a qualified technology to simulate normal production. These parts have only preliminary reliability and characterization data. Before pilot production prototypes may be shipped, written authorization from the customer must be on file in the applicable sales office acknowledging the qualification status and the fact that product changes may still occur while shipping pilot production prototypes

1.10.2 Part Numbers Not Fully Addressed by This Document

Devices not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document, as described in the following tables.

Table 21. Part Numbers Addressed by XPC755B*xxnnn*T*x* Series Part Number Specification (Document Order No. MPC755BTXPNS/D)

XPC	755	B	*xx*	*nnn*	T	*x*

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	350 400	T: 2.0 V ± 100 mV –40° to 105°C	D: 2.7; PVR = 0008 3203 E: 2.8; PVR = 0008 3203

Table 22. Part Numbers Addressed by XPC755B*xxnnn*LD Series Part Number Specification (Document Order No. MPC755BLDPNS/D)

XPC	*xxx*	B	*xx*	*nnn*	L	D

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755 745	B = HiP4DP	PX = PBGA RX = CBGA	300 350 400	L: 2.0 V ± 100 mV 0° to 105°C	D: 2.7; PVR = 0008 3203

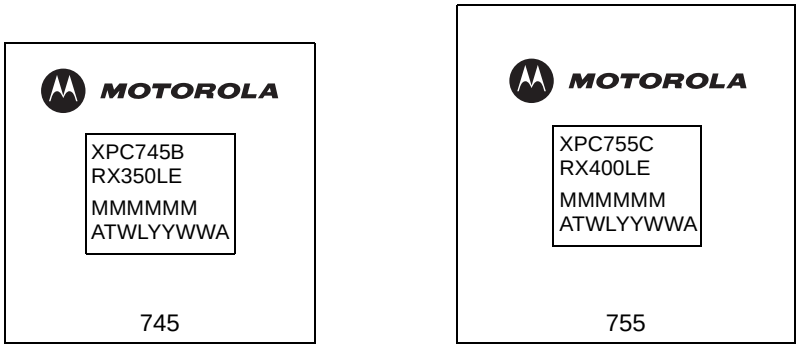
Table 23. Part Numbers Addressed by XPC755*xxxnnn*LE Series Part Number Specification (Document Order No. MPC755BLEPNS/D)

XPC	755	*x*	*xx*	*nnn*	L	E

Product Code	Part Identifier	Process Descriptor	Package	Processor Frequency	Application Modifier	Revision Level
XPC	755	B = HiP4DP	RX = CBGA	400	L: 2.0 V ± 100 mV 0° to 105°C	E: 2.7; PVR = 0008 3203
			PX = PBGA			
		C = HiP4DP	RX = CBGA	450		

1.10.3 Part Marking

Parts are marked as the example shown in Figure 29.



Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 29. Part Marking for BGA Device

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