National Semiconductor

ADVANCE INFORMATION

MM74C946 4½-Digit Counter/Decoder/ Driver for LCD Displays

General Description

The MM74C946 is a 4½-digit CMOS counter which contains a counter chain, decoders, output latches, LCD segment drivers, count inhibit and backplane oscillator/driver circuitry. This device also contains leading zero blanking and a carry output to increase flexibility and facilitate cascading of multiple 4-digit sections.

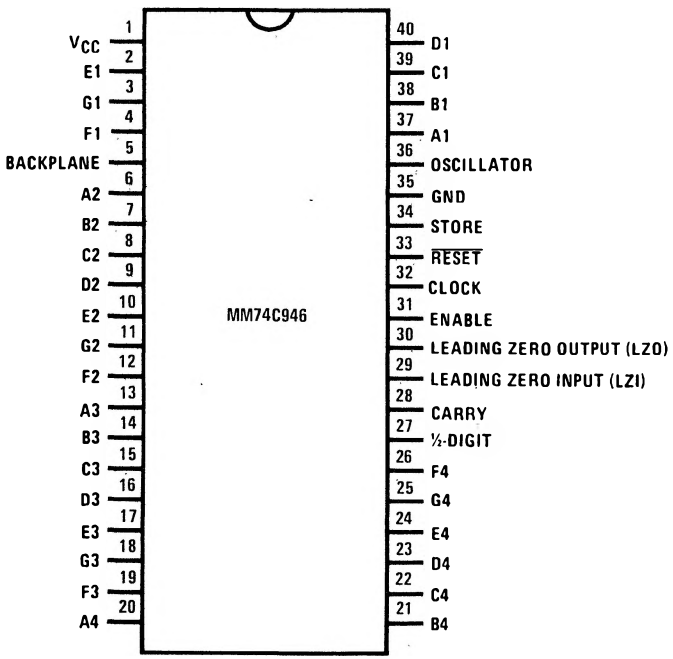
This device provides 29 segment outputs to drive a standard 4½-digit liquid crystal display. An on-chip backplane oscillator/driver is also provided. This can be disabled by grounding the oscillator pin, thus allowing the device to be slaved to an external backplane signal via the backplane pin.

Features

- Low power operation—less than 100 μW quiescent
- Direct 4½-digit 7-segment display drive for higher contrast and long display life
- Pin compatible to Intersil's ICM7224
- Store and $\overline{\text{Reset}}$ inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading 4-digit blocks
- Schmitt trigger on the clock input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- On-chip backplane oscillator/driver which can be disabled to permit slaving of multiple devices to an external backplane signal

Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range MM74C946	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Input)	$V_{CC}=5V$		3.3		V
V_{T-} Negative Going Threshold Voltage (Clock Input)	$V_{CC}=5V$		1.8		V
Hysteresis ($V_{T+}-V_{T-}$) (Clock Input)	$V_{CC}=5V$		1.5		V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Inputs Except Clock Input)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Inputs Except Clock Input)	$V_{CC}=5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=-10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=+10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN}\rvert$	$V_{CC}=5V$, $V_{IN}=5V/0V$		0.005	1.0	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC}=5V$, $V_{IN}=0V$	-2.0		-25.0	μA
Oscillator Pin Current (I_{OSL})	$V_{CC}=5V$, $V_{IN}=0V/5V$		± 2		μA
Supply Current (I_{CC}) (Note 3)	$V_{CC}=5V$, $V_{IN}=0V/5V$		10		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) (Clock Input)	$V_{CC}=5V$	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$) (Clock Input)	$V_{CC}=5V$			0.7	V
Logical "1" Input Voltage ($V_{IN(1)}$) (All Input Except Clock)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) (All Input Except Clock)	$V_{CC}=5V$			0.4	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.4 0.4	V V

DC Electrical Characteristics (Continued)

Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC} = 5V$ $T_A = 25°C$		2.6		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$ $T_A = 25°C$		2.8		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$ $T_A = 25°C$		1.9		mA
Output Sink Current (I_{SINK}) (Segment Outputs)	$V_{CC} = 5V$ $T_A = 25°C$		1.6		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25°C$		16.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$ $T_A = 25°C$		13.0		mA
Output Source Current (I_{SOURCE}) (½-Digit)	$V_{CC} = 5V$ $T_A = 25°C$		3.8		mA
Output Sink Current (I_{SINK}) (½-Digit)	$V_{CC} = 5V$ $T_A = 25°C$		3.2		mA

AC Electrical Characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified.

	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	$V_{CC} = 5.0V$				
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$		2		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$				ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$				ns
$t_{SET(CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$				ns
$t_{SET(R, S)}$	Reset to Store Set-Up Time	$V_{CC} = 5.0V$				ns
$t_{SET(E, S)}$	Enable to Store Set-Up Time	$V_{CC} = 5.0V$				ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$				ns
t_{pdc}	Propagation Delay Reset to Carry	$V_{CC} = 5.0V$				ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating		125		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 4)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		μs
t_{rfb}	Backplane Rise/Fall Time	$C_{load} = 5000$ pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating		16		kHz

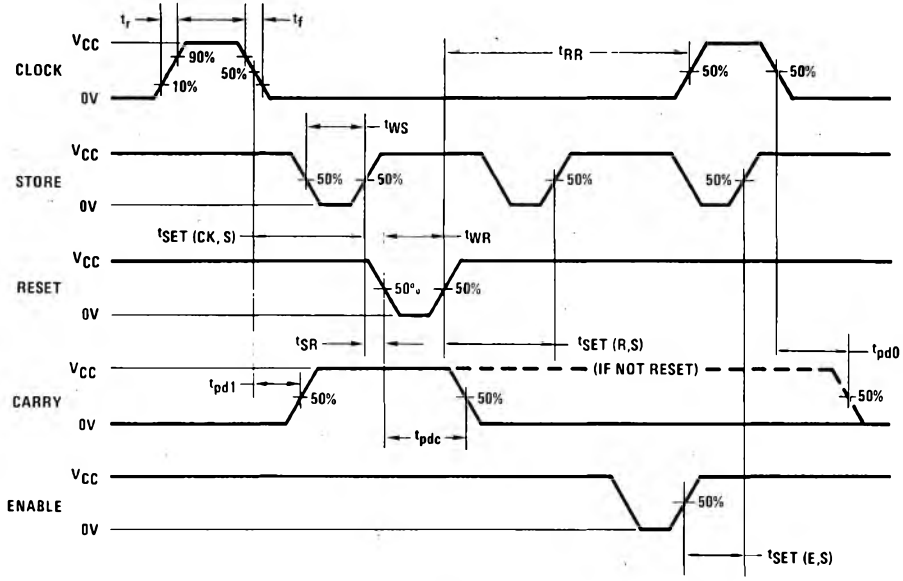
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These input pins have pull-ups to V_{CC}.

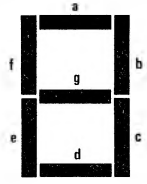
Note 3: See test circuit. Display blanked.

Note 4: Does not apply to backplane and oscillator pins.

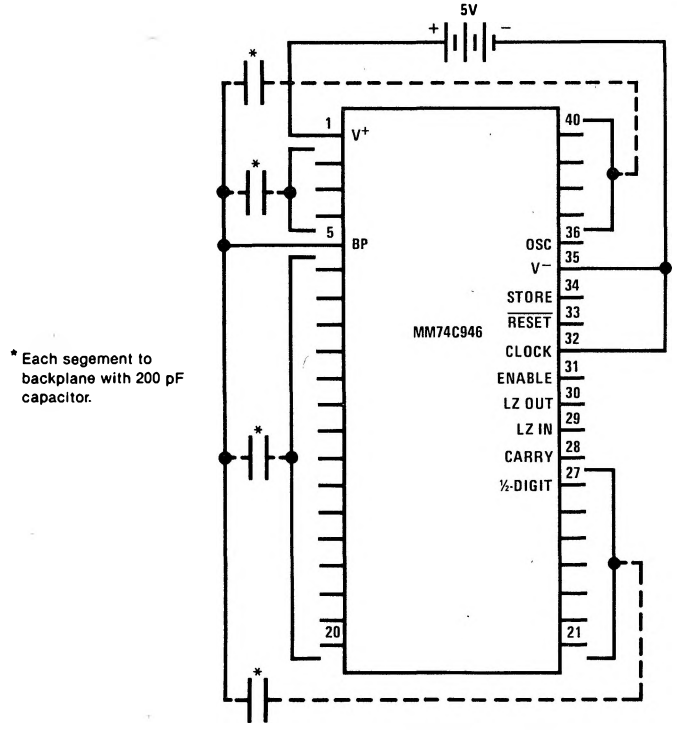
AC Waveforms



Segment Identification

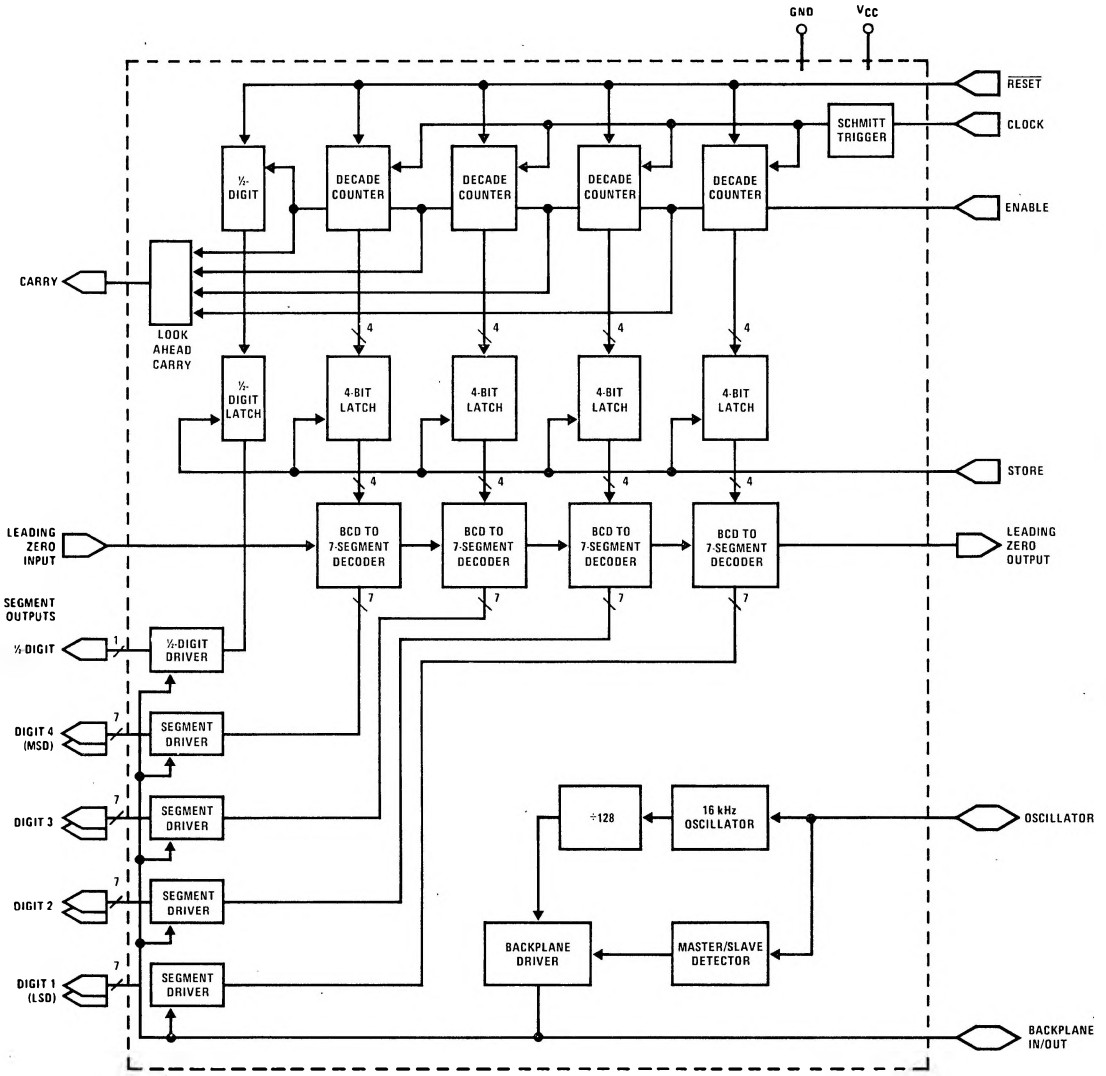


Test Circuit



* Each segement to backplane with 200 pF capacitor.

Block Diagram



Control Pin Description

Backplane In/Out—When the oscillator pin is grounded this pin is an input allowing an external device to generate the backplane waveform. When the oscillator pin is left open this pin is an output supplying backplane drive for an LCD.

Oscillator—The oscillator frequency may be lowered by tying a capacitor between this pin and ground. If this pin is grounded the backplane pin becomes an input.

Store Input—This controls the latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high data on counter outputs is stored in latches and displayed.

$\overline{\text{Reset}}$ Input—When low, counters are reset to zero.

Clock Input—Advances counter on negative edge.

Enable Input—When low, halts counter operation.

Leading Zero Input (LZI)—When high, enables leading zero blanking.

Leading Zero Output (LZO)—This signal goes high when counter equals zero and LZI is high.

Carry Output—Goes high for one clock period when count of 9999 is reached.

A1-G1—Digit 1 segment outputs.

A2-G2—Digit 2 segment outputs.

A3-G3—Digit 3 segment outputs.

A4-G4—Digit 4 segment outputs.

½-Digit Output—Goes high when count goes from 9999 to 0000 and stays high until $\overline{\text{Reset}}$ goes low.

Application Hints

Counter Circuitry Description

The MM74C946 contains a 4-digit resettable synchronous counter with a Schmitt trigger on the clock input. An additional D flip-flop clocked by the counter carry out provides a true ½-digit, or it can be used to indicate an overflow condition. The counters increment on the negative clock edge. The ½-digit sets on the negative clock edge which increments the counter past 9999. It can be reset only when the counter is reset by taking the reset pin to ground. The counter and carry output operation is independent of the state of the ½-digit flip-flop.

The carry output goes high on the negative edge of the clock when the transition from 9998 to 9999 occurs and then goes low on the next count. Thus counters may be cascaded in a ripple carry mode or synchronous mode by using the enable input.

The counter can be inhibited from responding to clock input pulses by taking the enable input low, thus freezing the counter to its state prior to the event.

The counter outputs feed a series of flow-through latches. When the store input is low, the latch outputs follow their inputs. When the store input is taken high, the contents of the counter are stored in the latches and are displayed.

The latch outputs feed 4 decimal to 7-segment decoders which include circuitry to provide leading zero blanking. When the leading zero input is low or the ½-digit is set, leading zero blanking is inhibited. When the leading zero input is high, all leading zeroes will be blanked. A leading zero output is provided to allow correct blanking of all leading zeroes in multiple device designs. This output will be high when all 4 digits are blanked. (Remember the leading zero input must be high and the ½-digit must be reset.)

Display Circuitry Description

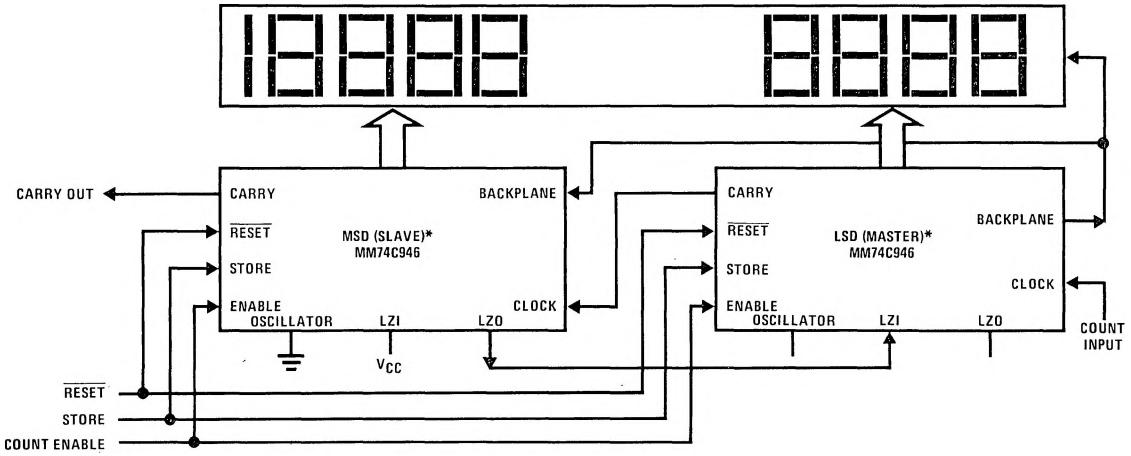
The MM74C946 has 30 segment outputs capable of directly driving 4 digits of 7 segments plus an additional ½-digit of 2 segments. The segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life.

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C946 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven by multiple counters. The maximum fanout of a master backplane driver is limited by its total capacitive load which is the sum of the slaved backplane input capacitances and the display backplane capacitance.

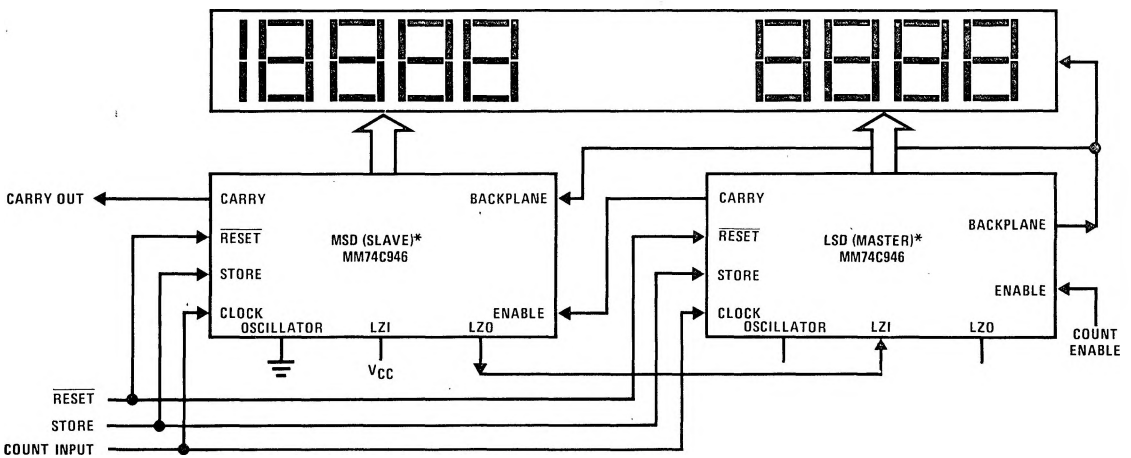
An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency typically is 125 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane will be put in the slave mode.

Typical Applications

Ripple Carry Cascading



Synchronous Cascading



* Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.