National Semiconductor

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the Invert/Non-invert control pin. A logical "0" on the Invert/Non-invert control pin selects active high true decoding at the Segment inputs. A logical "1" on the Invert/Non-invert control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The Error output goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE® condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable (OE).

The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-though condition when Latch Enable (LE) is at a logical "0", and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

3V-15V

0.45 V_{CC} (typ.)

1 TTL load

Features

- Wide supply range
- High noise immunity
- TTL compatible fan out
- Selectable active true inputs
- TRI-STATE outputs
- On-chip latch
- Error output
- Minus output



Absolute Maximum Ratings

| Voltage at Any Output | |
|-------------------------|------|
| Voltage at Any Input | |
| Operating Temperature R | ange |
| MM54C915 | |
| MM74C915 | |

- 0.3V to V_{CC} + 0.3V - 0.3V to 18V -55°C to +125°C -40°C to +85°C

| Storage Temperature Range | -65°C to +150°C |
|---------------------------------------|-----------------|
| Package Dissipation | 500 mW |
| Operating VCC Range | 3V to 15V |
| Maximum VCC | 18V |
| Lead Temperature, (Soldering, 10 seco | nds) 300°C |
| | |

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

| | PARAMETER | CONDITIONS | MIN | ТҮР | MAX | UNITS |
|--------------------|--|--|--|----------------------|-----------------|----------------|
| смоѕ то с | MOS | | | | l== | 4 |
| VIN(1) | Logical "1" Input Voltage | $V_{CC} = 5V$ $V_{CC} = 10V$ | 3.3 8 | 4.5 9 | | |
| VIN(0) | Logical "O" Input Voltage | V _{CC} = 15V V _{CC} = 5V V _{CC} = 10V V _{CC} = 15V | 12.5 | 0.5 1 1.5 | 1.5 2 2.5 | |
| ¹ IN(1) | Logical "1" Input Current | V _{IN} = 15V | | 0.005 | 1 | μA |
| | Logical "0" Input Current | VIN = OV | -1 | -0.005 | | μΑ |
| VOUT(1) | Logical "1" Output Voltage | I _O = 10 μA V _{CC} = 5V V _{CC} = 10V V _{CC} = 15V | | 4.5 9 13.5 | | v v v |
| VOUT(0) | Logical "O" Output Voltage | I _O = 10 μA V _{CC} = 5V V _{CC} = 10V V _{CC} = 15V | | 0.5 1 1.5 | | |
| ICC | Supply Current | $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$ | | 0.25 0.75 1.00 | 1 2.5 3 | mA mA mA |
| CMOS/TTL | INTERFACE | | | | | |
| VIN(1) | Logical "1" Input Voltage MM54C915 MM74C915 | V _{CC} = 4.5V V _{CC} = 4.75V | V _{CC} -1.7 V _{CC} -1.7 | | | v v |
| VIN(0) | Logical ''O'' Input Voltage MM54C915 MM74C915 | V _{CC} = 4.5V V _{CC} = 4.75V | | | 0.8 0.8 | v v |
| VOUT(1) | Logical ''1'' Output Voltage MM54C915 MM74C915 | I _O = -360 μA V _{CC} = 4.5V V _{CC} = 4.75V | 2.4 2.4 | | | v v |
| VOUT(0) | Logical "O" Output Voltage MM54C915 MM74C915 | IO = 1.6 mA V _{CC} = 4.5V V _{CC} = 4.75V | | | 0.4 0.4 | v v |
| OUTPUT D | RIVE (Short Circuit Current) | | | | | |
| ISOURCE | Output Source Current P-Channel | $T_{A} = 25^{\circ}C, V_{O} = 0V,$ (Note 2) $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$ | -1.75 -8 -15 | -3.3 -15 -25 | | mA mA mA |
| ISINK | Output ['] Sink Current N-Channel | $T_{A} = 25^{\circ}C, V_{O} = V_{CC}$ (Note 2) $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$ | 5 20 30 | 8 30 50 | | mA mA mA |

| (AnAme Fen | CONDITIONS | | | MAX | UNITS |
|------------------------------|--|--|---|--|---|
| Propagation Delay Time to | CL = 50 pF | 2 | | | |
| Logical "O" or a Logical "1" | V _{CC} = 5V | | 500 | 1000 | ns |
| | V _{CC} = 10V | | 300 | 600 | ns |
| | V _{CC} = 15V | | 300 | 600 | ns |
| Propagation Delay Time From | RL = 10k, CL = 10 pF | | | | |
| Logical "O" or Logical "1" | V _{CC} = 5V | | 110 | 200 | ns |
| into High Impedance State | V _{CC} = 10V | | 75 | 130 | ns |
| | V _{CC} = 15V | | 60 | 110 | ns |
| Propagation Delay Time From | RL = 10k, CL = 50 pF | | | | |
| High Impedance State to a | V _{CC} = 5V | | 150 | 250 | ns |
| Logical "O" or Logical "1" | V _{CC} = 10V | | 80 | 140 | ns |
| | V _{CC} ≈ 15V | | 70 | 125 | ns |
| Input Data Set-Up Time | С _L = 50 рF | | | | |
| | V _{CC} = 5V | | 500 | 1000 | ns |
| | V _{CC} = 10V | | 300 | 600 | ns |
| | V _{CC} = 15V | | 300 | 600 | ns |
| Input Data Hold Time | CL = 50 pF | | | | |
| | V _{CC} = 5V | 1 | -150 | 0 | ns |
| | V _{CC} = 10V | | -100 | 0 | ns |
| | V _{CC} = 15V | | -100 | 0 | ns |
| Input Capacitance | Any Input, (Note 3) | | 5 | 7.5 | pF |
| TRI-STATE Output Capaci- | Any Output, (Note 3) | | 10 | | pF |
| tance | | | | | |
| | Propagation Delay Time to Logical "O" or a Logical "1" Propagation Delay Time From Logical "O" or Logical "1" into High Impedance State Propagation Delay Time From High Impedance State to a Logical "O" or Logical "1" Input Data Set-Up Time Input Data Hold Time Input Capacitance TRI-STATE Output Capaci- | Propagation Delay Time to Logical "0" or a Logical "1" $C_L = 50 \text{ pr}$ $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$ Propagation Delay Time From Logical "0" or Logical "1" $R_L = 10k, C_L = 10 \text{ pF}$ $V_{CC} = 5V$ $V_{CC} = 5V$ Propagation Delay Time From High Impedance State $R_L = 10k, C_L = 50 \text{ pF}$ $V_{CC} = 15V$ Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1" $R_L = 10k, C_L = 50 \text{ pF}$ $V_{CC} = 5V$ $V_{CC} = 15V$ Input Data Set-Up Time $C_L = 50 \text{ pF}$ $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$ Input Data Hold Time $C_L = 50 \text{ pF}$ $V_{CC} = 5V$ $V_{CC} = 15V$ Input Data Hold Time $C_L = 50 \text{ pF}$ $V_{CC} = 15V$ Input Capacitance TRI-STATE Output Capaci-Any Output, (Note 3) | Propagation Delay Time to Logical "0" or a Logical "1" $C_L = 50 \text{ pr}$ VCC = 5V VCC = 15VVCC = 5V VCC = 15VPropagation Delay Time From Logical "0" or Logical "1" $R_L = 10k, C_L = 10 \text{ pF}$ VCC = 5V VCC = 10V VCC = 15VPropagation Delay Time From High Impedance State to a Logical "0" or Logical "1" $R_L = 10k, C_L = 50 \text{ pF}$ VCC = 15VPropagation Delay Time From High Impedance State to a Logical "0" or Logical "1" $R_L = 10k, C_L = 50 \text{ pF}$ VCC = 10V VCC = 15VInput Data Set-Up Time $C_L = 50 \text{ pF}$ VCC = 15VInput Data Hold Time $C_L = 50 \text{ pF}$ VCC = 15VInput Data Hold Time $C_L = 50 \text{ pF}$ VCC = 15VInput Capacitance TRI-STATE Output Capaci-Any Output, (Note 3) | Propagation Delay Time to Logical "0" or a Logical "1" $CL = 50 \text{ pr}$ 500VCC = 5V VCC = 10V VCC = 15V 300 300Propagation Delay Time From Logical "0" or Logical "1" into High Impedance State $R_L = 10k, C_L = 10 \text{ pF}$ $V_{CC} = 5V$ 110Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1" $R_L = 10k, C_L = 50 \text{ pF}$ $V_{CC} = 15V$ 60Propagation Delay Time From High Impedance State to a Logical "0" or Logical "1" $R_L = 10k, C_L = 50 \text{ pF}$ $V_{CC} = 15V$ 150Input Data Set-Up Time $C_L = 50 \text{ pF}$ $V_{CC} = 15V$ 500 300 300 $V_{CC} = 15V$ 300Input Data Hold Time $C_L = 50 \text{ pF}$ $V_{CC} = 15V$ -150 -100 -100Input Capacitance TRI-STATE Output Capaci-Any Input, (Note 3)5 | Propagation Delay Time to $C_L = 50 \text{ pr}$ Logical "0" or a Logical "1" $V_{CC} = 5V$ 500 1000 VCC = 10V 300 600 VCC = 15V 300 600 Propagation Delay Time From RL = 10k, CL = 10 pF 300 600 Logical "0" or Logical "1" VCC = 5V 110 200 into High Impedance State VCC = 10V 75 130 VCC = 15V 60 110 250 Propagation Delay Time From RL = 10k, CL = 50 pF 60 110 Propagation Delay Time From RL = 10k, CL = 50 pF 500 1000 VCC = 5V 150 250 250 Logical "0" or Logical "1" VCC = 10V 80 140 VCC = 10V 80 140 VCC = 15V 70 125 Input Data Set-Up Time CL = 50 pF 500 1000 00 VCC = 10V 300 600 1000 VCC = 15V 300 600 Input Data Hold Time CL = 50 pF VCC = 10V -150 0 0 0 Input Capacitance |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

Note 3: Capacitance is guaranteed by periodic testing.

| CHARACTER | BCD OUTPUTS | | | NON-BCD | | |
|-----------------|-------------|----|----|---------|---------|-------|
| AT SEGMENT | D | C | BA | | OUTPUTS | |
| INPUTS | 23 | 24 | 21 | 20 | ERROR | MINUS |
| a | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 . | 0 | 0 | 0 | 1 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 |
| Ч | 0 | 1 | 0 | 0 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 |
| Ь | 0 | 1 | 1 | 0 | 0 | 0 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 |
| B | 1 | 0 | 0 | 0 | 0 | 0 |
| Ч | 1 | 0 | 0 | 1 | 0 | 0 |
| q | 1 | 0 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 0 | 0 |
| с, | X | X | X | X | 1 | 1 |
| All other input | X | X | X | X | 1 | 0 |
| combinations | X | X | X | X | 1 | 0 |







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