National Semiconductor

MM54C192/MM74C192 Synchronous 4-Bit Up/Down Decade Counter
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General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters, while the MM54C193 and MM74C193 are binary counters.

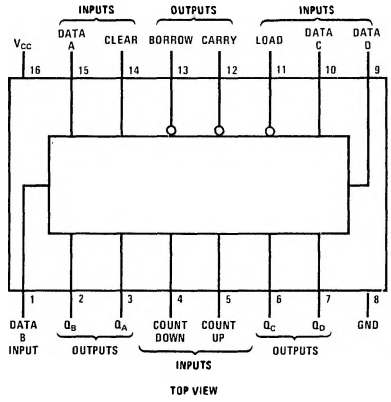
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

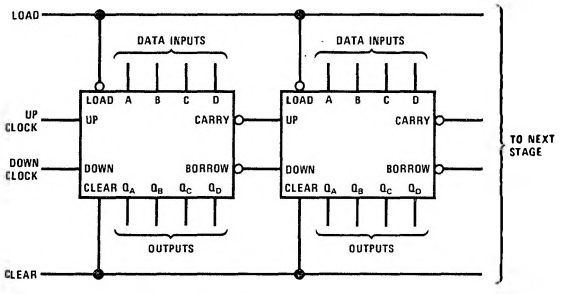
Features

- High noise margin — 1 V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3 V to 15 V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} (typ.)

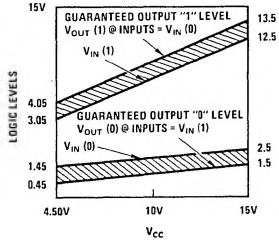
Connection Diagram



Cascading Packages



Guaranteed Noise Margin as A Function of V_{CC}



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$
Operating Temperature Range	
MM54C193	$-55°C$ to $+125°C$
MM74C193	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 15 V
Absolute Maximum V_{CC}	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

	Parameter	Conditions	Min.	Typ.	Max.	Units
	CMOS to CMOS					
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
	CMOS to Tenth Power Interface					
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
	Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

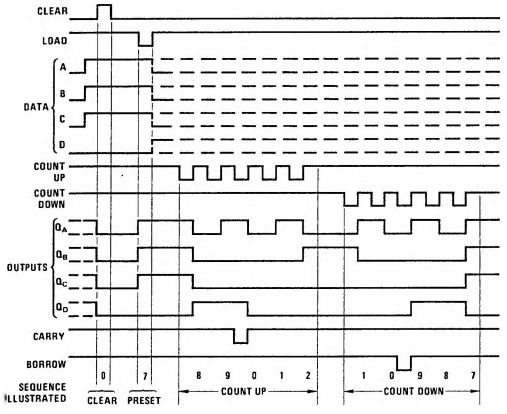
Parameter		Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to Q from Count Up or Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 100	400 160	ns ns
t_{pd}	Propagation Delay Time to Borrow from Count Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_{pd}	Propagation Delay Time to Carry from Count Up	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_S	Time Prior to Load that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 30	160 50	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 40	160 65	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to Q from Load	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Count Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 35	200 80	ns ns
f_{MAX}	Maximum Count Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.5 6	4 10		MHz MHz
t_r, t_f	Count Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			15 5	μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Timing Diagrams



Note I: Clear outputs to zero.
Note II: Load (preset) to binary thirteen.
Note III: Count up to fourteen, fifteen, carry, zero, one and two.
Note IV: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

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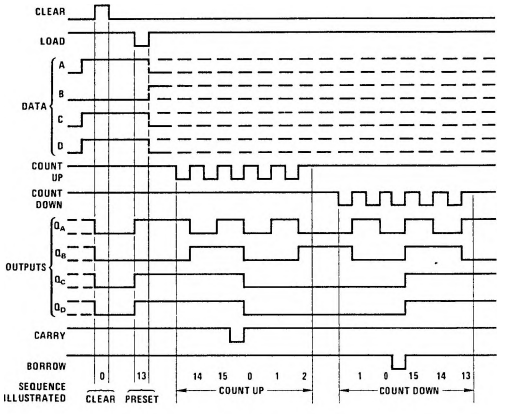

Note I: Clear outputs to zero.
Note II: Load (preset) to BCD seven.
Note III: Count up to eight, nine, carry, zero, one, and two.
Note IV: Count down to one, zero, borrow, nine, eight, and seven.

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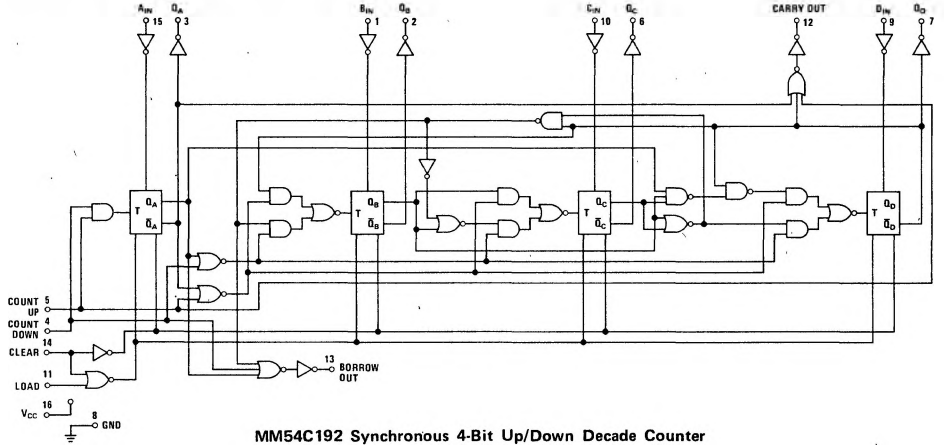
NOTE A: Clear overrides load, data, and count inputs.
NOTE B: When counting up, count down input must be high; when counting down, count-up input must be high.

Schematic Diagrams



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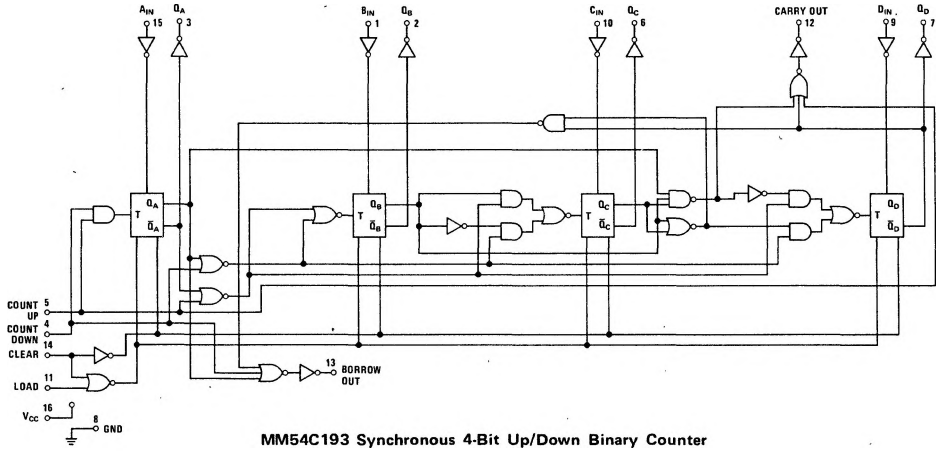

MM54C193 Synchronous 4-Bit Up/Down Binary Counter