



MM54C154/MM74C154 4-Line to 16-Line Decoder/Demultiplexer

General Description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

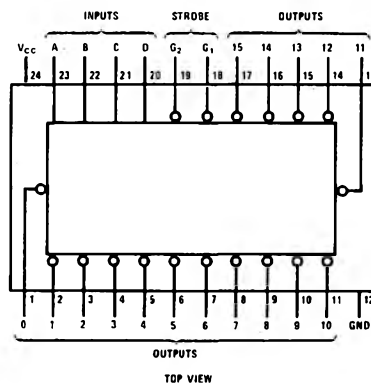
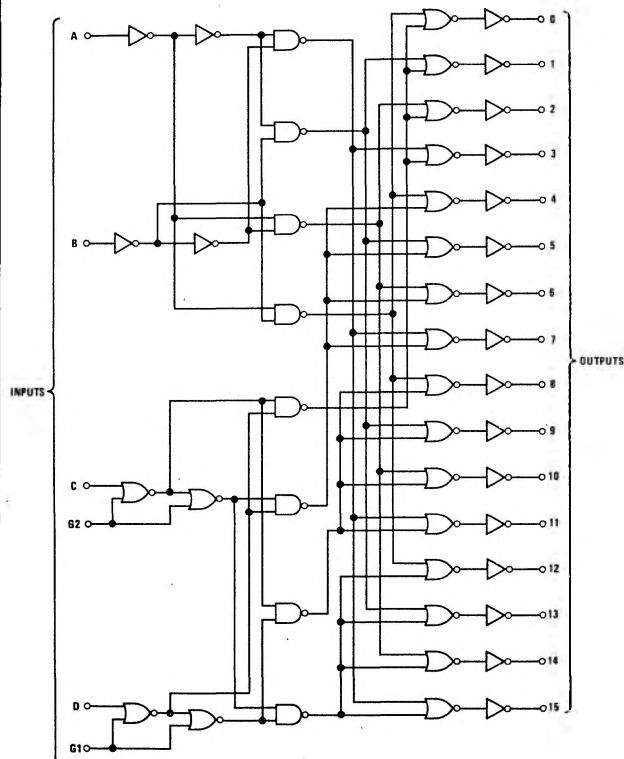
Features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise margin 1V guaranteed
- High noise immunity 0.45 V_{CC} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC}+0.3$ V
Operating Temperature Range	
MM54C154	-55°C to +125°C
MM74C154	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum V_{CC} Voltage	18 V
Package Dissipation	500 mW
Operating V_{CC} Range	3 V to 15 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max./min. limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS					
$V_{IN(1)}$ Logical "1" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V	3.5 8.0			V V
$V_{IN(0)}$ Logical "0" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V			1.5 2.0	V V
$V_{OUT(1)}$ Logical "1" Output Voltage	$V_{CC} = 5.0$ V, $I_O = -10$ μ A $V_{CC} = 10$ V, $I_O = -10$ μ A	4.5 9.0			V V
$V_{OUT(0)}$ Logical "0" Output Voltage	$V_{CC} = 5.0$ V, $I_O = +10$ μ A $V_{CC} = 10$ V, $I_O = +10$ μ A			0.5 1.0	V V
$I_{IN(1)}$ Logical "1" Input Current	$V_{CC} = 15$ V, $V_{IN} = 15$ V		0.005	1.0	μ A
$I_{IN(0)}$ Logical "0" Input Current	$V_{CC} = 15$ V, $V_{IN} = 0$ V	-1.0	-0.005		μ A
I_{CC} Supply Current	$V_{CC} = 15$ V		0.05	300	μ A
CMOS to LPTTL Interface					
$V_{IN(1)}$ Logical "1" Input Voltage	54C $V_{CC} = 4.5$ V 74C $V_{CC} = 4.75$ V	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$ Logical "0" Input Voltage	54C $V_{CC} = 4.5$ V 74C $V_{CC} = 4.75$ V			0.8 0.8	V V
$V_{OUT(1)}$ Logical "1" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = -100$ μ A 74C $V_{CC} = 4.75$ V, $I_O = -100$ μ A	2.4 2.4			V V
$V_{OUT(0)}$ Logical "0" Output Voltage	54C $V_{CC} = 4.5$ V, $I_O = 360$ μ A 74C $V_{CC} = 4.75$ V, $I_O = 360$ μ A			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)					
I_{SOURCE} Output Source Current	$V_{CC} = 5.0$ V, $V_{IN(0)} = 0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = 0$ V	-1.75			mA
I_{SOURCE} Output Source Current	$V_{CC} = 10$ V, $V_{IN(0)} = 0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = 0$ V	-8.0			mA
I_{SINK} Output Sink Current	$V_{CC} = 5.0$ V, $V_{IN(1)} = 5.0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK} Output Sink Current	$V_{CC} = 10$ V, $V_{IN(1)} = 10$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise noted.

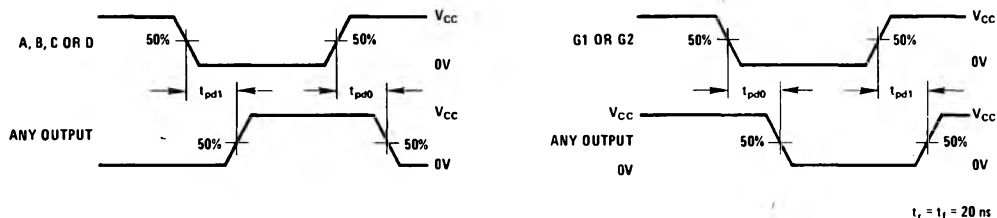
Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}	Propagation Delay to a Logical "0" From Any Input to Any Output $V_{CC} = 5.0\text{ V}$, $V_{CC} = 10\text{ V}$		275 100	400 200	ns ns
t_{pd0}	Propagation Delay to a Logical "0" from G1 or G2 to Any Output $V_{CC} = 5.0\text{ V}$, $V_{CC} = 10\text{ V}$		275 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from Any Input to Any Output $V_{CC} = 5.0\text{ V}$, $V_{CC} = 10\text{ V}$		265 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from G1 or G2 to Any Output $V_{CC} = 5.0\text{ V}$, $V_{CC} = 10\text{ V}$		265 100	400 200	ns ns
C_{IN}	Input Capacitance (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance (Note 3)		60		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



Truth Table

INPUTS					OUTPUTS																
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition