

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers **MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE® Hex Inverters**

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

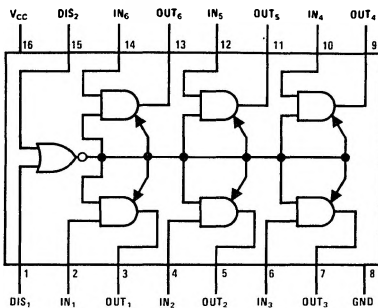
Features

- Wide supply voltage range 3.0 V to 15 V
- Guaranteed noise margin 1.0 V
- High noise immunity 0.45 V_{CC} (typ.)
- TTL compatible drive 1 TTL Load

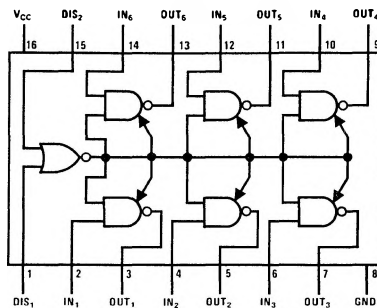
Applications

- Bus drivers Typical propagation delay
into 150pF load is 40ns.

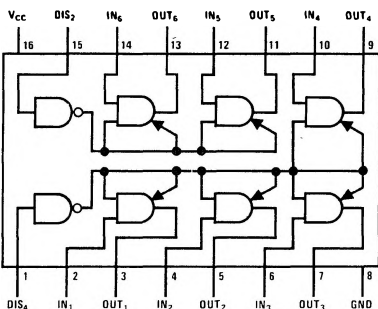
Connection Diagrams (Dual-In-Line and Flat Packages)

MM70C95/MM80C95


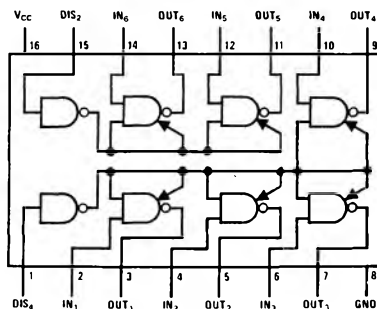
TOP VIEW

MM70C96/MM80C96


TOP VIEW

MM70C97/MM80C97


TOP VIEW

MM70C98/MM80C98


TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	-0.3 V to $V_{CC} + 0.3$ V
Operating Temperature Range	
MM70CXX	-55°C to +125°C
MM80CXX	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Package Dissipation	500 mW
Power Supply Voltage (V_{CC})	18 V
Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics

Max./min. limits apply across temperature range, unless otherwise noted.

Parameter		Conditions	Min.	Typ.	Max.	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0$ V $V_{CC} = 10$ V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0$ V, $V_{CC} = 10$ V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15$ V		0.005	1.0	μ A
$I_{IN(0)}$	Logical "0" Input Current		-1.0	-0.005		μ A
I_{OUT}	Output Current in High Impedance State	$V_{CC} = 15$ V, $V_O = 15$ V $V_{CC} = 15$ V, $V_O = 0$ V		0.005 -0.005	1.0	μ A μ A
I_{CC}	Supply Current	$V_{CC} = 15$ V		0.01	15	μ A
TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	70C $V_{CC} = 4.5$ V 80C $V_{CC} = 4.75$ V	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	70C $V_{CC} = 4.5$ V 80C $V_{CC} = 4.75$ V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	70C $V_{CC} = 4.5$ V, $I_O = -1.6$ mA 80C $V_{CC} = 4.75$ V, $I_O = -1.6$ mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	70C $V_{CC} = 4.5$ V, $I_O = 1.6$ mA 80C $V_{CC} = 4.75$ V, $I_O = 1.6$ mA			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0$ V, $V_{IN(1)} = 5.0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = 0$ V	-4.35			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10$ V, $V_{IN(1)} = 10$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = 0$ V	-20			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0$ V, $V_{IN(0)} = 0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = V_{CC}$	4.35			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10$ V, $V_{IN(0)} = 0$ V $T_A = 25^\circ\text{C}$, $V_{OUT} = V_{CC}$	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics $T_A = 25^\circ\text{C}$, $C_L = 50\text{pF}$, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0} , t_{pd1} Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM70C95/MM80C95, MM70C97/MM80C97 MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$		60 25 70 35	100 40 150 75	ns ns ns ns
t_{pd0} , t_{pd1} Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output MM70C95/MM80C95, MM70C97/MM80C97 MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0\text{V}$, $C_L = 150\text{pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{pF}$ $V_{CC} = 5.0\text{V}$, $C_L = 150\text{pF}$ $V_{CC} = 10\text{V}$, $C_L = 150\text{pF}$		85 40 95 45	160 80 210 110	ns ns ns ns
t_{1H} , t_{0H} Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0") MM70C95/MM80C95 MM70C96/MM80C96 MM70C97/MM80C97 MM70C98/MM80C98	$R_L = 10\text{k}$, $C_L = 5.0\text{pF}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$		80 50 100 70 70 50 90 70	135 90 180 125 125 90 170 125	ns ns ns ns ns ns ns ns
t_{H1} , t_{H0} Delay from Disable Input to Logical "1" Level (from High Impedance State) MM70C95/MM80C95 MM70C96/MM80C96 MM70C97/MM80C97 MM70C98/MM80C98	$R_L = 10\text{k}$, $C_L = 50\text{pF}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$ $V_{CC} = 5.0\text{V}$ $V_{CC} = 10\text{V}$		120 50 130 60 95 40 120 50	200 90 225 110 175 80 200 90	ns ns ns ns ns ns ns ns
C_{IN} Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT} Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD} Power Dissipation Capacitance	(Note 3)		60		pF

Truth Table

MM70C95/MM80C95

DISABLE DIS ₁	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

DISABLE DIS ₁	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE DIS ₄	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

MM70C98/MM80C98

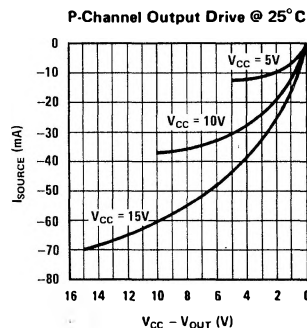
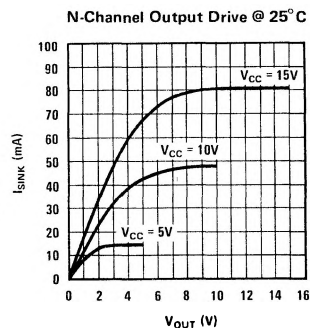
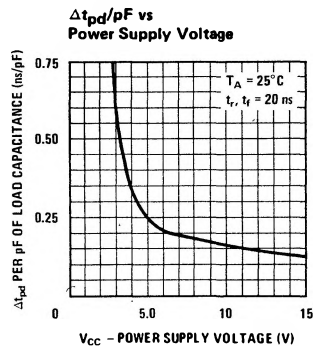
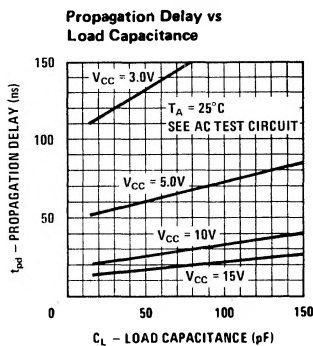
DISABLE DIS ₄	INPUT DIS ₂	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only

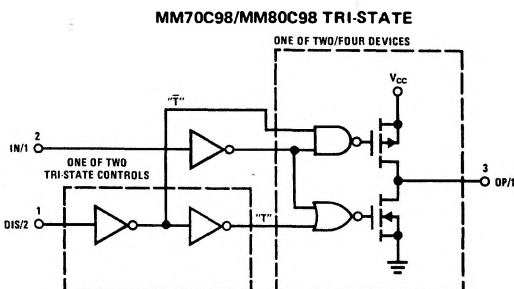
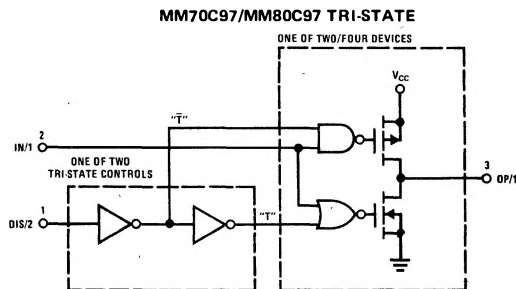
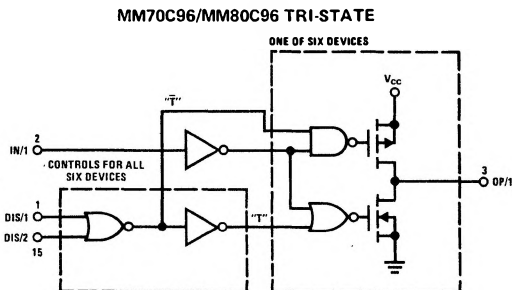
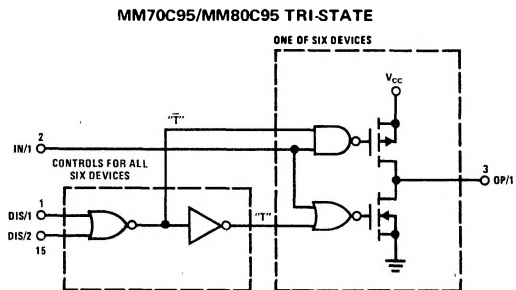
**Output 1-4 only

X = Irrelevant

Typical Performance Characteristics



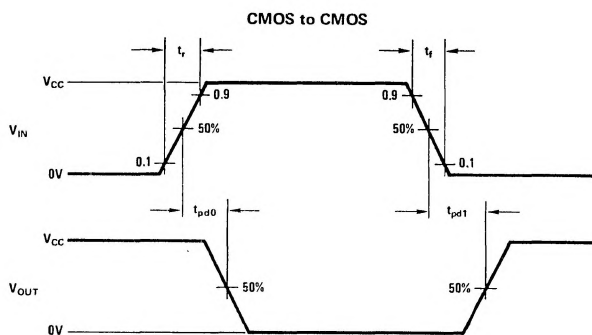
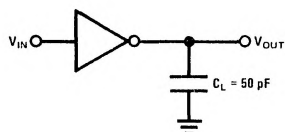
Schematic Diagram



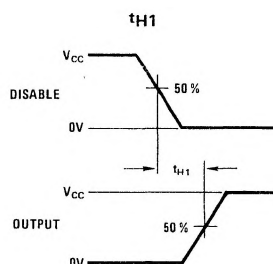
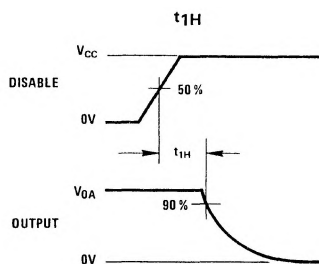
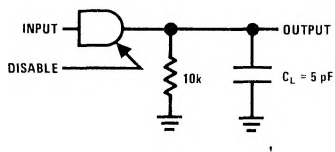
AC Test Circuit and Switching Time Waveforms

MM70C95/MM80C95, MM70C97/MM80C97,
MM70C96/MM80C96, MM70C98/MM80C98

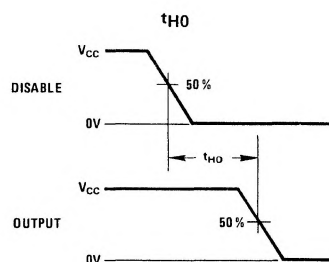
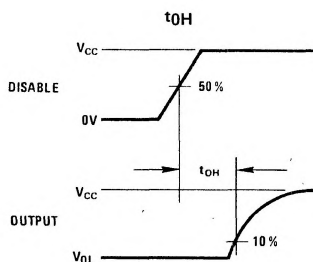
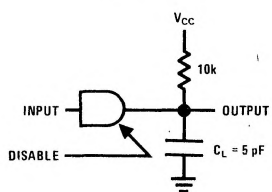
t_{pd0} , t_{pd1}



t_{1H} and t_{H1}



t_{0H} and t_{H0}



Note: Delays measured with input t_r , $t_f \leq 20$ ns