

FEATURES

- 44 hr. min., 125°C burn-in plus industrial screening for greater reliability (see Figure 6 for processing description)
- -40°C to 85°C temperature range
- □ Two speeds
 - 2.5 MHz MKI3880(P)-70 (Z80 CPU)
 - 4.0 MHz MKI3880(P)-74 (Z80A CPU)

DESCRIPTION

The Mostek Z80 family of components is a significant advancement in the state-of-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could deliver previously. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and, in most cases, data that is to be processed. For example, a typical instruction sequence may be to read data from a

- Single 5-Volt supply and single-phase clock required
- Software compatible with 8080A CPU
- Complete development and OEM system product support
- □ Military MKB version available (-55°C/125°C)
- Typical power 625 mW

specific peripheral device, store it in a location in memory, check the parity, and write it out to another peripheral device. Note that the Mostek component set includes the CPU and various general purpose I/O device controllers, as well as a wide range of memory devices. Thus, all required components can be connected together in a very simple manner with virtually no other external logic. The user's effort then becomes primarily one of the software development. That is, the user can concentrate on describing his problem and translating it into a series of instructions that can be loaded into the microcomputer memory. Mostek is dedicated to making this step of software generation as simple as possible. A good example of this is our assembly language in which a simple mnemonic is used to represent every instruction that the CPU can perform. This language is self-documenting in such a way that from the mnemonic the user can understand exactly what the instruction is doing without constantly checking back to a complex cross listing. Please refer to the Z80 Data Book for extensive Z80 operation documentation.



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	40°C to +85°C
Storage Temperature	65°C to +150°C
Voltage on Any Pin with Respect to Ground	\ldots -0.3 V to +7 V
Power Dissipation	1.5 W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to 85°C, V_{CC} = 5 V \pm 5% unless otherwise specified)

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	TEST CONDITIONS
V _{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
VIHC	Clock Input High Voltage	V _{CC} 6		V _{cc} +.3	v	8
V _{IL}	Input Low Voltage	-0.3		0.8	v	
V _{IH}	Input High Voltage All inputs except NMI	2.4		V _{cc}	V	
V _{IH(NMI)}	Input High Voltage (NMI)	2.7		V _{cc}	v	

DC ELECTRICAL CHARACTERISTICS

(T_A = -40°C to 85°C, V_{CC} = 5 V \pm 5% unless otherwise specified)

SYM	PARAMETER	MIN	ТҮР	MAX	UNITS	TEST CONDITIONS
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 1.8mA
V _{он}	Output High Voltage	2.4			v	I _{OH} = -250 μA
Icc	Power Supply Current			200	mA	
I _{LI}	Input Leakage Current			±10	μA	$V_{IN} = 0$ to V_{CC}
ILOH	Tri-State Output Leakage Current in Float			10	μΑ	V_{OUT} = 2.4 to V_{CC}
ILOL	Tri-State Output Leakage Current in Float			-10	μΑ	V _{OUT} = 0.4V
ILD	Data Bus Leakage Current In Input Mode			±10	μΑ	0 < V _{IN} < V _{CC}

AC ELECTRICAL CHARACTERISTICS

MKI3880(P)-70 Z80-CPU ($T_A = -40^{\circ}$ C to 85°C, $V_{CC} = +5$ V, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
φ	t _c t _w (ΦΗ) t _w (ΦL) t _r f	Clock Period Clock Pulse Width, Clock High Clock Pulse Width, Clock Low Clock Rise and Fall Time	.4 180 180	[12] (D) 2000 30	μsec nsec nsec nsec	
	t _{D(AD)} t _{F(AD)} t _{acm}	Address Output Delay Delay to Float Address Stable Prior to MREQ (Memory Cycle)	[1]	145 110	nsec nsec nsec	C _L = 50pF
A ₀₋₁₅	t _{aci}	Address Stable Prior to IORO, RD or WR (I/O Cycle)	[2]		nsec	
	t _{ca}	Address Stable From RD, WR, IORQ or MREQ	[3]	{	nsec	Except T3-M1
	t _{caf}	Address Stable From RD or WR During Float	[4]		nsec	
	t _{D(D)} t _{F(D)} t _{SΦ(D)}	Data Output Delay Delay to Float During Write Cycle Data Setup Time to Rising Edge of Clock During M1 Cycle	50	250 90	nsec nsec nsec	
D ₀₋₇	^t S∓(D)	Data Setup Time to Falling Edge at Clock During M2 to M5	60		nsec	C _L = 50pF
	t _{dcm}	Data Stable Prior to WR (Memory Cycle)	[5]		nsec	
	t _{dci} t _{cdf} t _H	Data Stable Prior to WR (I/O Cycle) Data Stable From WR Input Hold Time	[6] [7] O		nsec nsec nsec	
	tDLo(MR)	MREQ Delay From Falling Edge of	1	100	nsec	
MREQ	t _{DHΦ(MR)}	MREQ Delay From Rising Edge of Clock, MREQ High		100	nsec	
	t _{DH} \$(MR)	MREQ Delay From Falling Edge of Clock, MREQ High		100	nsec	C _L = 50pF
	t _{w(MRL)} t _{w(MRH)}	Pulse Width, MREO Low Pulse Width, MREO High	[8] [9]		nsec nsec	
	^t DLΦ(IR)	IORQ Delay From Rising Edge of Clock, IORQ Low		90	nsec	
IORO	^t DL∓(IR)	IORQ Delay From Falling Edge of Clock, IORQ Low		110	nsec	C _L = 50pF
	t _{DHΦ(IR)}	IORO Delay From Rising Edge of Clock, IORO High		100	nsec	
	t _{DH} €(IR)	IORQ Delay From Falling Edge of Clock, IORQ High		110	nsec	
	t _{DL} (RD)	RD Delay From Rising Edge of Clock,		100	nsec	
RD	t _{DL} (RD)	RD Delay From Falling Edge of Clock,		130	nsec	C _L = 50pF
	t _{DHΦ(RD)}	RD Delay From Rising Edge of Clock,		100	nsec	
	^t DH⊕(RD)	RD Delay From Falling Edge of Clock, RD High		110	nsec	

AC ELECTRICAL CHARACTERISTICS (Cont.)

(T_A = -40°C to 85°C, V_{CC} = +5 V, \pm 5%, unless otherwise noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
	t _{DLΦ} (WR)	WR Delay From Rising Edge of Clock, WR Low		80	nsec	
WR		WR Delay From Falling Edge of Clock, WR Low		90	nsec	C _L = 50pF
	^t DHΦ(WR)	WR Delay From Falling Edge of Clock, WR High		100	nsec	
	tw(WRL)	Pulse Width, WR Low	[10]		nsec	
MI	t _{DL(M1)}	M1 Delay From Rising Edge of Clock M1 Low		130	nsec	C ₁ = 50pF
	t _{DH(M1)}	M1 Delay From Rising Edge of Clock, M1 High		130	nsec	2
RFSH	t _{DL(RF)}	RFSH Delay From Rising Edge of Clock,		180	nsec	C. = 30pF
	t _{DH(RF)}	RFSH Delay From Rising Edge of Clock RFSH High		150	nsec	
WAIT	t _{S(WT)}	WAIT Setup Time to Falling Edge of Clock	70		nsec	
HALT	t _{D(HT)}	HALT Delay Time From Falling Edge of Clock		300	nsec	C _L = 50pF
ÎNT	t _{s(IT)}	INT Setup Time to Rising Edge of Clock	80		nsec	
NMI	tw(NML)	Pulse Width, NMI Low	80		nsec	
BUSRO	t _{s(BQ)}	BUSRO Setup Time to Rising Edge of Clock	80		nsec	
BUSAK	t _{DL(BA)}	BUSAK Delay From Rising Edge of		120	nsec	C. = 50pF
	t _{DH(BA)}	BUSAK Delay From Falling Edge of Clock, BUSAK High		110	nsec	
RESET	t _{s(RS)}	RESET Setup Time to Rising Edge of Clock	90		nsec	
	t _{F(C)}	Delay to/from Float (MREQ, IORQ, RD and WRI)		80	nsec	
	t _{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

NOTES:

A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.

B. The RESET signal must be active for a minimum of 3 clock cycles.

C. Output Delay vs. Load Capacitance

 $T_A = 85^{\circ}C V_{CC} = 5V \pm 5\%$

Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.

D. Although static by design, testing guarantees t_W (\PhiH) of 200 μsec maximum. t_{acm} = t_w (ΦH) + t_f -75 111

[2]

- $t_{aci} = t_c -80$ $t_{ca} = t_W (\Phi L) + t_r -40$ $t_{caf} = t_W (\Phi L) + t_r -60$ [3]
- [4]
- [5] t_{dcm} = t_c -210

[6]
$$t_{dci} = t_W (\Phi L) + t_r - 210$$

7]
$$t_{cdf} = t_{w} (\Phi L) + tr -80$$

- $t_{cdf} = t_{w} (\Psi L) + t_{f}$ $t_{w} (MRL) = t_{c} -40$ $t_{w} (MRH) = t_{w} (\Phi H) + t_{f} -70$ (8) [9]
- [10]
- $t_W(WR) = t_c -40$

[11] $t_{mr} = 2t_c + t_w (\Phi H) + t_f -80$ [12] $t_c = t_w (\Phi H) + t_w (\Phi L) + t_r + t_f$



AC ELECTRICAL CHARACTERISTICS

MKI3880(P)-74 Z80A-CPU ($T_A = -40^{\circ}$ C to 85°C, $V_{CC} = +5V$, ±5%, Unless Otherwise Noted)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
Φ	t _c t _w (ΦH) t. (ΦL)	Clock Period Clock Pulse Width, Clock High Clock Pulse Width, Clock Low	.25 110 110	[12] (D) 2000	µsec nsec nsec	
	t _r ,f	Clock Rise and Fall Time		30	nsec	
	t _{D(AD)}	Address Output Delay		110	nsec	
	t _{F(AD)} t _{acm}	Address Stable Prior to MREQ	[1]	90	nsec	C _L = 50pF
A ₀₋₁₅	t _{aci}	Address Stable Prior to IORO, RD or WR (I/O Cycle)	[2]		nsec	
	t _{ca}	Address Stable From RD, WR, IORQ or MREQ	[3]		nsec	Except T3-M1
	t _{caf}	Address Stable From RD or WR During Float	[4]		nsec	
	^t D(D)	Data Output Delay		170	nsec	
ļ		Delay to Float During Write Cycle Data Setup Time to Rising Edge of	35	90	nsec	
ļ	*SΦ(D)	Clock During M1 Cycle				
D ₀₋₇	tS⊕(D)	Data Setup Time to Falling Edge at Clock During M2 to M5	50		nsec	C _L = 50pF
	t _{dcm}	Data Stable Prior to WR (Memory Cycle)	[5]		nsec	
	t _{dci}	Data Stable Prior to WR (I/O Cycle)	[6]		nsec	
	t _{cdf}	Input Hold Time	0		nsec	
		MREQ Delay From Falling Edge of	20	85	nsec	
MREQ	t _{DHΦ(MR)}	MREQ Delay From Rising Edge of Clock, MREQ High		85	nsec	
	^t DH⊕(MR)	MREQ Delay From Falling Edge of Clock, MREQ High		85	nsec	C _L = 50pF
	tw(MRL)	Pulse Width, MREQ Low	[8]		nsec	
	tw(MRH)	Pulse Width, MREQ High	[9]		nsec	
	t _{DLΦ} (IR)	IORQ Delay From Rising Edge of Clock, IORQ Low		75	nsec	
IORQ	^t DL∳(IR)	IORQ Delay From Falling Edge of Clock, IORQ Low		85	nsec	C _L = 50pF
	t _{DH} ∓(IR)	IORQ Delay From Rising Edge of Clock, IORQ High		85	nsec	
	t _{DHΦ(IR)}	IORQ Delay From Falling Edge of Clock, IORQ High		85	nsec	
- C P	t _{DLΦ(RD)}	RD Delay From Rising Edge of Clock, RD Low		85	nsec	
RD	tDL&(RD)	RD Delay From Falling Edge of Clock, RD Low		95	nsec	C _L = 50pF
	tDH4(RD)	RD Delay From Rising Edge of Clock, RD High		85	nsec	
	t _{DH} @(RD)	RD Delay From Falling Edge of Clock, RD High		85	nsec	

AC ELECTRICAL CHARACTERISTICS (Cont.)

(T_A = -40°C to 85°C, V_{CC} = +5 V, \pm 5%, unless otherwise noted)

SIGNAL	SYM	PARAMETER	MIN	МАХ	UNIT	TEST CONDITIONS
	t _{DL} (WR)	WR Delay From Rising Edge of Clock, WR Low		65	nsec	
WR	t _{DL} (WR)	WR Delay From Falling Edge of Clock, WR Low		80	nsec	C _L = 50pF
	t _{DHΦ(WR)}	WR Delay From Falling Edge of Clock, WR High		80	nsec	
	tw(WRL)	Pulse Width, WR Low	[10]		nsec	
M1	t _{DL(M1)}	M1 Delay From Rising Edge of Clock M1 Low		100	nsec	C ₁ = 50pF
	t _{DH(M1)}	M1 Delay From Rising Edge of Clock, M1 High		100	nsec	
RFSH	t _{DL(RF)}	RFSH Delay From Rising Edge of Clock,		130	nsec	$C_{\rm c} = 50 \rm pF$
	t _{DH(RF)}	RFSH Delay From Rising Edge of Clock RFSH High		120	nsec	
WAIT	t _{S(WT)}	WAIT Setup Time to Falling Edge of Clock	70		nsec	
HALT	t _{D(HT)}	HALT Delay Time From Falling Edge of Clock		300	nsec	C _L = 50pF
INT	t _{s(IT)}	INT Setup Time to Rising Edge of Clock	80		nsec	
NMI	tw(NML)	Pulse Width, NMI Low	80		nsec	
BUSRO	t _{s(BQ)}	BUSRO Setup Time to Rising Edge of Clock	50		nsec	
BUSAK	t _{DL(BA)}	BUSAK Delay From Rising Edge of		100	nsec	$C_{\rm c} = 50 \mathrm{pF}$
	t _{DH(BA)}	BUSAK Delay From Falling Edge of Clock, BUSAK High		100	nsec	
RESET	t _{s(RS)}	RESET Setup Time to Rising Edge of Clock	60		nsec	
	t _{F(C)}	Delay to/From Float (MREQ, IORQ, RD and WR)		80	nsec	
	t _{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

NOTES:

A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.

B. The RESET signal must be active for a minimum of 3 clock cycles.

C. Output Delay vs. Load Capacitance $T_A = 85^{\circ}C V_{CC} = 5V \pm 5\%$

Add 10 nsec delay for each 50pF increase in load up to a maximum of 200pF for the data bus and 100pF for address and control lines.

D. Although static by design, testing guarantees $t_{\rm W}$ (ΦH) of 200 μsec maximum. [1]

- [2]
- $t_{acm} = t_w (\Phi H) + t_f -65$ $t_{aci} = t_c -70$ $t_{ca} = t_w (\Phi L) + t_f -50$ [3]
- [4] $t_{caf} = t_W (\Phi L) + t_r - 45$ (C)

$$t_{dci} = t_{w} (\Phi L) + t_{r} - 170$$

- [7] $t_{cdf} = t_{W} (\Phi L) + t_{r} -70$ $t_{W} (MRL) = t_{c} -30$
- [8]
- t_{W} (MRH) = t_{W} (Φ H) + t_{f} -40 [9]

 $t_W (\overline{WR}) = t_C - 30$ [10] in n $t_{mr} = 2t_c + t_w (\Phi H) + t_f - 65$

[12]
$$t_c = t_w (\Phi H) + t_w (\Phi L) + t_r + t_f$$



XIV-16

CAPACITANCE

 $T_{\Delta} = 25^{\circ}C$, f = 1 MHz

SYM	PARAMETER	MAX	UNIT	TEST CONDITIONS
СФ	Clock Capacitance	35	pF	Unmeasured Pins
C _{IN}	Input Capacitance	5	pF	Returned to Ground
С _{ОUT}	Output Capacitance	10	pF	

"0"

.8 V

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CLOCK

AC TIMING DIAGRAM

Figure 5

Timing measurements are made at the following voltages, unless otherwise specified.



MKI INDUSTRIAL HI-REL SCREENING Figure 6

	Screen	MIL-STD 883 Method	Reqmt.
Package Assembly	Die Inspect Pre-Seal Inspect	75X Mostek Spec. 30X-60X Mostek Spec.	100% 100%
Environmental	Temperature Cycle Centrifuge Fine Leak Gross Leak	1010 Cond. C, 5 Cycles 2001 Cond. D, 20Kg Y ₁ 1014 Cond. B, 1 X 10 ⁻⁷ atm cc/sec Mostek Spec.	100% 100% 100% 100%
Electrical	Electrical Screens	5005 Grp. A electrical sub-groups, testing condi- tions and limits which guarantee ac, dc and functional performance over the full temperature range.	100%
Voltage Stress (DRAMs only)	1	1015 Cond. D, 10 hrs. min., 125°C	100%
Burn-in		1015 Cond. D, 44 hrs. min., 125°C	100%
QA Acceptance	Hermeticity Electrical Tests Visual/Mechanical Solderability Pre-shipment Inspect.	Fine and gross leak samples 5005 Grp. A sample testing to guarantee performance to data sheet over full temp. range. Visual tests to guarantee marking, construction and mechanical integrity	.25% AQL .4% AQL .65% AQL LTPD 10 .65% AQL