PRELIMINARY

PROCESSED TO MIL-STD-883, METHOD 5004, CLASS B, 16,384 x 1 BIT-DYNAMIC RAM MKB4516(P/J/E) - 80/81/82

FEATURES

- Military temperature range: $-55°C \leq T_C \leq +110°C$
- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- 100 ns access time, 235 ns cycle time (MKB4516-80)
  120 ns access time, 270 ns cycle time (MKB4516-81)
  150 ns access time, 320 ns cycle time (MKB4516-82)
- Common I/O capability using "early write"
- Interchangeable with M2118
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and are protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MKB4564 (64K RAM)
- 128 refresh cycles (2 msec)
- Available to the DESC part number 8101501EX
- Indefinite D_{OUT} hold using $\overline{CAS}$ control

DESCRIPTION

The MKB4516 is a single +5 V power supply version of the industry standard MKB4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MKB4516 are achieved by state-of-the-art circuit device techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatibility, and +5 V operation.

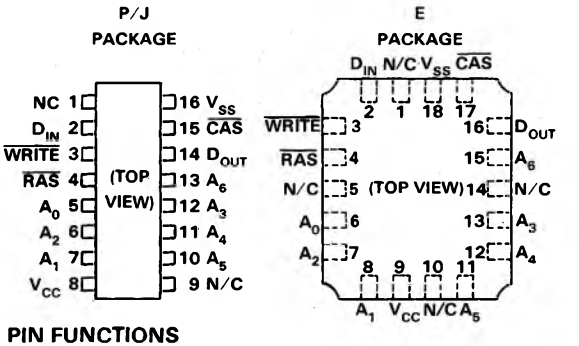
The MKB4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH. The output of the MKB4516 can be held valid indefinitely by holding $\overline{CAS}$ active low. This is quite useful since a refresh cycle can be performed while holding data valid from a previous cycle.

The MKB4516 is designed to be compatible with JEDEC standards for the 64K x 1 dynamic RAM. It is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. Compatibility with the MKB4564 will also permit a common board design to service both the MKB4516 and the MKB4564 (64K RAM) designs. The MKB4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MKB4027 did for the MKB4116.

The small memory user need no longer pay a three power supply penalty for achieving the economics of using dynamic RAM over static RAM with this new generation device.

PIN OUT

Figure 1



PIN FUNCTIONS

A_0 - A_6	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Col. Address Strobe	$\overline{WRITE}$	Read/Write Input
D_{IN}	Data In	$\overline{RFSH}$	Refresh
D_{OUT}	Data Out	V_{CC}	Power (+5 V)
NC	Not Connected	V_{SS}	GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -2.0 V to +7.0 V
Operating Temperature, T_C (Case) ..... -55°C to +110°C
Storage Temperature ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_C ≤ 110°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	2,17

DC ELECTRICAL CHARACTERISTICS

(-55°C ≤ T_C ≤ 110°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)		38	mA	3
I_{CC1}	Operating Current (T_C = 110°C)		30	mA	3,18
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH} D_{OUT} = High Impedance)		4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)		32	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		35	mA	3
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (0 V ≤ V_{IN} ≤ +5.5 V, all other pins not under test = 0 volts	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA	2.4	 0.4	V V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATION CONDITIONS (4, 5, 9)

($-55°C \leq T_C \leq 110°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4516-80		MK4516-81		MK4516-82		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RELREL}	t_{RC}	Random read or write cycle time	235		270		320		ns	6
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	285		320		410		ns	6
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	125		145		190		ns	6
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		100		120		150	ns	7
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		55		65		80	ns	8
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	45	0	50	0	60	ns	9
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	110		120		135		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	115	10^4	140	10^4	175	10^4	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	70		85		105		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	100		120		165		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	55	10^4	65	10^4	95	10^4	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	45	25	55	25	70	ns	10
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		0		0		ns	11
t_{AVREL}	t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row Address hold time	15		15		15		ns	
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column Address hold time	15		15		20		ns	
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	60		70		90		ns	
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	11
t_{CELWX}	t_{WCH}	Write command hold time	25		30		45		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_H	t_{WP}	Write command pulse width	25		30		50		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	60		65		110		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		50		100		ns	

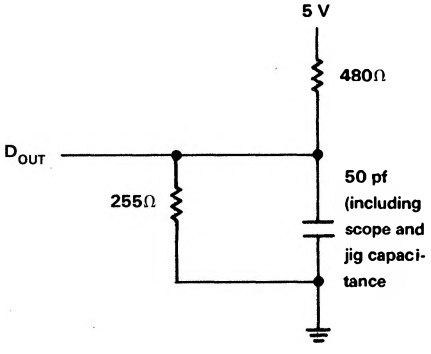
AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL		PARAMETER	MK4516-10		MK4516-12		MK4516-15		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX	MIN	MAX		
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	12
t_{CELDX}	t_{DH}	Data-in hold time	25		30		45		ns	12
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		70		85		ns	
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	WRITE command set-up time	0		0		0		ns	13
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to WRITE delay	55		65		80		ns	13
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to WRITE delay	100		120		150		ns	13
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	

AC TEST CONDITIONS

Input Levels.....0 V to 3.0 V
Transition times..... 5 ns
Input timing reference level.....1.5 V
Output timing reference levels.....0.8 V - 2.0 V
Output load.....See figure

OUTPUT LOAD



CAPACITANCE

($-55°C \leq T_C \leq 110°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

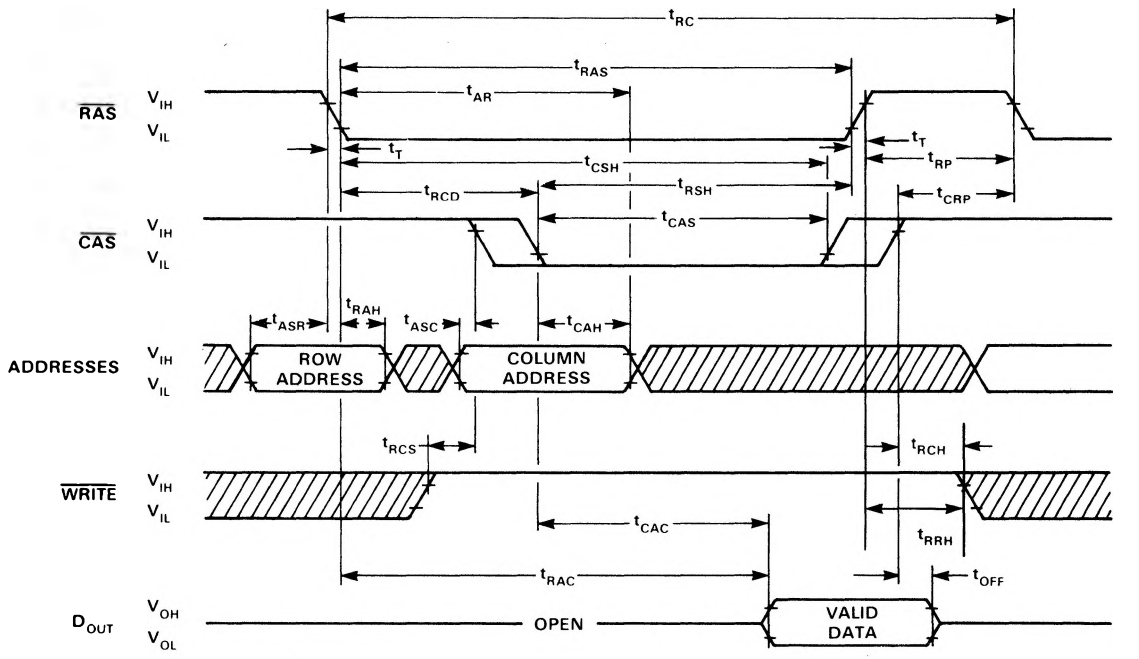
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{11}	Input (A_0 - A_5), D_{IN}	4	5	pF	15
C_{12}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	15
C_O	Output (D_{OUT})	5	7	pF	15,16

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause.
5. V_{IH} min. and V_{IL} max are reference levels for measuring timing of Input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-55°C \leq T_C \leq +110°C$) is assigned.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
10. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
13. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
14. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
15. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level. This parameter is sample tested only.
16. $\overline{CAS} = V_{IH}$ D_{OUT}.
17. Includes the dc level and all instantaneous signal excursions.
18. Power consumption decreases with increasing temperature.

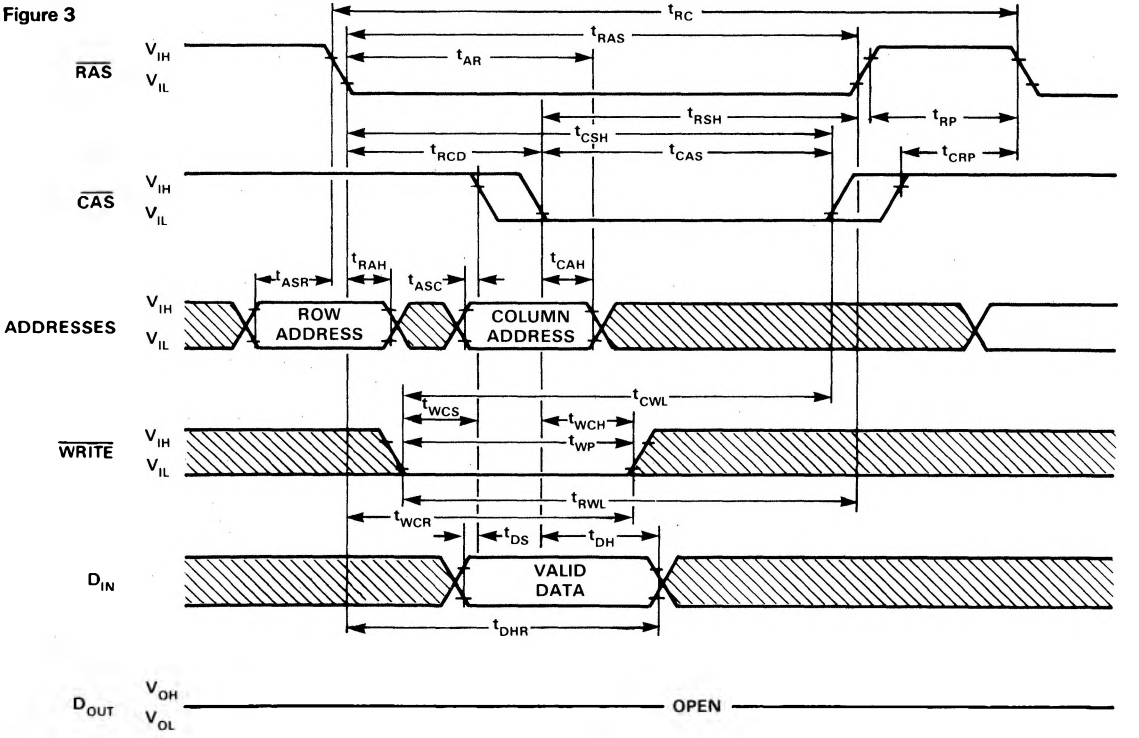
READ CYCLE

Figure 2



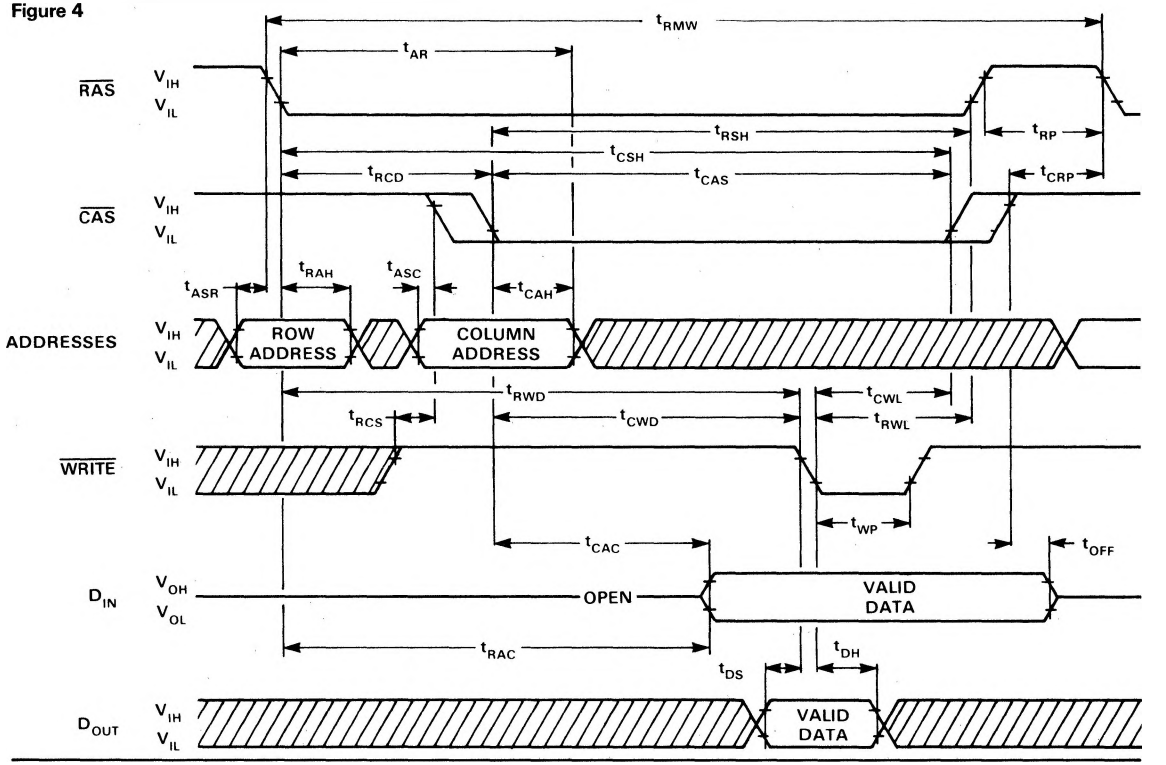
WRITE CYCLE

Figure 3



READ-WRITE/READ-MODIFY-WRITE CYCLE

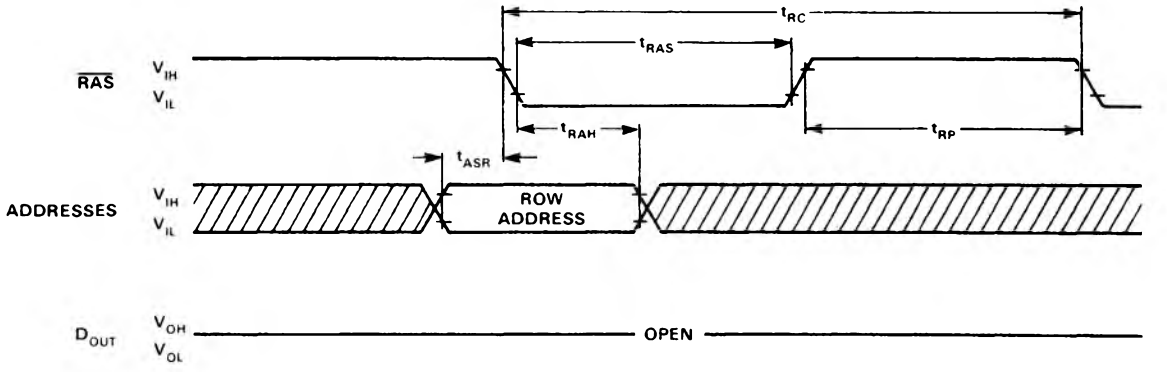
Figure 4



"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE

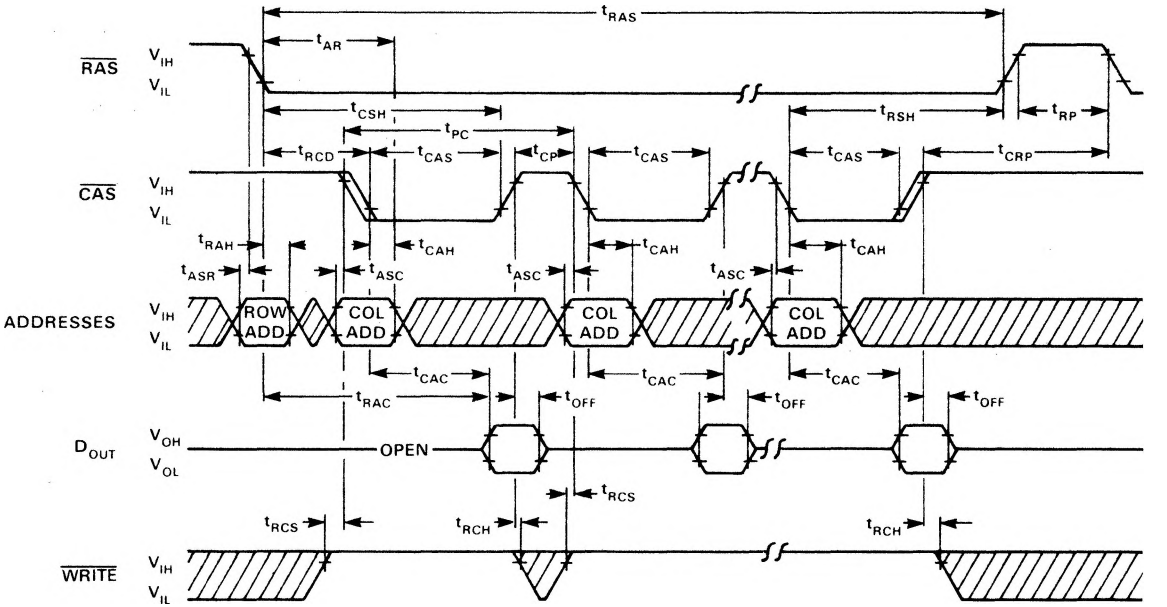
NOTE: $\overline{\text{CAS}}$ = V_{IH} $\overline{\text{WRITE}}$ = DON'T CARE

Figure 5



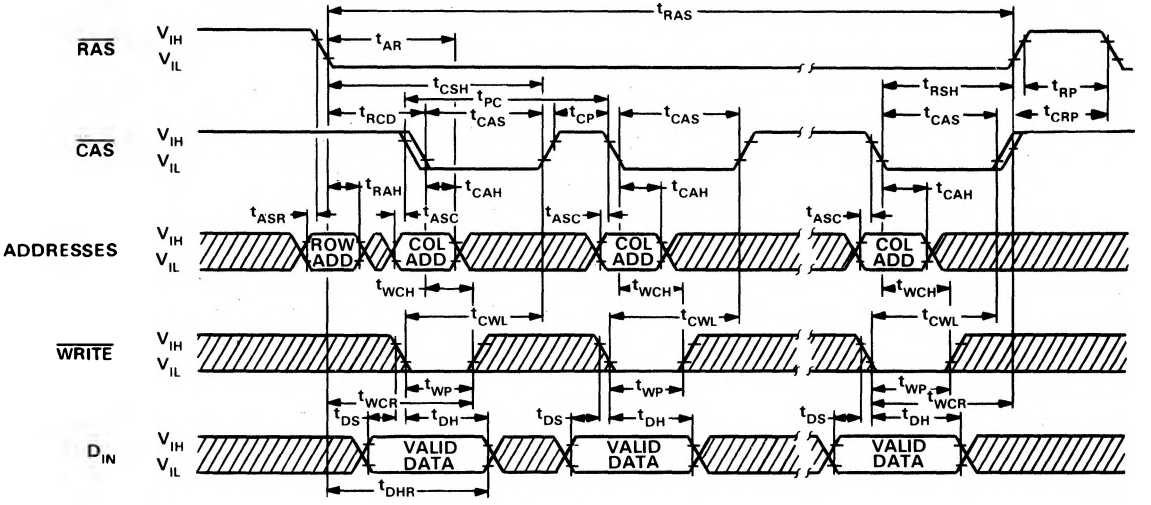
PAGE MODE READ CYCLE

Figure 6



PAGE MODE WRITE CYCLE

Figure 7



OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MKB4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be acitvated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MKB4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the accesss time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthed by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write), or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input is set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating.

Once the output data port has gone active, it wil remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Page Mode Operation

The Page Mode feature of the MKB4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first success within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MKB4516, this results in as much as a 45% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MKB4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page mode boundary need not be sequentially addressed and any combination of read-write and read-modify-write cycle are permitted within the page mode operation.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.