ADVANCE INFORMATION

MOSTEK®

68000 MICROCOMPUTER PERIPHERALS

Multi-Function Peripheral

MK68901

FEATURES

- ☐ Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
- ☐ 16 source interrupt controller
  - 8 internal sources
  - 8 external sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
      - Optional In-service status
- ☐ 8 input/output pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmable edge selection
- ☐ Single channel USART
  - Full duplex
  - Asynchronous to 62.5 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals
  - Modem control
- ☐ MK68000 BUS compatible
- ☐ 48 Pin dip

INTRODUCTION

The MK68901 MFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are:

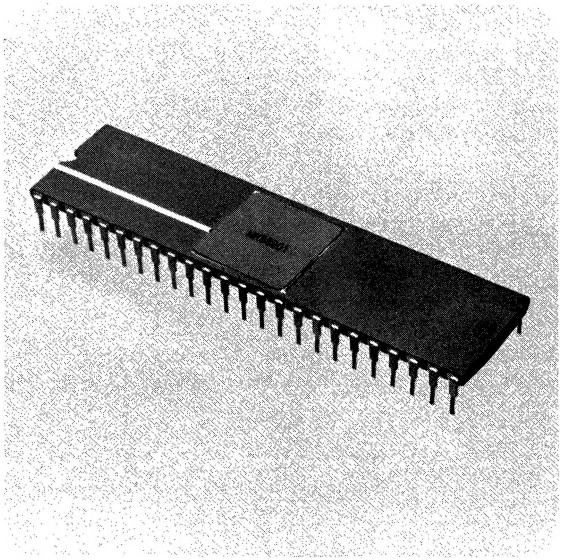
Four timers

Interrupt controller for 16 sources

Eight parallel I/O lines

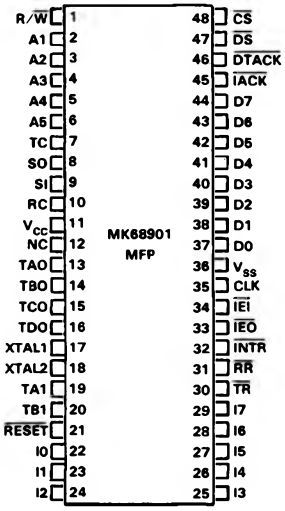
Single channel USART

MK68901
Figure 1



DEVICE PINOUT

Figure 2



The use of the MFP in a system can significantly reduce chip count, thereby reducing system cost. The MFP is completely MK68000 bus compatible, and 24 directly addressable internal registers provide the necessary control and status interface to the programmer.

The MFP is an enhancement of the MK3801 STI, a Z80 family peripheral.

PIN DESCRIPTION

Vss: Ground

Vcc: +5 volts (± 5%)

$\overline{CS}$: Chip Select (Input, Active Low). Used to activate the MK68901 MFP for accesses to the registers.

$\overline{DS}$: Data Strobe (Input, Active Low). Used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (Input, Active High for read, Active Low for write).

$\overline{DTACK}$: Data Transfer Acknowledge (Output, Active Low). Used to signal the CPU that data is ready, or that data has been accepted by the MK68901 MFP.

A1-A5: Address Inputs. Used to address one of the internal registers during a read or write operation.

D0-D7: Data Bus (Bi-Directional). Used to receive data from or transmit data to one of the internal registers during a read or write operation. Also used to pass a vector during interrupt acknowledge.

$\overline{RESET}$: Device Reset (Input, Active Low). When activated, all internal registers (except for timer, USART Data registers, and transmit status register) will be cleared. All timers will be stopped. The USART receiver and transmitter will be disabled. All interrupt channels will be disabled and all pending interrupts will be cleared. The General Purpose I/O and Interrupt lines will be placed in the tri-state input mode. All timer outputs will be forced to the low (logic "0") state.

I0-I7: General Purpose I/O and Interrupt lines. These lines may be used as I/O lines and/or interrupt inputs. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

$\overline{INTR}$: Interrupt Request (Output, Active Low, open drain). Used to communicate an interrupt request from the MK68901 to the CPU.

$\overline{IACK}$: Interrupt Acknowledge. (Input, Active Low). Used to signal the MK68901 that the CPU is a knowledging its interrupt. $\overline{CS}$ and $\overline{IACK}$ are mutually exclusive.

$\overline{IEI}$: Interrupt Enable In (Input, Active Low). Used to signal the MK68901 that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (Output, Active Low). Used to signal lower priority peripherals that neither the MK68901 nor another higher priority peripheral is requesting interrupt service.

SO: Serial Output. The output of the USART transmitter.

SI: Serial Input. The input to the USART receiver.

RC: Receiver Clock (Input). Controls the serial bit rate of the USART receiver.

TC: Transmitter Clock (Input). Controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready (Output, Active Low). DMA output for receiver.

$\overline{TR}$: Transmitter Ready (Output, Active Low). DMA output for transmitter.

TAO, TBO, TCO, TDO: Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO can be reset (logic "0") by a write to TACR, or TBCR, respectively.

XTAL1, XTAL2: Timer Clock inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with a TTL level clock. All chip accesses are independent of the timer clock.

TAI, TBI: Timer A, B inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with I4 and I3 are used for TAI and TBI, respectively. Thus, when running a timer in one of these two modes, I4 or I3 can be used for I/O only.

REGISTER MAP

Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
0	GPIP	GENERAL PURPOSE I/O
1	AER	ACTIVE EDGE REGISTER
2	DDR	DATA DIRECTION REGISTER
3	IERA	INTERRUPT ENABLE REGISTER A
4	IERB	INETRRUPT ENABLE REGISTER B
5	IPRA	INTERRUPT PENDING REGISTER A
6	IPRB	INTERRUPT PENDING REGISTER B
7	ISRA	INTERRUPT IN-SERVICE REGISTER A
8	ISRB	INTERRUPT IN-SERVICE REGISTER B
9	IMRA	INTERRUPT MASK REGISTER A
A	IMRB	INTERRUPT MASK REGISTER B
B	VR	VECTOR REGISTER
C	TACR	TIMER A CONTROL REGISTER
D	TBCR	TIMER B CONTROL REGISTER
E	TCDCR	TIMERS C AND D CONTROL REGISTERS
F	TADR	TIMER A DATA REGISTER
10	TBDR	TIMER B DATA REGISTER
11	TCDR	TIMER C DATA REGISTER
12	TDDR	TIMER D DATA REGISTER
13	SCR	SYNC CHARACTER REGISTER
14	UCR	USART CONTROL REGISTER
15	RSR	RECEIVER STATUS REGISTER
16	TSR	TRANSMITTER STATUS REGISTER
17	UDR	USART DATA REGISTER

CLK: Clock input. Used to control accessing of the MK68901 MFP.

INTERRUPT CONTROLLER

Each individual function in the MK68901 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during the interrupt acknowledge cycle is shown in Figure 4, while the vector register is shown in Figure 5.

There are 16 vector addresses generated internally by the MK68901, one for each of the 16 interrupt channels.

INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers provide control of interrupt processing for all I/O facilities of the MK68901. These registers allow the programmer to enable or disable any or all of the 16 interrupts, provide masking for any interrupts, and provide access to the pending and in-service status of the interrupts. Optional End-of-Interrupt modes are available under software control. All the interrupts are prioritized as shown in Figure 6.

INTERRUPT OPERATION

The Interrupt Enable Registers enable or disable the setting of an interrupt in the Interrupt Pending Registers. A '0' in a bit of the Interrupt Enable Registers disables the interrupt for the associated channel while a '1' enables the interrupt. Once an interrupt is enabled, the occurrence of an interrupting condition on that channel will cause the corresponding bit in the Interrupt Pending Register to be set which indicates that an interrupt is pending in the MK68901. Pending interrupts are presented to the CPU in order of priority unless they have been masked off. Masking is done by clearing the bit in the Interrupt Mask Register corresponding to the channel whose interrupt is to be masked. The channel's interrupt will remain pending until the mask bit for that channel is set, at which time the interrupt for that channel will be processed in order of priority.

When an interrupt vector is generated for a pending interrupt and passed to the CPU, the bit in the Interrupt Pending Register associated with the channel generating the interrupt will be cleared. At this time, no history of the interrupt remains in the MK68901.

In order to retain historical evidence of an interrupt being serviced by the CPU, the In-Service Register may be enabled by setting the S-bit in the Vector Register. If the In-Service Register is enabled, the bit of the In-Service Register corresponding to the interrupting channel will be set when the interrupt vector is passed to the CPU. At the same time, the Interrupt Pending bit will be cleared since the interrupt is now in service. The in-service bit can be cleared by writing a zero into it.

The daisy chaining capability (by using the $\overline{IEI}$ and $\overline{IEO}$ signals) would allow a designer to configure many MK68901 MFP's in the chain. It also allows for the freedom of putting more interrupt sources at one interrupt level. The MK68901 can handle up to eight external interrupts. The individual enabling, masking, edge selection, and vectoring capability allow the MFP to be an intelligent multiplexor for MK68000 systems.

TIMERS

There are four timers on the MK68901 MFP. Two of the timers (Timer A and Timer B) are full function timers which perform the basic delay function and can also perform event counting, pulse width measurement, and waveform generation functions. The other two timers (Timer C and Timer D) are delay timers only. One or both of these timers can be used to supply the baud rate clocks for the USART.

All timers are prescaler/counter timers with a common independent clock input (XTAL1, XTAL2), and are not required to be operated from the system clock. In addition, all timers have a time-out output function that toggles each time the timer times out.

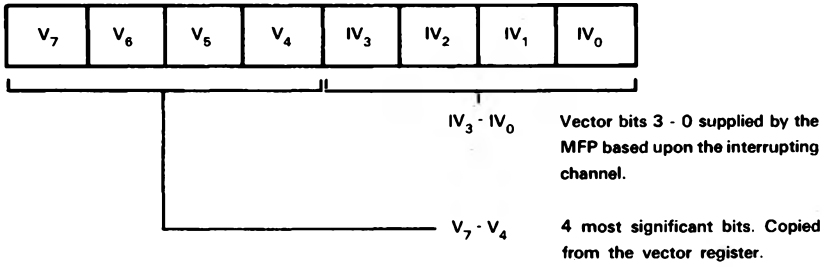
TIMER CONTROL REGISTERS

The 4 timers (A, B, C, and D) are programmed via 3 control registers and 4 timer data registers. Timers A and B are controlled by the control registers TACR and TBCR respectively (See Figure 7) and by the timer data registers TADR and TBDR. Timer C and D are controlled by the control registers TCDCR (See Figure 8) and two timer data registers TCDR and TDDR. Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write into the time constant register. Timer A and B input pins, TAI and TBI, are used for the event and pulse width modes for timers A and B.

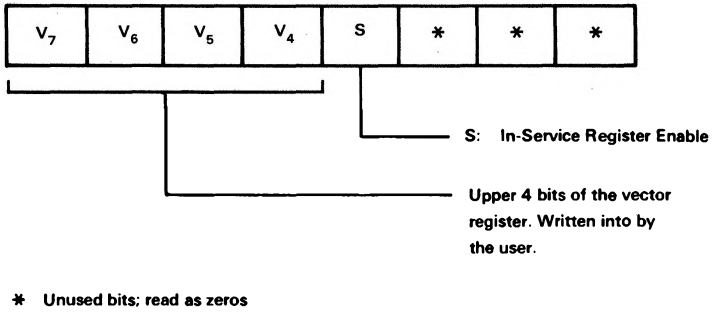
USART

Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation. Variable word length and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for

INTERRUPT VECTOR
Figure 4



VECTOR REGISTER
Figure 5



INTERRUPT PRIORITIES

Figure 6

PRIORITY	CHANNEL	DESCRIPTION
HIGHEST	1111	General Purpose Interrupt 7(I7)
	1110	General Purpose Interrupt 6(I6)
	1101	Timer A
	1100	Receive Buffer Full
	1011	Receive Error
	1010	Transmit Buffer Empty
	1001	Transmit Error
	1000	Timer B
	0111	General Purpose Interrupt 5(I5)
	0110	General Purpose Interrupt 4(I4)
	0101	Timer C
	0100	Timer D
	0011	General Purpose Interrupt 3(I3)
	0010	General Purpose Interrupt 2(I2)
	0001	General Purpose Interrupt 1(I1)
LOWEST	0000	General Purpose Interrupt 0(I0)

TIMERS A AND B CONTROL REGISTERS

Figure 7

*	*	*	TIMER A RESET	AC_3	AC_2	AC_1	AC_0	TACR
*	*	*	TIMER B RESET	BC_3	BC_2	BC_1	BC_0	TBCR

C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷4 Prescale
0	0	1	0	Delay Mode, ÷10 Prescale
0	0	1	1	Delay Mode, ÷16 Prescale
0	1	0	0	Delay Mode, ÷50 Prescale
0	1	0	1	Delay Mode, ÷64 Prescale
0	1	1	0	Delay Mode, ÷100 Prescale
0	1	1	1	Delay Mode, ÷200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷4 Prescale
1	0	1	0	Pulse Width Mode, ÷10 Prescale
1	0	1	1	Pulse Width Mode, ÷16 Prescale
1	1	0	0	Pulse Width Mode, ÷50 Prescale
1	1	0	1	Pulse Width Mode, ÷64 Prescale
1	1	1	0	Pulse Width Mode, ÷100 Prescale
1	1	1	1	Pulse Width Mode, ÷200 Prescale

* Unused bits; read as zeros.

transmission. Moreover, the MK68901 allows stripping of all Sync Words received in synchronous operation. The handshake control lines $\overline{RR}$ (Receiver Ready) and $\overline{TR}$ (Transmitter Ready)allow DMA operation. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

USART CONTROL REGISTERS

The USART is provided with 3 control/status registers and a data register. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 9. Status of both the Receiver and Transmitter sections is accessed by means of the 2 Status

TIMERS C AND D CONTROL REGISTER

Figure 8

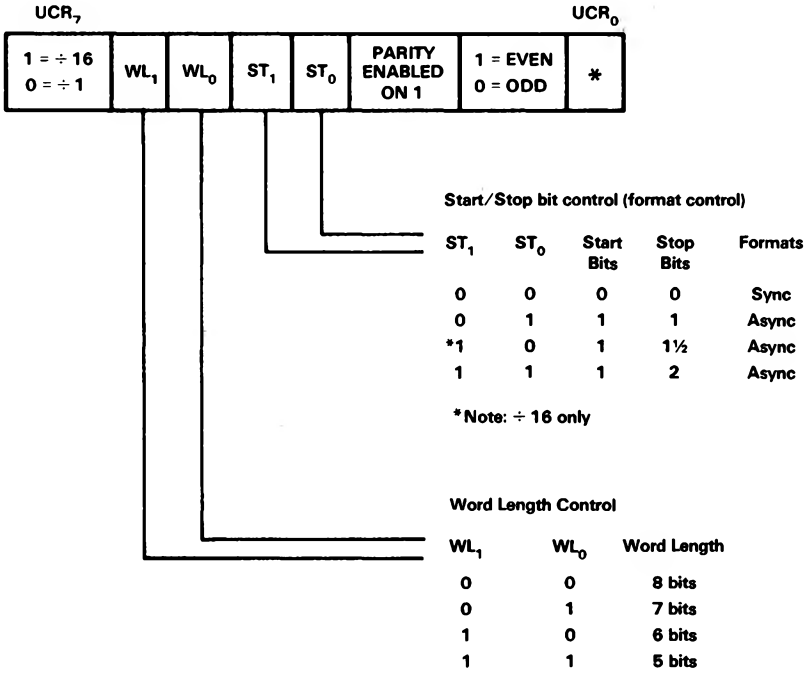
*	CC_2	CC_1	CC_0	*	DC_2	DC_1	DC_0

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷4 Prescale
0	1	0	Delay Mode, ÷10 Prescale
0	1	1	Delay Mode, ÷16 Prescale
1	0	0	Delay Mode, ÷50 Prescale
1	0	1	Delay Mode, ÷64 Prescale
1	1	0	Delay Mode, ÷100 Prescale
1	1	1	Delay Mode, ÷200 Prescale

* Unused bits; read as zeros.

USART CONTROL REGISTER (UCR) Port C

Figure 9



* Unused bits; read as zeros

RECEIVER STATUS REGISTER (RSR) Port '15'

Figure 10

RSR_7							RSR_0
BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND/SEARCH OR BREAK DETECT	MATCH/CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

TRANSMITTER STATUS REGISTER (TSR) Port '16'

TSR_7							TSR_0
BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	END OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

H	L	Serial Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop[1]

[1]Connects transmitter output to receiver input. In loopback mode, transmitter goes high when disabled. Also connects clocks when TC given priority.

USART DATA REGISTER (UDR) Port '17'

Figure 11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

GENERAL PURPOSE I/O CONTROL REGISTERS

Figure 12

ACTIVE EDGE CONTROL REGISTER (AER) Port 1

1 = RISING
0 = FALLING

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

DATA DIRECTION REGISTER (DDR) Port 2

1 = OUTPUT
0 = INPUT

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

GENERAL PURPOSE I/O DATA REGISTER (GPIP) Port 0

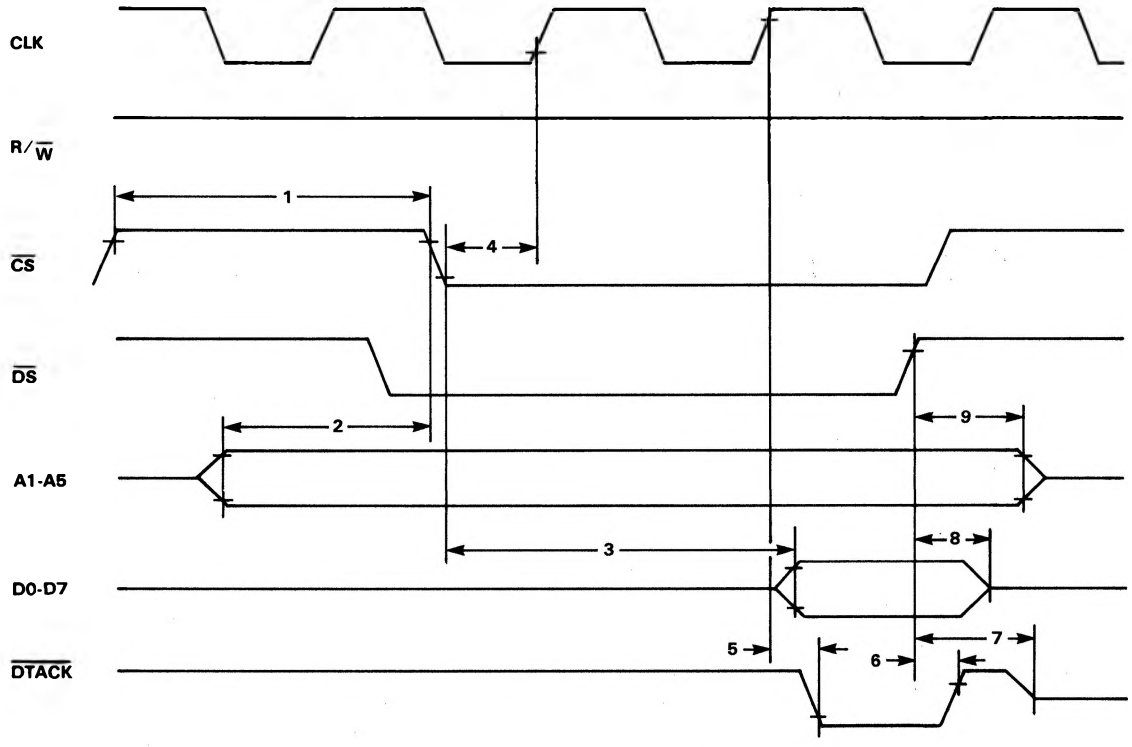
GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1 (TR)	GPIP 0 (RR)

Registers, as shown in Figure 10. Data written to the Data Register is passed to the transmitter, while reading the data register will access data received by the USART. The USART Data Register form is illustrated in Figure 11.

ERROR CONDITIONS

Error conditions in the USART are determined by monitoring the Receive Status register (Port '15') and the Transmitter Status Register (Port '16'). These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save any error conditions during data transfer, the MFP interrupt controller may be used by enabling error interrupts (Port 4), for the desired channel (Receive error or Transmit error) and by masking these bits off (Port A). Once the transfer is complete, the Interrupt Pending Register (Port 6) can be polled to determine the presence of a pending error interrupt, and therefore an error.

READ CYCLE
Figure 13



NOTES:

1. $\overline{CS}$ High time between reads
2. Address setup for READ cycle
3. Data valid from $\overline{CS}$ if $\overline{CS}$ setup to CLK met
4. $\overline{CS}$ setup to CLK
5. $\overline{DTACK}$ delay from rising edge of CLK
6. $\overline{DS}$ or $\overline{CS}$ high to $\overline{DTACK}$ high
7. $\overline{DS}$ high to $\overline{DTACK}$ high impedance
8. $\overline{DS}$ high to Data Bus high impedance
9. Address hold time for READ cycle

GENERAL PURPOSE I/O - INTERRUPT PORT

The General Purpose I/O - Interrupt Port provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

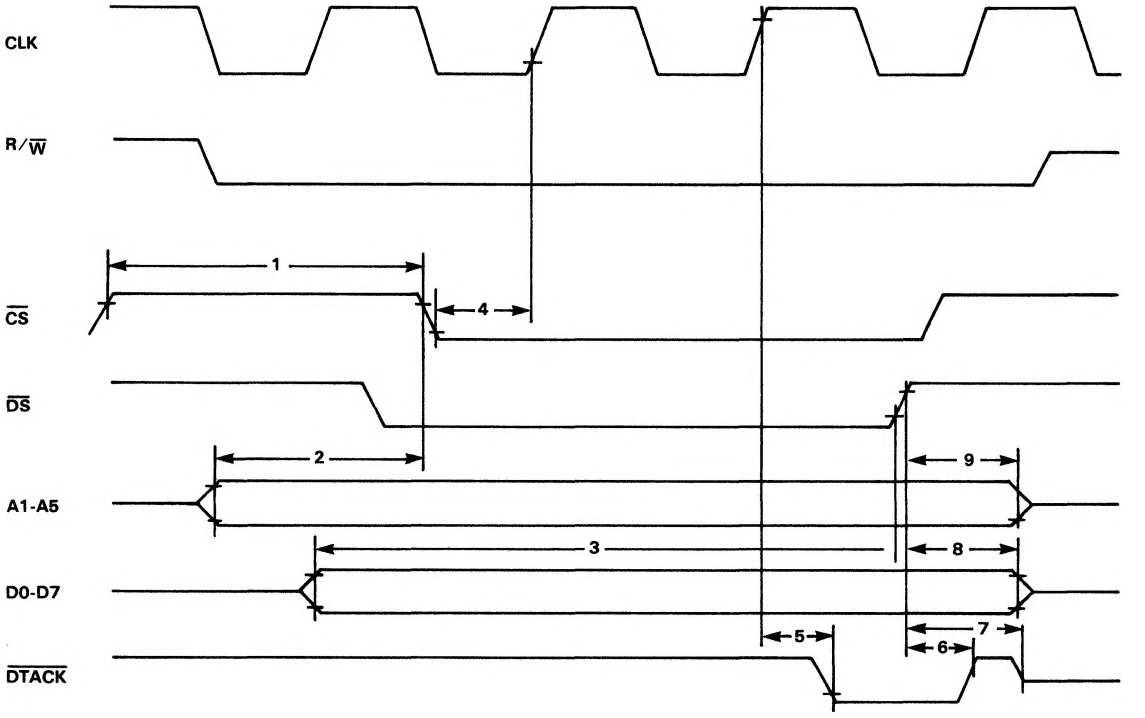
GENERAL PURPOSE I/O CONTROL REGISTERS

The General Purpose I/O and Interrupt Port has 3 associated registers. One allows the programmer to specify the Active Edge for each bit that will trigger the interrupt associated with that bit. The other register specifies the Data Direction (input and output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. The General Purpose I/O Control and Data Registers are illustrated in Figure 12.

REGISTER ACCESS

All register accesses are dependent on CLK. To read a register (See Figure 13), $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The internal read control signal is essentially the combination of $\overline{CS}$, $\overline{DS}$, and R/$\overline{W}$. Thus the read operation will begin when $\overline{CS}$ and $\overline{DS}$ go active and end when either $\overline{CS}$ or $\overline{DS}$ goes inactive. The address bus must be stable prior to the start of the operation and must remain

WRITE CYCLE
Figure 14



NOTES:
1. CS High time between writes
2. Address setup time for write cycle
3. Data setup prior to end of write cycle
4. CS setup to rising edge of CLK
5. DTACK delay from rising edge of CLK
6. DS high to DTACK high
7. DS high to DTACK high impedance
8. Data hold time
9. Address hold time

stable until the end of the operation. Unless a read operation, or interrupt acknowledge cycle, is in progress, the data bus (D0-D7) will remain in the tri-state condition.

To write a register (See Figure 14), CS and DS must be asserted and R/W must be low. The MK68901 will respond by sampling the data bus and decoding the address bus for the register selected. After the MK68901 asserts DTACK, the CPU negates DS. At this time, the MFP latches the data bus and writes the contents into the appropriate register. Also, when DS is negated, the MFP rescinds DTACK.