# **MOS Counter Time-Base Circuit**

Ion-implanted for full TTL/DTL compatibility

Internal clock operates from: External signal

External RC network External crystal

- □ Operates DC to above 1 MHz
- □ Binary-encoded for frequency selection

## DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and di-vider chain manufactured by Mostek using its depletionload, ion-implantation process and P. - channel technology. The 16-pin DIP package provides frequency division ranges from 1 to  $36 \times 10^{8}$ . The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks,

With an input frequency of 1

MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1  $\mu$ s through 100 seconds. Oneminute, ten-minute, and onehour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.



MK 5009 P

MK 5009 N

MOSTEK



1	ADDRESS INPUTS				WITHOUT RESET	RES	SET	BYPASS MODES (see page 3)							
						Reset Max.	Reset Min.	Mode 1	Mode 2	Mode 3					
ĺ					$R_{MAX} = 0$	$R_{MAX} = 1$	$R_{MAX} = 0$	$R_{MAX} = V_{GG}$	$R_{MAX} = 0$	$R_{MAX} = V_{GG}$					
	23	2²	י2	20	$R_0 = 0$	$R_{o} = 0$	$R_{o} = 1$	$R_0 = 0$	$R_0 = V_{GG}$	$R_0 = V_{GG}$					
Ī	0	0	0	0	÷ 10º	- <u>+</u> 10º	÷ 10º	÷ 10º	÷ 10º	÷ 10º					
	0	0	0	1	÷ 10'			÷ 10'	÷ 10'	÷ 10'					
	0	0	1	0	÷ 10 <sup>2</sup>	Resets	Resets	÷ 10 <sup>2</sup>	÷ 10²	÷ 10 <sup>2</sup>					
ł	0	0	1	1	÷ 103			÷ 103	÷ 10³	÷ 10³					
I	0	1	0	0	÷ 10⁴	Counters	Counters	÷ 104	÷ 10⁴	÷ 10⁴					
I	0	1	0	1	÷ 10⁵			÷ 10 <sup>2</sup>	÷ 10⁵	÷ 10²					
	0	1	1	0		to their	to their	÷ 10 <sup>3</sup>	÷ 10°	÷ 10³					
	0	1	1	1	÷ 107			÷ 104	÷ 10'	÷ 10⁴					
	1	0	0	0	÷ 10 <sup>8</sup>	Highest	Lowest	÷ 105	÷ 105	÷ 10²					
1	1	0	0	1	÷ 6 × 10'			÷ 6 × 104	÷ 6 × 104	÷ 6 × 10'					
	1	0	1	0	$\div$ 36 $ imes$ 10 <sup>8</sup>	States	States	$\div$ 36 $ imes$ 10 <sup>5</sup>	.÷ 36 × 10⁵	$\div$ 36 $ imes$ 10 <sup>2</sup>					
	1	0	- 1	1	$\div$ 6 $\times$ 10 <sup>8</sup>			$\div$ 6 $\times$ 10 <sup>5</sup>	$\div$ 6 $\times$ 10 <sup>5</sup>	$\div$ 6 $\times$ 10 <sup>2</sup>					
1			*						—	-					
ļ	1	1	1	0	÷ 2 × 10⁴			$\div 2 \times 10^{1}$	$\div$ 2 $\times$ 10 <sup>1</sup>	÷ 2 × 10'					
	1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.					

\*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs. Logic 1 = High =  $V_{ss}$ Logic 0 = Low =  $V_{oo}$ 

# **ABSOLUTE MAXIMUM RATINGS**

Voltage on Any Terminal Relative to V <sub>ss</sub> .								. + 0.3V to - 20V
Operating Temperature Range (Ambient)			 	 				. 0°C to +70°C
Storage Temperature Range (Ambient) .		•	•		•			 - 55°C to + 150°C

# **RECOMMENDED OPERATING CONDITIONS**

(0°C  $\leq$ T<sub>A</sub>  $\leq$ 70°C)

	PARAMETER	MIN	ТҮР	MAX	UNITS	NOTES
V <sub>ss</sub>	Supply Voltage	+ 4.5		+ 5.5	V	
V <sub>DD</sub>	Supply Voltage	0.0		0.0	V	
V <sub>GG</sub>	Supply Voltage	- 9.6		- 14.4	V	
f <sub>XTAL</sub>	Crystal Frequency	0.1		2.0	MHz	
f <sub>RC</sub>	RC Frequency	DC		200	kHz	
f <sub>EXT</sub>	External Frequency	DC		2.0	MHz	
t <sub>PL</sub>	Logic 0 Pulse Width, CLAMP	_				Note 5
	Ext. Input	200			nsec	
t <sub>PH</sub>	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			µsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V <sub>IL</sub>	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V <sub>GG</sub>		$V_{GG} + 1.0$	V	Note 2
	All Other Logic Inputs	100 March 100		0.8	V	
V <sub>ін</sub>	Input Voltage, Logic 1, All Logic Inputs	V <sub>ss</sub> -1.0	V <sub>ss</sub>	$V_{ss} + 0.3$	V	

# **ELECTRICAL CHARACTERISTICS**

'(V<sub>SS</sub> == +5V ±10%; V<sub>DD</sub> == 0 V; V<sub>GG</sub> == -12.0 V ±20%; 0 ° C  $\leq$  T<sub>A</sub>  $\leq$  70 °C)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I <sub>ss</sub> I <sub>GG</sub>	Supply Current, V <sub>ss</sub> Supply Current, V <sub>66</sub>		6.0 6.0	11.0 11.0	mA mA	Note 1
I <sub>IL</sub>	Input Current, Logic 0			- 1.6	mA	Note 2; $V_1 = 0.4V$
V <sub>оL</sub> V <sub>он</sub>	Output Voltage, Logic 0 Output Voltage, Logic 1	2.4		0.4	v v	$I_{OL} = 1.6mA^{*}$ $I_{OH} = -40 \mu A^{*}$
f <sub>sta</sub>	Frequency Stability w/ Volt. Change, RC Mode / Temp. Change, RC Mode Crystal Mode		± 3.0 - 0.2 		% / V % / °C	Note 3 Note 4
t <sub>e e</sub>	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Sup- ply Voltage Constant

Typical values at Vss = +5V, Vob = OV, Vgg = -12V, and T\_A = 25°C

\*VoH, VoL apply only to Time Out.

Special Products

<sup>1.</sup> Logic inputs at Vss, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to Iss when at logic 0.

<sup>2.</sup> Logic Inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext/Int Select; and Clamp.

<sup>3.</sup> Frequency variations due to power supply changes only.

<sup>4.</sup> Crystal mode stability is dependent upon crystal.

<sup>5.</sup> Minimum logic 0 time at clamp input is 50% of oscillator period.

# **DESCRIPTION OF OPERATION**

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The  $\div$  10<sup>1</sup> counter output is used to generate an internal clock signal for the 10<sup>2</sup> through  $36 \times 10^8$  counter stages, which are fully synchronous with each other.

#### **OSCILLATOR CONTROLS**

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide<u>one</u>-shot or accurate start-up operations. When Clamp goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the Clamp (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance ( $C_L$ ) specified for the selected crystal. It is recommended that  $C1 = C2 = 2 C_L$ .

#### **RESET/BYPASS CONTROLS**

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10  $\mu$ s or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage,  $V_{GG}$ , allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

# EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

# **OSCILLATOR OUTPUT**

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.



## **APPLICATION — 10 MHz Frequency Counter**

The circuit shown below is a frequency counter capable of counting input rates up to 10 MHz, selected in four ranges. The MK 5009 P provides the time base intervals while the Mostek MK 5002 P counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009 P, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, four 7475's, and four BCD-to-seven-segment decoders.



Special Products