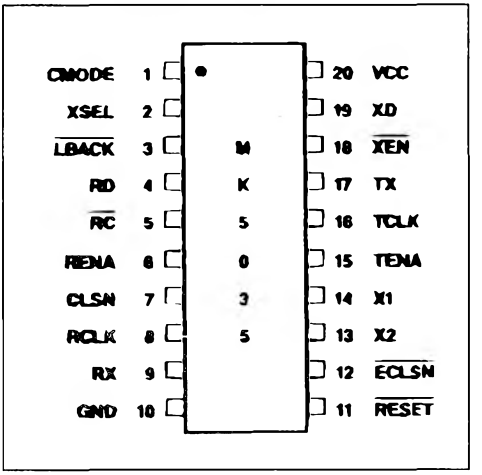
SGS-THOMSON MICROELECTRONICS

MK5035N

StarLAN ENCODER DECODER

- CONFORMS WITH STARLAN SPECIFICATION
- SUPPORTS MULTI-POINT EXTENSION
- AUTO COMPENSATION FOR LINE REVERSAL
- COMPATIBLE WITH MK5032 VLANCE AND INTEL 82586/82588
- CLOSE PIN COMPATIBILITY WITH SEEQ8023
- DATA RATES TO 2.66Mbps SUPPORTED
- MANCHESTER DATA ENCODING/DECODING
- COLLISION DETECTION CIRCUITRY WITH THE FOLLOWING FEATURES :
  - detects missing mid-bit transitions
  - transitions too close together
  - transitions too far apart
  - external collision input pin
  - carrier dropout
  - watchdog timer
  - AT&T release 1 collision presence signal
  - echo timeout
- RECEIVE END-OF-FRAME DETECTION
  - input protection at end-of-frame
- LOOPBACK CAPABILITY
- RECEIVE CARRIER AUTOMATICALLY CONVERTED TO A LEVEL SIGNAL
- ECHO TIMER TO SIGNAL ERROR IF TRANSMITTED FRAME IS NOT RECEIVED
- HEARTBEAT GENERATION
- IN 82586 MODE, INSENSITIVE TO EXTRA BITS AHEAD OF PREAMBLE
- DIGITAL PHASE-LOCKED LOOP
- ON CHIP CRYSTAL OSCILLATOR, 8X OR 6X OPERATION
- CMOS TECHNOLOGY
- 20-PIN DIP
- SINGLE 5-VOLT SUPPLY
- ALL INPUTS AND OUTPUTS TTL COMPATIBLE*

Figure 1 : MK5035 Pin Assignment.



GENERAL DESCRIPTION

The MK5035 is a Manchester Encoder/Decoder chip incorporating several features that make it an ideal StarLAN station chip. The MK5035 performs three functions. It encodes data from a controller chip into Manchester data. It decodes Manchester data from the line transceiver and produces NRZ data and clock for the controller chip. It also detects collisions and signals the controller chip that a collision has occurred.

The MK5035 has several enhancements for StarLAN and Multi-Point extension (MPE) StarLAN. These include auto compensation for wiring reversal, echo timer, external collision detect, watchdog timer, and heartbeat, among others.

* Crystal inputs have CMOS thresholds.

PIN DESCRIPTION

CONTROLLER INTERFACE

RX	Output	RX is the serial receive data after decoding.
RENA	Output	This signal indicates that data is available to the controller on the RX output.
RCLK	Output	RCLK is the receive data clock recovered from the incoming data RD.
TX	Input	TX is the serial data to be transmitted. It is clocked into the chip by TCLK.
TENA	Input	This signal indicates that data is valid on the TX input. It goes active with the first bit of transmission.
TCLK	Output	TCLK is the transmit data clock. All transmit interface signals are synchronized to this clock.
CLSN	Output	This signal is asserted when a manchester violation is detected on the RD line or when the external collision input (ECLSN) goes active.

TRANSCEIVER INTERFACE

XD	Output	Encoded transmit data output.
$\overline{XEN}$	Output	Transmit output enable. This signal goes low to indicate XD active. It goes high at the end of transmission.
RD	Input	Encoded receive data input.
$\overline{RC}$	Input	Receive carrier input. Receive carrier can be either a pulse stream or an active low signal to indicate carrier active. The chip contains internal squelch circuitry, as shown in figure 3, to convert a pulse signal to a level signal.
$\overline{ECLSN}$	Input	External collision input. When this pin is held low for at least 20nS, an external collision is signaled.

OTHER PINS

CMODE	Input	This input allows the part to be used with either Mostek or Intel controllers :

CMODE = 0, 82586/82588 (see note)

Transmit data (TX) is sampled on the rising edge of TCLK. Receive data (RX) transitions on the rising edge of RCLK.

TENA - active low

RENA - active low - goes active when phase lock loop is locked.

CLSN - active low

CMODE = 1, SGS-THOMSON VLANCE MK5032

Transmit data (TX) is sampled on the falling edge of TCLK. Receive data (RX) transitions on the falling edge of RCLK.

TENA - active high

RENA - active high - goes active when phase lock loop is locked.

CLSN - active high

$\overline{LBACK}$	Input	When this input is low the part will be put into internal loopback. The transmit data will be internally looped back as receive data. See figure 2. The outputs XD and $\overline{XEN}$ will be held inactive during loopback.
$\overline{RESET}$	Input	When this pin is low the chip is in reset mode. All interface signals will be inhibited except TCLK. $\overline{RESET}$ should remain active for three TCLK periods.
XSEL	Input	This input selects the clock divider. If XSEL = 0, it is 8X. If XSEL = 1, it is 6X.
X1, X2	Inputs	Crystal oscillator inputs. A crystal can be connected between these inputs, or a CMOS level square wave can be connected to X1 while X2 is left unconnected.
VCC	Input	+ 5V ± 5%
GND		

Note : Compatible with controller chips based on preliminary controller data sheets.

Figure 2 : StarLAN Encoder Decoder. MK5035.

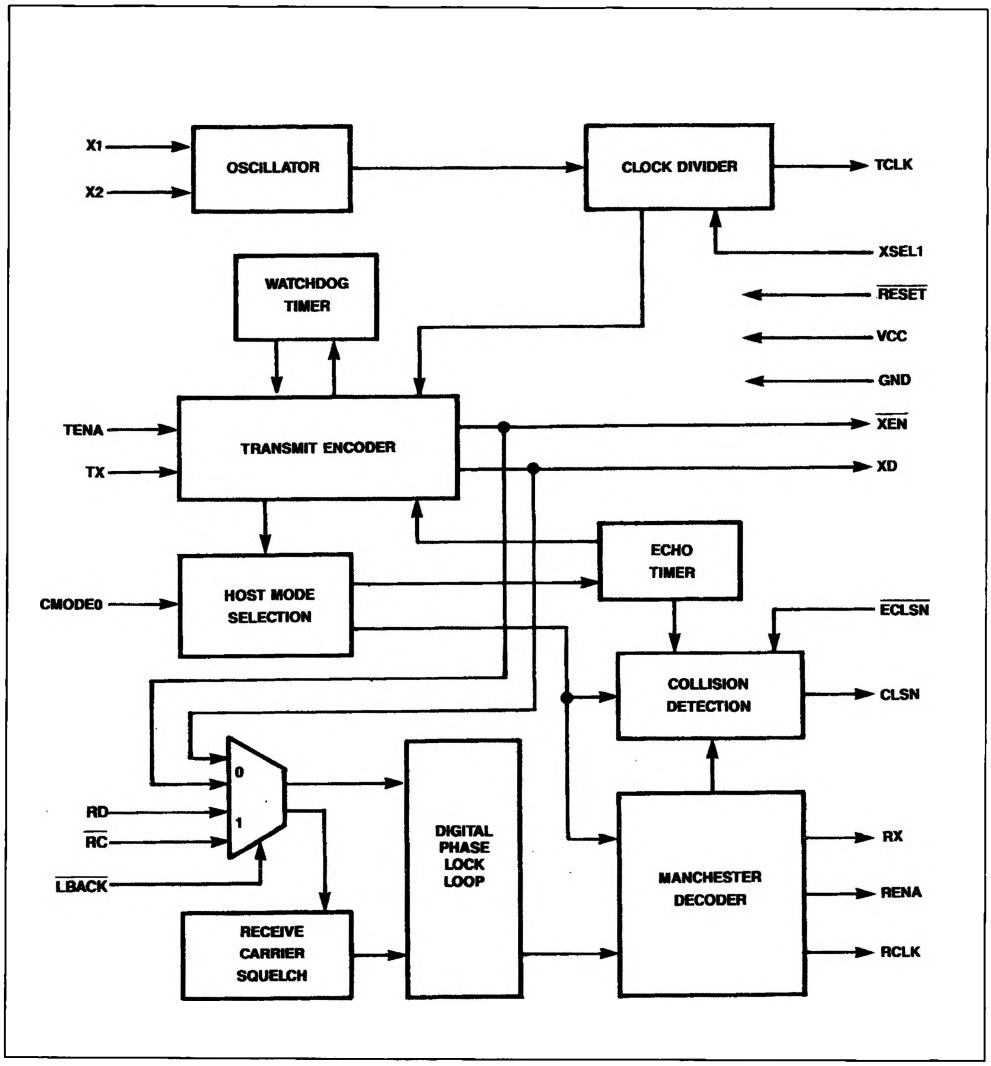
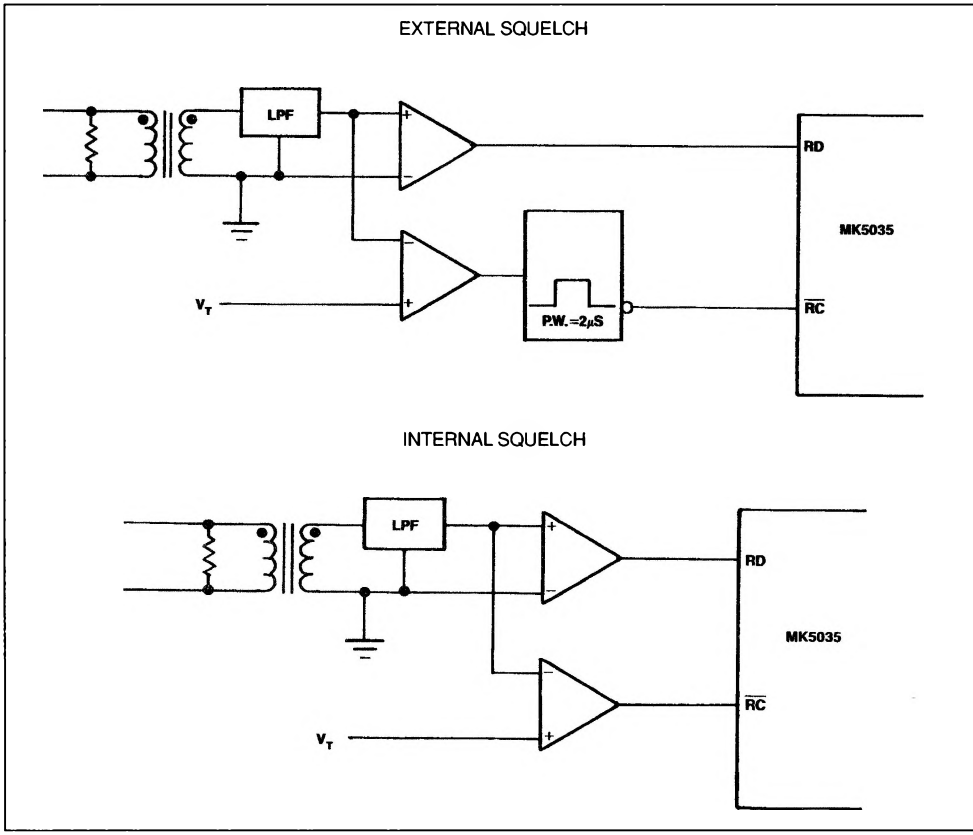


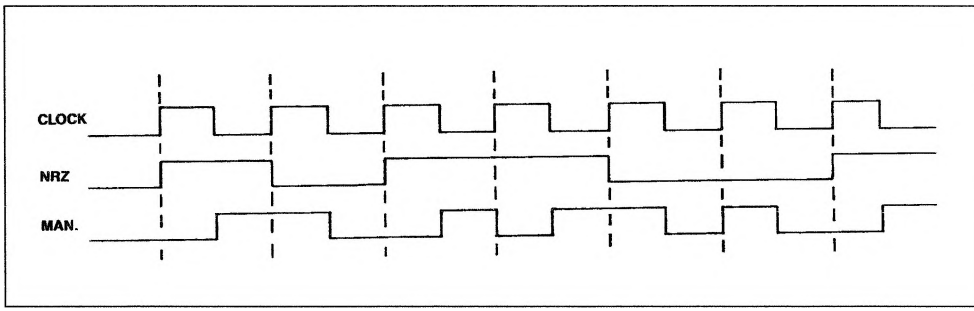
Figure 3 : Internal Versus External Time Squelch.



CIRCUIT DESCRIPTION

TRANSMITTER

The transmitter encodes NRZ data from the controller chip into the Manchester data. The diagram below shows the two encoding schemes.



Data encoding and transmission begin when the controller chip brings TENA active. The start of data encoding is delayed by two bits when in 82586/82588 mode. T_X is sampled using TCLK as the clock. The encoded data is output on XD. XEN goes low with the first bit of data output on XD. The transmit delay, delay from TENA active to XEN active, is less than 1.5 TCLKs. The controller chip signals end of data by bringing TENA inactive.

XD will be held high for an additional 1.5 TCLKs if the last data bit is a one, and for 2 TCLKs if the last data bit is a zero. During this time XEN is held active.

RECEIVER

The receiver consists of four major sections.

1) Receive carrier squelch

2) Internal loopback

3) Digital phase locked loop

4) Manchester decoder

The receiver takes Manchester data in on RD, when receive carrier (RC) is active, and decodes the data into NRZ data and also produces clock (RCLK) from the data. The NRZ data is output to the controller on RX.

RECEIVE CARRIER SQUELCH

The Receive carrier pin has internal squelch logic that allows the signal to be either a level signal or a pulse train. Receive carrier is active low. The receive carrier must be present for 3 clock samples to be considered a valid carrier. Once the carrier is considered valid then it must be active for only one clock sample time every two bit times to remain valid. (see figure 3).

Automatic Compensation For Wiring Reversal

When installing twisted pair telephone wiring, it is often difficult and expensive to maintain proper polarity on the wire pairs. The MK5035 will automatically compensate for this reversal. Any frame that is received with inverse polarity will be detected and decoded with the correct polarity.

LOOPBACK

When loopback is enabled ($\overline{\text{LBACK}}$ low), RD and RC are ignored. Transmit data is internally looped back as receive data. The transmitter outputs XD and XEN are disabled during loopback.

DIGITAL PHASE LOCKED LOOP (DPLL)

The digital phase locked loop is implemented with a counter that clears on each transition of the receive data. The phase locked loop will declare "lock" after receiving data that has two "long transitions". A long transition occurs when the receive data does not change for at least 4/6 (5/8 in 8X mode) of a bit time.

MANCHESTER DECODER

The receive data (after inversion if needed) is fed into the decoder along with the recovered 2X clock from the DPLL. The decoder changes the receive data to NRZ data. The NRZ data is output on TX. RENA signals the controller chip that data is available. (see mode pin descriptions). RCLK is a 1X clock output that is synchronous with the data on RX.

PROTECTION TIME

After the end of a received frame the receiver is disabled for 20 bit times. This protection time guarantees immunity to spikes caused by transformer coupling after the end of frame.

COLLISION

CLSN is an output to the controller chip that indicates a possible problem with the data. There are several sources of collision.

1) Transitions too close together
   Collision is signaled if the receive data stream transitions a second time in less than 2/6 (3/8 in 8X mode) bit times.

2) Transitions too far apart
   Collision is signaled if the receive data stream does not transition again within 9/6 (10/8 in 8X mode) bit times.

3) Manchester violation
   If the data violates Manchester coding rules, then collision is signaled.
   A Manchester violation is a missing mid-bit transition.

4) Watchdog timer
   If the watchdog timer expires, then collision will be signaled.

5) Echo timer
If the echo timer expires without receive carrier going active, then collision will be signaled.

6) External collision
If the external collision pin ($\overline{\text{ECLSN}}$) goes low for at least 20ns, then collision will be signaled.

7) Receive carrier lost during transmission
If the MK5035 is transmitting and the receive carrier goes active and then inactive before it is through transmitting, then collision is signaled.

8) Heartbeat

Collision, as a result of heartbeat, will be signaled 8 TCLKs after TENA goes away, and collision will remain active for at least 8 TCLKs.

Once CLSN is activated it remains active until both TENA and RENA go inactive. The exception to this is heartbeat. If heartbeat signals collision, then collision is guaranteed to remain for 8 TCLKs.

WATCHDOG TIMER

The watchdog timer ensures that the MK5035 will not transmit for more than 101K bit times. The timer is started when TXEN goes active. The timer resets when TXEN goes inactive. If TXEN remains active for more than 101K bit times, then the timer will time-out causing collision to be asserted and $\overline{\text{XEN}}$ to go inactive. If loopback is enabled, watchdog timeout will occur after 325 bit times. This particular timer value allow StarLAN HUBs to activate their own jabber functions, thereby alerting net management.

ECHO TIMER

When the echo timer is enabled the MK5035 expects the data that it is transmitting to be received on $\overline{\text{RC}}$/RD within 510 bit times. The echo timer is activated when TXEN goes active. If 510 bit times elapse before RENA goes active, then the timer will time out causing collision to be activated.

Oscillator

The MK5035 will accept two forms of clock input : a CMOS input or a crystal. If pin X2 is left unconnected, a 6.0/8.0MHz ± 0.01% CMOS clock may be applied to pin X1. Alternately, a crystal circuit may be connected between X1 and X2 to form the basis of an oscillator. Typically, a 6.0/8.0 ± 0.005% parallel resonant crystal is needed to insure the ± 0.01% frequency accuracy required for StarLAN. Refer to figure 4. A fundamental mode, parallel resonance type crystal should be used with the manufacturer's suggested load capacitance.

Reset Input

The reset pin is an active low Schmidt trigger input. A simple RC network may be used to insure correct operation upon power-up. Refer to fig. 5.

Figure 4 : Oscillator Operation.

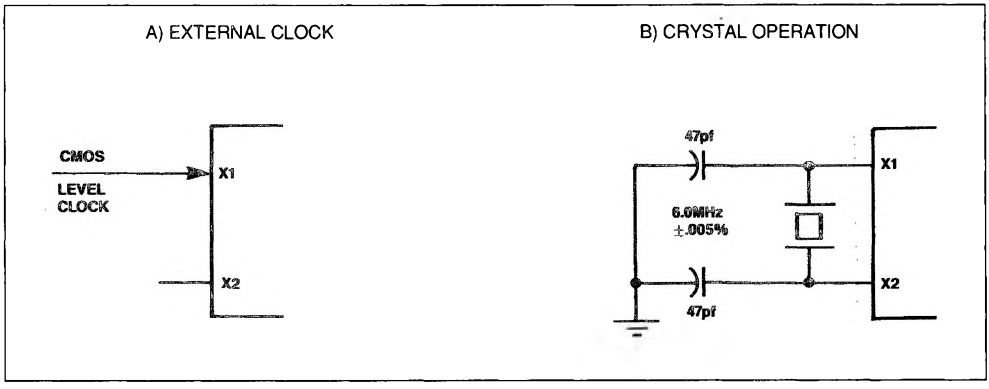
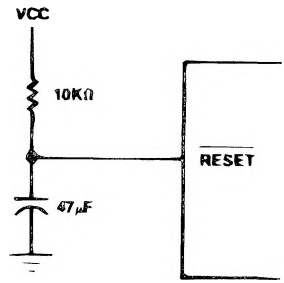


Figure 5 : Typical RC Connection for Power-On Reset.



ELECTRICAL SPECIFICATIONS

This chapter provides tabular presentations for Absolute Maximum Ratings, DC Characteristics, Capacitance and AC Timing Specifications. In addition, illustrations are provided for an Output Load Diagram (figure 9) and Station Timing Diagrams.

ABSOLUTE MAXIMUM RATINGS

Symbol	Paramter	Value	Unit
T_A	Temperature Under Bias	−25 to +100	°C
T_{stg}	Storage Temperature	−65 to +150	°C
V_I	Voltage on any Pin with Respect to Ground	−0.5 to V_{CC} +0.5	V
P_D	Power Dissipation (no load)	50	mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5% unless otherwise specified)

Symbol	Test conditions	Min.	Max.	Units
V_{IL}		− 0.5	+ 0.8	V
V_{IH}	Except X1	+ 2.0	V_{CC} + 0.5	V
V_{IH}	X1	+ 3.5	V_{CC} + 0.5	V
V_{OL}	@ I_{OL} = 3.2mA, except X2		+ 0.5	V
V_{OH}	@ I_{OH} = − 0.4mA, except X2	+ 2.4		V
V_{OH}	@ I_{OH} = − 40μA, except X2	+ 3.2		V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}		± 10	μA
I_{CC}			8	mA

CAPACITANCE : F = 1MHz

Symbol	Conditions	Min.	Max.	Units
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

(T_A = 0°C to 70°C, V_{CC} = + 5V ± 5% unless otherwise specified, V_{TH} = 2.0V, V_{TL} = 0.8V)

#	Signal	Symbol	Parameter	Min. ns	Typ. ns	Max. ns
1	X1	T_{X1T}	X1 period	62		
2	X1	T_{X1L}	X1 low time	24		
3	X1	T_{X1H}	X1 high time	24		
4	X1	T_{X1R}	Rise time of X1	0		8
5	X1	T_{X1F}	Fall time of X1	0		8
6	$\overline{XEN}$	$T_{\overline{XEN}}$	$\overline{XEN}$ delay from X1		40	65
7	XD	T_{XD}	XD delay from X1		40	65
8	XD	J_{XD}	Transmit jitter $\lvert T_{XD}\uparrow - T_{XD}\downarrow \rvert \div 2$		4	6
9	TCLK	T_{CLK}	TCLK delay from X1			70
10	TX	T_{TXST1}	TX setup to falling edge of TCLK, CMODE = 1	90		
11	TX	T_{TXHT1}	TX hold from falling edge of TCLK, CMODE = 1	15		
12	TX	T_{TXS}	TX setup to X1	15		
13	TX	T_{TXH}	TX hold from X1	15		
14	TENA	T_{TNAST1}	TENA setup to falling edge of TCLK, CMODE = 1	90		
15	TENA	T_{TNAST1}	TENA hold from falling edge of TCLK, CMODE = 1	15		
16	TENA	T_{TENAS}	TENA setup to X1	15		
17	TENA	T_{TENAH}	TENA hold from X1	15		
18	TX	T_{TXSTO}	TX setup to rising edge of TCLK, CMODE = 0	90		
19	TX	T_{TXSTO}	TX hold to rising edge of TCLK, CMODE = 0	15		
20	TX	T_{TXS}	TX setup to X1, CMODE = 0	15		
21	TX	T_{TXH}	TX hold from X1, CMODE = 1	15		
22	TENA	T_{TNASTO}	TENA setup to positive edge of TCLK, CMODE = 0	90		
23	TENA	T_{TNAHTO}	TENA hold to positive edge of TCLK, CMODE = 0	15		
24	TENA	T_{TNAS}	TENA setup to X1, CMODE = 0	15		
25	TENA	T_{TNAH}	TENA hold from X1, cmode = 0	15		
26	CLSN	T_{CLSN}	CLSN delay from X1			70
27	$\overline{ECLSN}$	$T_{\overline{ECLSN}}$	Minimum detected pulse width		5	20
28	$\overline{RC}$	$T_{\overline{RCS}}$	$\overline{RC}$ setup to X1	15		
29	$\overline{RC}$	$T_{\overline{RCH}}$	$\overline{RC}$ hold from X1	15		

AC TIMING SPECIFICATIONS (continued)

#	Signal	Symbol	Parameter	Min. ns	Typ. ns	Max. ns
30	RD	T_{RCH}	RD setup to X1	15		
31	RD	T_{RDS}	RD hold from X1	15		
32	RD	J_{RD6}	RD Incoming Jitter Tolerance, 6X mode, X1 = 6MHz, $T_{X1T} - \lvert T_{RDS} \uparrow - T_{RDS} \downarrow \rvert$		165	161
33	RD	J_{RD8}	RD Incoming Jitter Tolerance, 8X mode, X1 = 8MHz, $T_{X1T} - \lvert T_{RDS} \uparrow - T_{RDS} \downarrow \rvert$		123	119
34	RCLK	T_{RCLK}	RCLK delay from X1, CMODE = 1		40	65
35	TX	T_{RXRCK1}	RX delay from falling RCLK, CMODE = 1	– 30		30
36	RX	T_{RX}	RX delay from X1, CMODE =1		40	65
37	RENA	$T_{RNARCK1}$	RENA delay from falling RCLK, CMODE =1	– 30		30
38	RENA	T_{RENA}	RENA delay from X1, CMODE =1		45	65
39	CLSN	$T_{CSNRCK1}$	CLSN delay from falling edge RCLK, CMODE = 1	– 30		30
40	CLSN	T_{CLSN}	CLSN delay from X1, CMODE = 1			70
41	RCLK	T_{RCLK0}	RCLK delay from X1, CMODE = 0		40	65
42	RCLK	P_{RCLK}	RCLK pulse width, CMODE = 0	T_{X1T}– 20		T_{X1T}+20
43	RCLK	T_{RXCLK}	RCLK delay from RX stable, CMODE = 0	T_{X1T}– 20		
44	RX	T_{CLKRX}	RX hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}$–20		
45	RCLK	T_{RNACLK}	RCLK delay from RENA stable, CMODE = 0	T_{X1T}– 20		
46	RENA	T_{CLKRNA}	RENA hold from falling edge of RCLK, CMODE = 0	$2*T_{X1T}$–20		
47	RCLK	T_{CSNCLK}	Rising RCLK delay from CLSN stable, CMODE = 0	$2*T_{X1T}$–20		
48	CLSN	T_{CLKCSN}	CLSN delay from rising edge of RCLK, CMODE = 0	T_{X1T}–20		

Figure 6 : External X1 Timing Diagram.

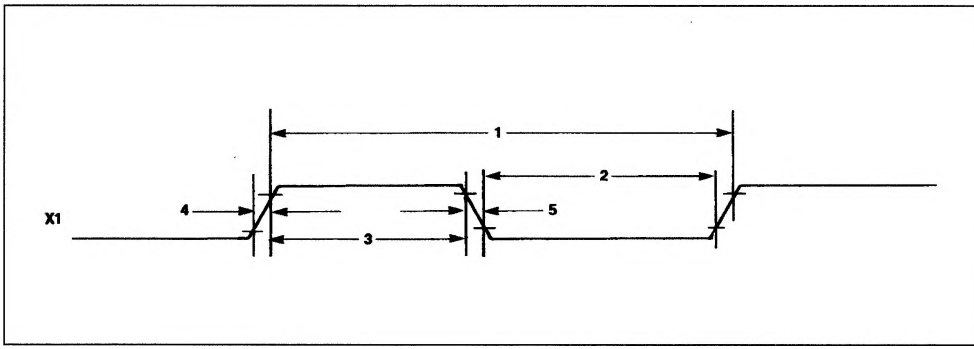


Figure 7 : Transmit Timing Diagram.

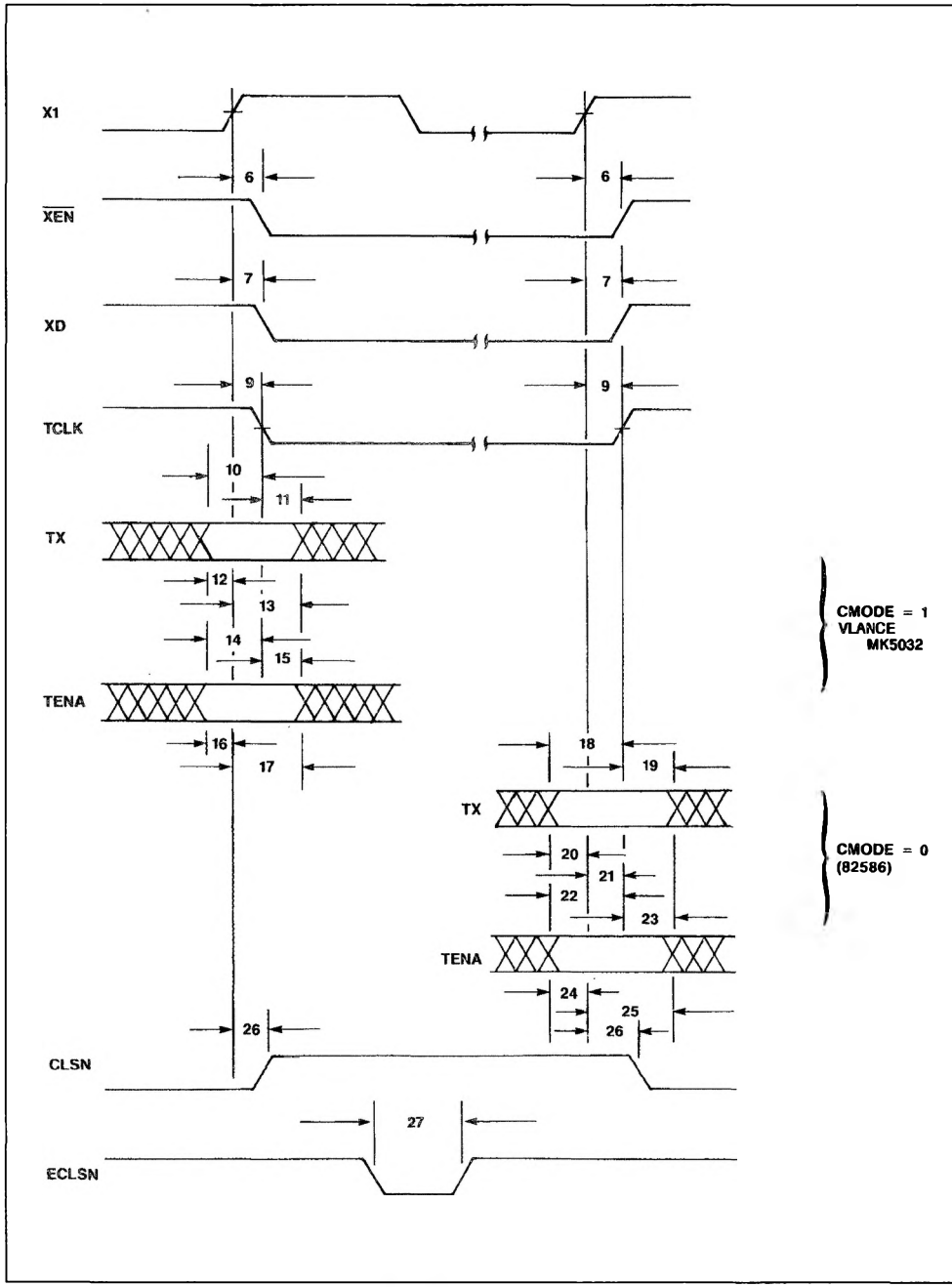


Figure 8 : Receiver Timing Diagram.

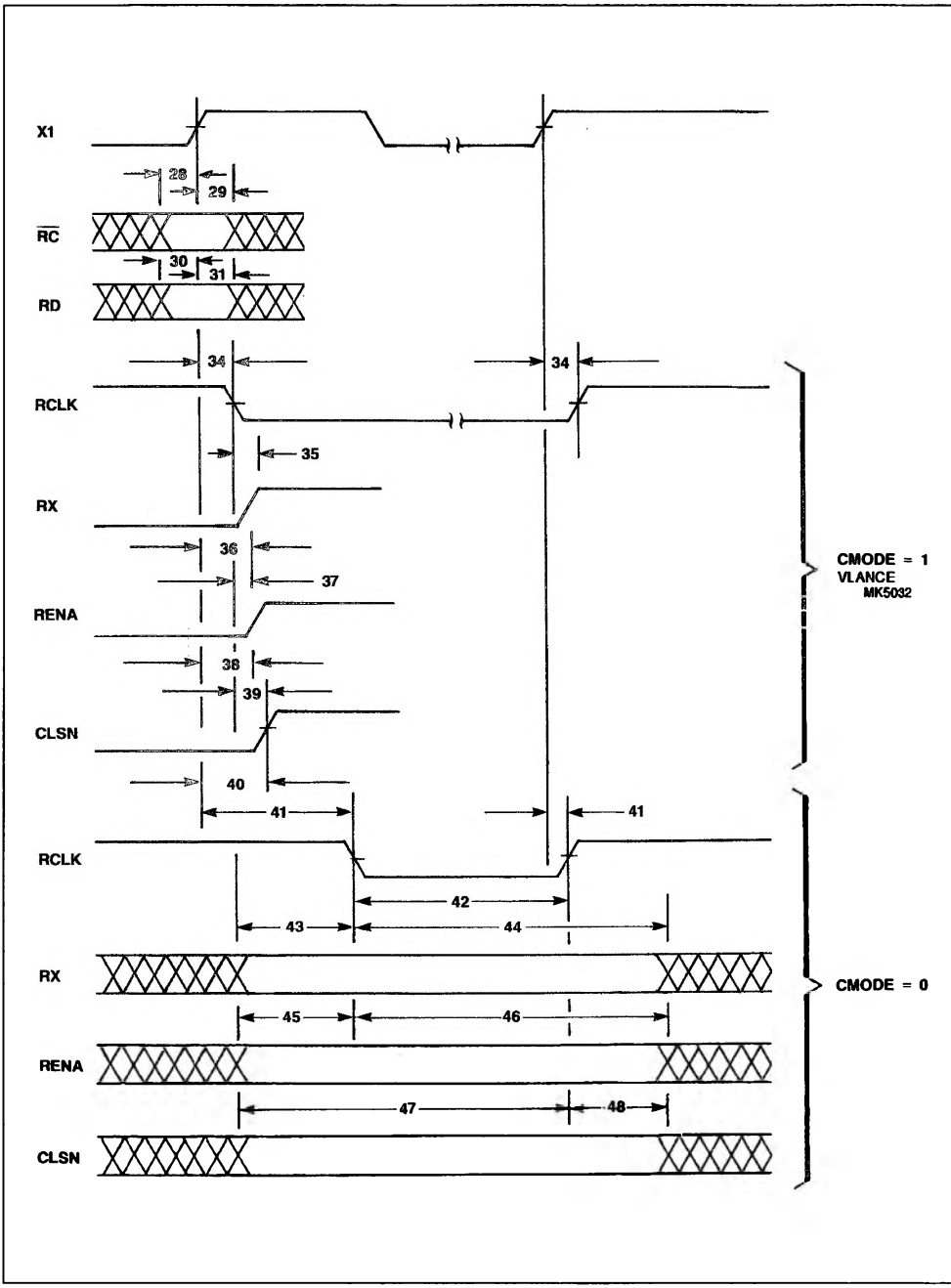
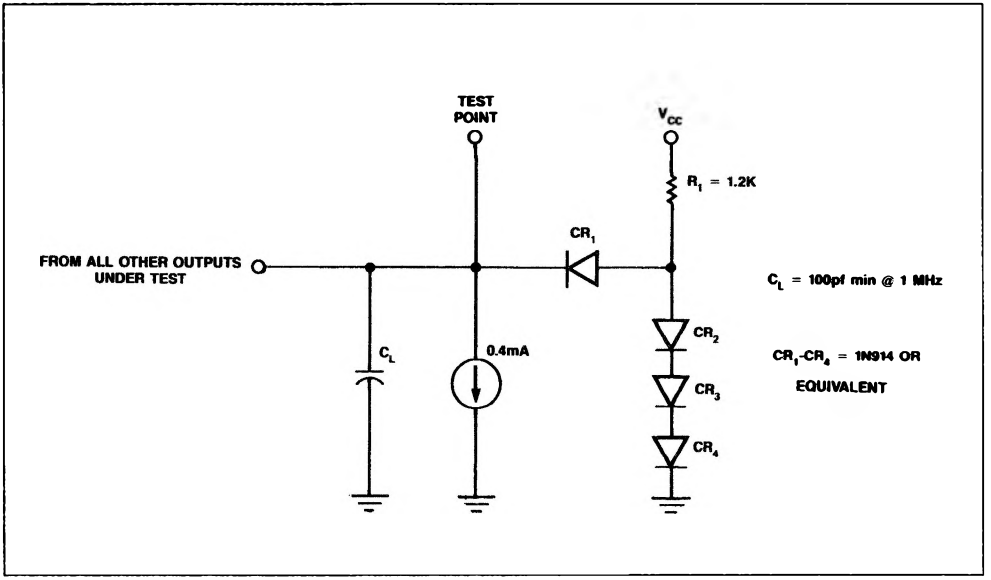
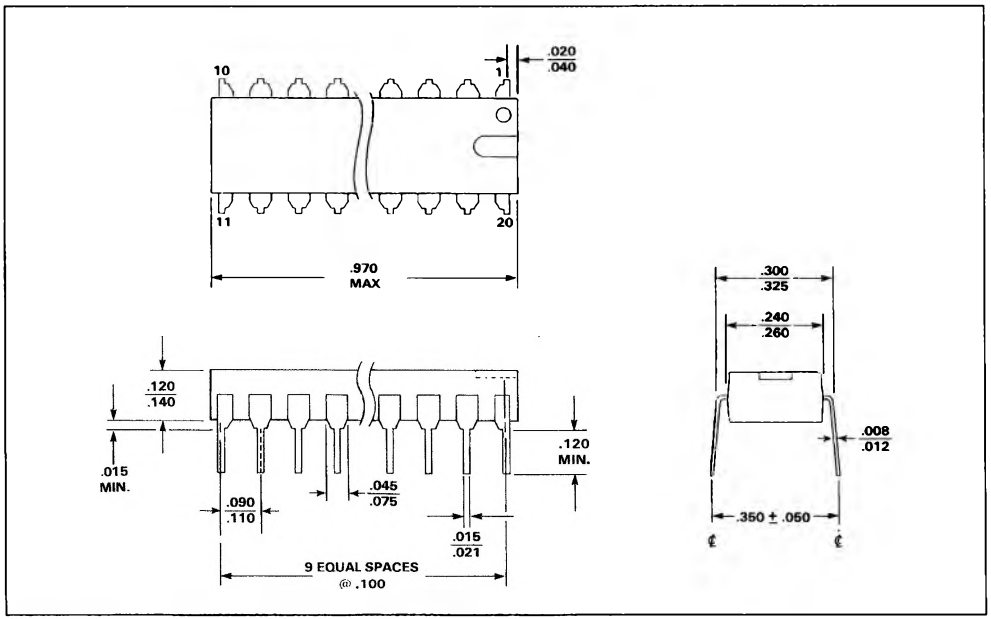


Figure 9 : Output Load Diagram.



PACKAGE DESCRIPTION

20 Pin Plastic - MK5035N



Note : Overall length includes .010 flash on either end of package.