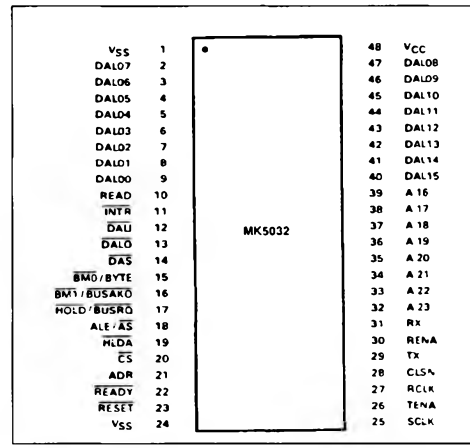
SGS-THOMSON MICROELECTRONICS

MK5032

VARIABLE BIT-RATE (1 – 10MHz) IEEE 802.3 CONTROLLER

- SUPPORTS LAN STANDARDS : IEEE 802.3, ETHERNET, CHEAPERNET, AND STARLAN
- SUPPORTS DATA RATES FROM 1 TO 10Mbps
- SUPPORTS SYSTEM CLOCKS FROM 1 TO 10MHz
- ON-CHIP DMA WITH BUFFER MANAGEMENT USING CIRCULAR QUEUES
- COMPLETE CSMA/CD DATA LINK CONTROLLER (MAC)
- PREAMBLE INSERTION AND CHECKING
- CRC INSERTION AND STRIPPING
- GENERAL PURPOSE BUS INTERFACE COMPATIBLE WITH 8086 AND 68000 BUSES
- CABLE FAULT DETECTION
- 48 PIN DIP. + 5V ONLY. ALL INPUTS/OUTPUTS TTL COMPATIBLE
- COMPATIBLE WITH MK5033, MK50351 ENCODER/DECODER AND WITH MK68591/2 SERIAL INTERFACE ADAPTOR

Figure 1 : Pin Connections.



DESCRIPTION

The 5032 variable Bit-Rate LANCE is a 48-pin VLSI device that simplifies the interfacing of a microcomputer or a minicomputer to an IEEE 802.3 Local Area Network.

PIN DESCRIPTION

DAL00-DAL15

(Data/Address Bus)

Input/Output Three State. The time multiplexed Address/Data bus. These lines will be driven as a bus master and as a bus slave.

READ

Input/Output Three State. Indicates the type of operation to be performed in the current bus cycle. When it is a bus master, MK5032 drives this signal.

MK5032 as bus slave :

High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.

MK5032 as bus master :

High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

$\overline{\text{INTR}}$

(Interrupt)

Output Open Drain. When enabled, an attention signal that indicates the occurence of one or more of the following events : a message reception or transmission has completed or an error has occured during the transaction ; the initialization procedure has completed ; or a memory error has been encountered. Setting INEA in CSR0 (bit 06) enables $\overline{\text{INTR}}$.

DALI

(Data/Address Line In)

Output Three State. An external bus transceiver control line. When MK5032 is a bus master and reads from the DAL lines, DALI is asserted during the data portion of the transfer.

$\overline{\text{DALO}}$

(Data/Address Line Out)

Output Three State. An external bus transceiver control line. When MK5032 is a bus master and drives the DAL lines, $\overline{\text{DALO}}$ is asserted during the address portion of a read transfer of for the duration of a write transfer.

$\overline{\text{DAS}}$
(Data Strobe)

Input/Output Three State. Defines the data portion of the bus transaction. DAS is driven is driven only as a bus master.

$\overline{\text{BM0}}$, $\overline{\text{BM1}}$ OR BYTE, $\overline{\text{BUSAKO}}$
(Byte Mask)

Output Three State. Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting $\overline{\text{RESET}}$ clears CSR3.

CSR3(00) BCON = 0

PIN 16 = $\overline{\text{BM1}}$ (Output Three State)

PIN 15 = $\overline{\text{BM0}}$ (Output Three State)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The BM lines are ignored as a bus slave and assume word transfers only. The MK5032 drives the BM lines only when it is a bus master. Byte selection occurs as follows :

$\overline{\text{BM1}}$	$\overline{\text{BM0}}$	
Low	Low	Whole Word
Low	High	Byte of DAL 08 - DAL 15
High	Low	Byte of DAL 00 - DAL 07
High	High	None

CSR3(00) BCON = 1

PIN 16 = $\overline{\text{BUSAKO}}$ (Output)

PIN 15 = BYTE (Output Three State)

BYTE. An alternate byte selection line. Byte selection occurs when the BYTE and DAL (00) lines are latched during the address portion of the bus transaction. BYTE, $\overline{\text{BM0}}$ and $\overline{\text{BM1}}$ are ignored when MK5032 is a bus slave. There are two modes of ordering bytes depending on bit (02) of CSR3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with various 16-bit microprocessors.

BSWP = 0		BSWP = 1		
BYTE	DAL(00)	BYTE	DAL(00)	
Low	Low	Low	Low	Whole Word
Low	High	Low	High	Illegal Condition
High	High	High	Low	Upper Byte
High	Low	High	High	Lower Byte

$\overline{\text{BUSAKO}}$. The DAM daisy chain output.

$\overline{\text{HOLD}}$/BUSRQ
(Bus Hold Request)

Input/Output Open Drain. MK5032 asserts this signal when it requires access to memory. HOLD is held low for the entire bus transaction. This bit is programmable through bit (00) of CSR3 (known as BCON) In the daisy chain DAM mode (BCON = 1) $\overline{\text{BUSRQ}}$ is asserted only if $\overline{\text{BUSRQ}}$ is inactive prior to assertion. Bit (00) of CSR3 is cleared when $\overline{\text{RESET}}$ is asserted.

CSR3(00) BCON = 0

PIN 17 = $\overline{\text{HOLD}}$ (Output Open Drain)

CSR3(00) BCON = 1

PIN 17 = $\overline{\text{BUSRQ}}$ (Output Open Drain)

BUSRQ will be asserted only if PIN 17 is high prior to assertion.

ALE/$\overline{\text{AS}}$
(Address Latch Enable)

Output Three State. Used to demultiplex the DAL lines and define the address portion of the bus cycle. This pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from high to low at the end of the address portion of the bus the address portion of the bus transaction and remains low during the entire data portion of the transaction. As $\overline{\text{AS}}$, the signal transitions from low to high at the end of the address portion of the bus transaction and remains high throughout the entire data portion of the transaction. The MK5032 drives the ALE/$\overline{\text{AS}}$ line only as a bus master.

CSR3(01) ACON = 0

PIN 18 = ALE

CSR3(01) ACON = 1

PIN 18 = $\overline{\text{AS}}$

$\overline{\text{HLDA}}$
(Bus Hold Acknowledge)

Input. A response to $\overline{\text{HOLD}}$ indicating that the MK5032 is the Bus Master. HLDA stops its response when HOLD ends its assertion.

$\overline{\text{CS}}$
(Chip Select)

Input. When asserted, $\overline{\text{CS}}$ indicates MK5032 is the slave device of the data transfer. $\overline{\text{CS}}$ must be valid throughout the data portion of the bus cycle.

$\overline{\text{ADR}}$
(Register Address Port Select)

Input. When $\overline{\text{CS}}$ is asserted, ADR indicates which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

DATA	PORT
Low	Register Data Port
High	Register Address Port

$\overline{\text{READY}}$

Input/Output Open Drain. When the MK5032 is a bus master, $\overline{\text{READY}}$ is an asynchronous acknow-

ledgement from external memory that will complete the data transfer. As a bus slave, the chip asserts READY when it has put data on the bus, or is about to take data off the bus. READY is a response to DAS. READY negates after DAS negates. Note : If DAS or CS deassert prior to the assertion of READY, READY cannot assert.

RESET

Input. Bus reset signal. Causes MK5032 to cease operation and to enter an idle state.

SCLK
(System Clock)

Input. A clock from 1 to 10MHz.

TENA
(Transmit Enable)

Output. Transmit Output Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)

Input. Normally a 6 square wave synchronized to the receive data and present only while receiving an input bit stream.

CLSN
(Collision)

Input. A logical input that indicates that a collision is occuring on the channel.

TX
(Transmit)

Output. Transmit output bit stream. This pin is programmable through bit (07) of the MODE REGISTER (MAN). When this bit is a "zero" the output data stream will be NRZ. When MAN is set to a "one", the data will be Manchester Encoded starting at a zero level and ending at the end of packet in a marking condition. (Continuous one level). This mode will function only when the data rate is programmed less than the rate of SCLK.

Three other bits in the MODE register provide a data rate division of 1, 2, 4, 6, 8, or 10. This means that the data rate of TX will be a division of SCLK. For more details on the MODE register, see the technical manual.

RENA
(Receive Enable)

Input. A logical input that indicates the presence of data on the channel.

RX
(Receive)

Input. Receive input bit stream.

A16 - A23
(High-Order Address Bus)

Output Three State. The additional address bits necessary to extend the DAL lines to produce a 24-bit address. These lines will be driven only as a bus master.

VCC

Power supply pin. + 5VDC ± 5 percent.

Filtering : A power supply filter is recommended at the MK5032 between V_{CC} (48) and V_{SS} (1, 24). This filter consists of two capacitors in parallel having the values of 10 µf and 0.47 µf respectively.

VSS

Ground. 0 VDC.

FUNCTIONAL CAPABILITIES

The MK5032 interfaces to a microprocessor bus characterized by time-multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The IEEE 802.3 packet format consists of 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The packets' variable widths accommodate both short-status command and terminal traffic packets and long data packets to printers and disks (1024-byte disk sectors, for example). Packets are spaced a minimum of 96 bit times apart to allow one node enough time to receive back-to-back packets.

The MK5032 operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between chip and processor. During initialization, the control processor loads the starting address of the initialization block plus the operating mode of the chip via two ports that can access four control registers into MK5032. The host processor talks directly to MK5032 only during this initial phase. All further communications are handled via a Direct Memory Access (DMA) machine under microword control contained within MK5032. Figure 2 shows a block diagram of the MK5032 and PLS (MK68591, MK50351, or MK5033) device used to create an IEEE 802.3 interface for a computer system.

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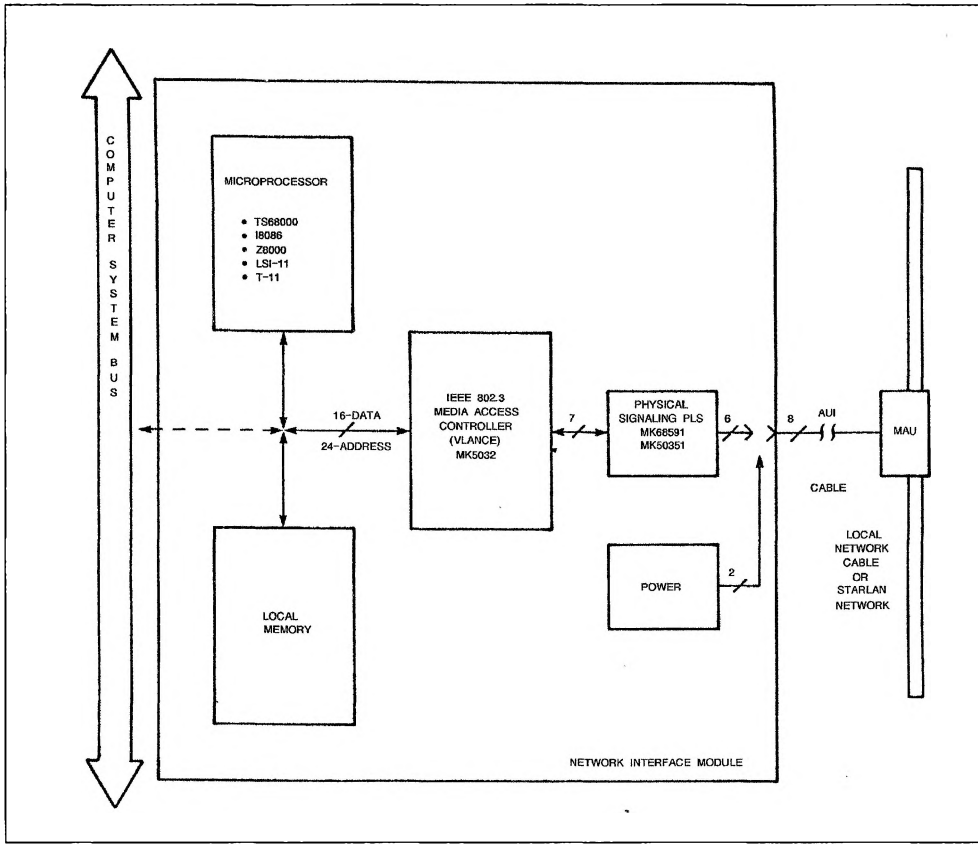
Figure 2 : Ethernet Local Area Network System Block Diagram.



FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

MK5032 provides the IEEE 802.3 interface as follows. In the transmit mode (since there is only one transmission path, IEEE 802.3 is a half duplex system), the MK5032 reads data from a transmit buffer by using DMA and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set in RDM1 of the receiver descriptor ring. In the receive mode, MK5032 accepts packets under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the MK5032 during an initialization cycle. There are two types of logical addresses. One is a group type mas ; where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical

ation is the so called "promiscuous mode" in which a node will accept all packets on the cable regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The IEEE 802.3 CSMA/CD network access algorithm is implemented completely within MK5032. In addition to listening for a clear network cable before transmitting, IEEE 802.3 handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. MK5032 is constantly monitoring the Collision (CLSN) pin. This signal is generated by the MAU when the signal level on the network cable indicates the presence of signals from two or more transmitters. If MK5032 is transmitted when CLSN is asserted, it will continue to transmit the preamble (collisions normally occur while the preamble is being transmitted), then will "jam" the network for 32 bit times. This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the IEEE 802.3 specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attemps to transmit packet, MK5032 will report a RTRY error due to excessive collisions and step over the transmitter buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, MK5032 will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error.

Fatal error reporting is provided by the MK5032 through a microprocessor interrupt and error flags in CSR0. These error conditions are collision error (the failure of the MAU to send a signal-quality-error message at the conclusion of a normal transmission), transmitter ON longer than 1518 bytes, a missed packet, and a memory error (failure of a memory transaction to complete within 256 sys clocks).

Additional errors are reported through bits in the descriptor rings (on a buffer by buffer basis). Receive error conditions include framing, CRC and buffers errors, and overflow. Transmit descriptor rings have error bits indicating buffer, underflow, late collision, and loss of carrier. Additionally, transmit descriptor rings have a bit indicating that the transmitter has unsuccessfully tried to transmit over a busy communication link.

Transmit descriptor rings also have ten bits reserved for a Time Domain Reflectometry counter (TDR). On the occurance of a collision, the value in the TDR will give the number of system clocks until the collision, which can be used to determine the distance to the fault.

BUFFER MANAGEMENT

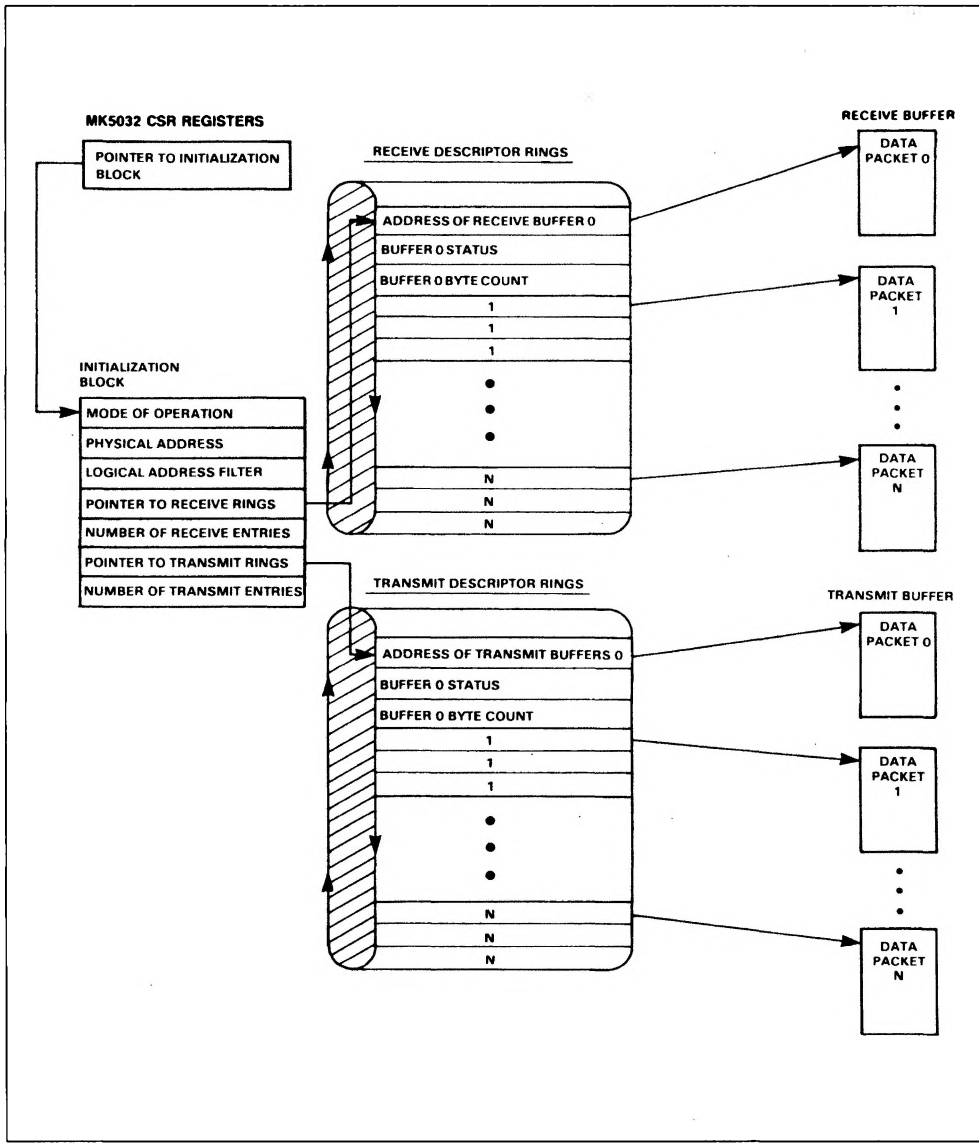
A key feature of the MK5032 and its DMA channel is the flexibility and speed of communication between the MK5032 and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown if figure 3. These rings control both transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring for execution by the MK5032. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The MK5032 searches the descriptor rings to determine the next empty buffer. This enables it to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

The parallel interface of MK5032 has been designed to be "friendly", or easy to interface, to many popular 16-bit microprocessors. These microprocessors include the TS68000, Z8000, 8086, LSI-11, T-11. MK5032 has a wide 24-bit linear address space when in the Bus Master Mode, allowing it to DMA the entire address space of the above microprocessors. MK5032 uses no segmentation or paging methods. As such, MK5032 addressing is closest to MK68000 addressing, but is compatible with the other microprocessors. When MK5032 is a bus master, a programmable mode of operation allows byte addressing, either by employing a Byte/Word control signal (much like that used on the 8086 or the Z8000) or by using an Upper Data Strobe/Lower Data Strobe much like that used on the TS68000, LSI-11 microprocessors. A programmable polarity on the Address Strobe signal eliminates the need for external logic. MK5032 interfaces with multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

After the initialization routine, packet reception or transmission, transmitter timeout error, a missed packet, or memory error, the MK5032 generates an interrupt to the host microprocessor.
The cause of the interrupt is ascertained by reading CSR0.Bit (06) of CSR0, INEA, enables or disables interrupts to the micorprocessor. In the polling mode, BIT (07) of CSR0 is sampled to determine if an interrupt causing condition has occurred.

Figure 3 : MK5032 Memory Management.



MK5032 INTERFACE DESCRIPTION

ALE, $\overline{DAS}$ and $\overline{READY}$ time all data transfers from the MK5032 in the Bus Master mode. The automatic adjustment of the MK5032 cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600ns long and can be increased in 100ns increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals (BM0 and BM1) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or AS strobes the addresses A0-A15 into the external latches. Approximately 100ns later, DAL00-DAL15 go into a three state mode. There is a 50ns delay to allow for tranceiver turnaround, then DAS falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the MK5032 stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200ns).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, control the bus transceivers. DALI signals to strobe data toward the MK5032 and DALO signals to strobe data or addresses away from the MK5032. During a read cycle, DALO goes inactive before DALI goes active to avoid "spiking" of bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or AS pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 are stable. This data remains valid on the bus until the memory device asserts $\overline{READY}$. At this point, $\overline{DAS}$ goes inactive, latching data into the memory device. Data is held for 75ns after the negation of $\overline{DAS}$.

MK5032 INTERFACE DESCRIPTION BUS SLAVE MODE

The MK5032 enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the MK5032 must be stopped (CSR0 bit 02) when CSR1, CSR2, or CSR3 is to be written to or read.

MK5032 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_A	Temperature Under Bias	− 25 to + 125	°C
T_{stg}	Storage Temperature	− 65 to + 150	°C
V_I	Voltage on any Pin with Respect to Ground	− 0.3 to + 7	V
P_D	Power Dissipation	2.0	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = + 5V ± 5 percent unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Input Low Voltage	− 0.5	+ 0.8	V
VI_H	Input High Voltage	+ 2.0	V_{CC} +0.5	V
V_{OL}	Output Low Voltage		+ 0.5	V
V_{OH}	Output High Voltage	+ 2.4		V
I_{IL}	Input Leakage		± 10	µA

CAPACITANCE F = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output		10	pF
C_{IO}			20	pF

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5 percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
1	SCLK	T_{SCT}	SCLK Period		99		101
2	SCLK	T_{SCL}	SCLK Low Time		45		55
3	SCLK	T_{SCH}	SCLK High Time		45		55
4	SCLK	T_{SCR}	Rise Time of SCLK		0		8
5	SCLK	T_{SCF}	Fall Time of SCLK		0		8
6	TENA	T_{TEP}	TENA Propagation delay after the rising edge of SCLK.	C_L = 50pF			75
7	TENA	T_{TEH}	TENA Hold Time after the rising edge of SCLK.	C_L = 50pF	5		
8	TX	T_{TDP}	TX data propagation delay after the rising edge of SCLK. (see note 1)	C_L = 50pF			75
8A	TX	T_{TDTT}	TX Transition - Transition (see note 2)	C_L = 50pF	B_t - 7		B_t - 7
9	TX	T_{TDH}	TX data Hold Time after the rising edge of SCLK. (see note 1)	C_L = 50pF	5		
10	RCLK	T_{RCT}	RCLK Period		85		118
11	RCLK	T_{RCH}	RCLK High Time		38		
12	RCLK	T_{RCL}	RCLK Low Time		38		
13	RCLK	T_{RCR}	Rise Time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX Data Rise Time		0		8
16	RX	T_{RDF}	RX Data Fall Time		0		8
17	RX	T_{RDH}	RX Data Hold Time (RCLK to RX data change)		5		
18	RX	T_{RDS} (see note 3)	RX Data Setup Time (RX data stable to the rising edge of RCLK)		See note 3		
19	RENA	T_{DPL}	RENA Low Time		120		
20	RENA	T_{RENH}	RENA Hold Time after rising edge of RCLK.		40		
21	CLSN	T_{CPH}	CLSN High Time		80		
22	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (bus master)		0		

AC TIMING SPECIFICATIONS (continued)

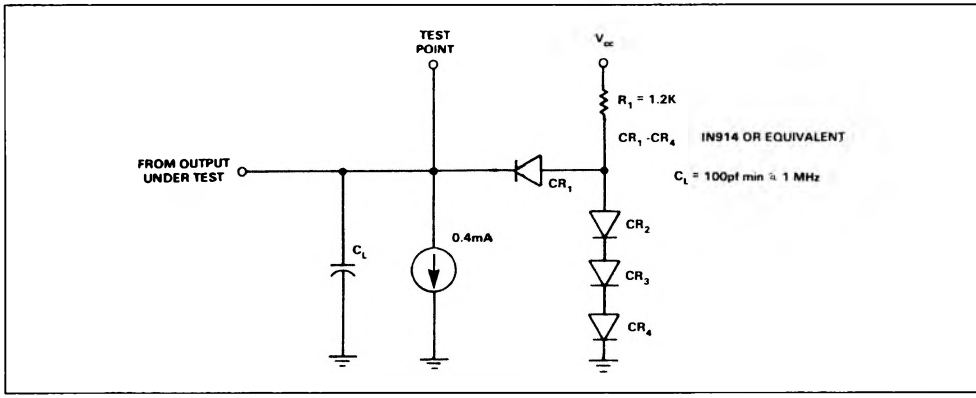
N°	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
25	$\overline{\text{RESET}}$	T_{RW}	$\overline{\text{RESET}}$ Pulse Width Low		200		
26	A/DAL	T_{CYCLE}	Read/Write, Address/Data Cycle time		600		
27	A	T_{XAS}	Address setup time to the falling edge of ALE.		75		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{\text{DAS}}$.		15		
29	DAL	T_{AS}	Address setupt time to the falling edge of ALE.		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE.		35		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{\text{DAS}}$ (bus master read).		50		
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{\text{DAS}}$ (bus master read).		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{\text{DAS}}$ (bus master write).		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{\text{DAS}}$ (bus master write).		200		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{\text{DAS}}$ (bus master write).		35		
36	DAL	T_{SD01}	Data driver delay after the falling edge of $\overline{\text{DAS}}$ (bus slave read).	(CSR 0, 3, RAP)		400	
37	DAL	T_{SD02}	Data driver delay after the falling edge of $\overline{\text{DAS}}$ (bus slave read).	(CSR 1, 2)		1200	
38	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{\text{DAS}}$ (bus slave read).		0		35
39	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{\text{DAS}}$ (bus slave write).		0		
40	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{\text{DAS}}$ (bus slave write).		0		
41	ALE	T_{ALEW}	ALE Width High		120		150
42	ALE	T_{DALE}	Delay from rising edge of $\overline{\text{DAS}}$ to the rising edge of ALE.		70		
43	$\overline{\text{DAS}}$	T_{DSW}	$\overline{\text{DAS}}$ Width Low		200		
44	$\overline{\text{DAS}}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{\text{DAS}}$.		80		130
45	$\overline{\text{DAS}}$	T_{RIDF}	Delay from the rising edge of $\overline{\text{DALO}}$ to the falling edge of $\overline{\text{DAS}}$ (bus master read).		15		
46	$\overline{\text{DAS}}$	T_{RDYS}	Delay from the falling edge of $\overline{\text{READY}}$ to the rising edge $\overline{\text{DAS}}$.	Taryd = 300ns	75		250
47	$\overline{\text{DALI}}$	T_{ROIF}	Delay from the rising edge of $\overline{\text{DALO}}$ to the falling edge of $\overline{\text{DALI}}$ (bus master read).		15		

AC TIMING SPECIFICATIONS (continued)

N°	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
48	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (bus master read).		135		
49	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time to the rising edge of $\overline{DAS}$ (bus master read).		0		
50	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (bus master read).		55		
51	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (bus master read).		110		
52	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (bus master read).		35		
53	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (bus master write).		35		
54	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (bus slave).		0		
55	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (bus slave).		0		
56	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (bus slave).		0		
57	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (bus slave).		0		
58	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600ns).				80
59	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (bus slave read).		75		
60	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus master).		0		
61	$\overline{READY}$	T_{SR01}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (bus slave).	(CSR 0, 3, RAP)		600	
62	$\overline{READY}$	T_{SR02}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (bus slave).	(CSR 1, 2)		1400	
63	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus slave).		0		35
64	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (bus slave).		0		
65	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (bus slave).		0		

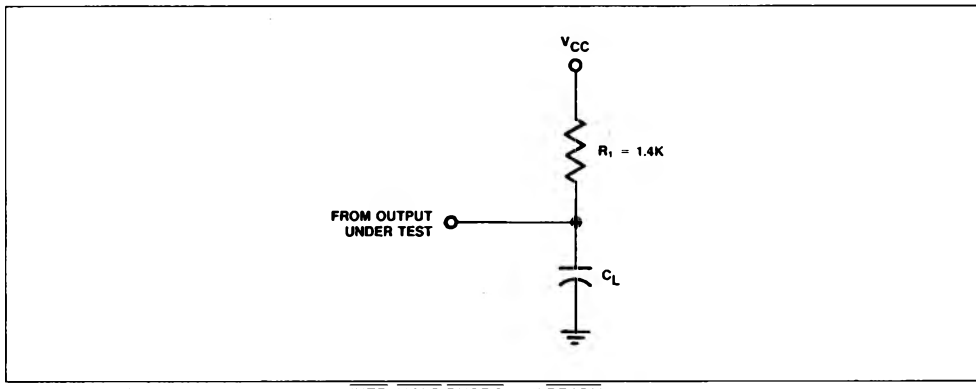
Notes : 1. This timing is for the NRZ mode only.
2. B_t = Bit time. This measurement is during preamble ; valid for Manchester Mode only.
3. $T_{RDS\ (min)} = T_{RCT} - 25ns$. Therefore, $T_{RCT} = 100ns$ when $T_{RDS\ (min)} = 75ns$.

Figure 4 : Output Load Diagram.



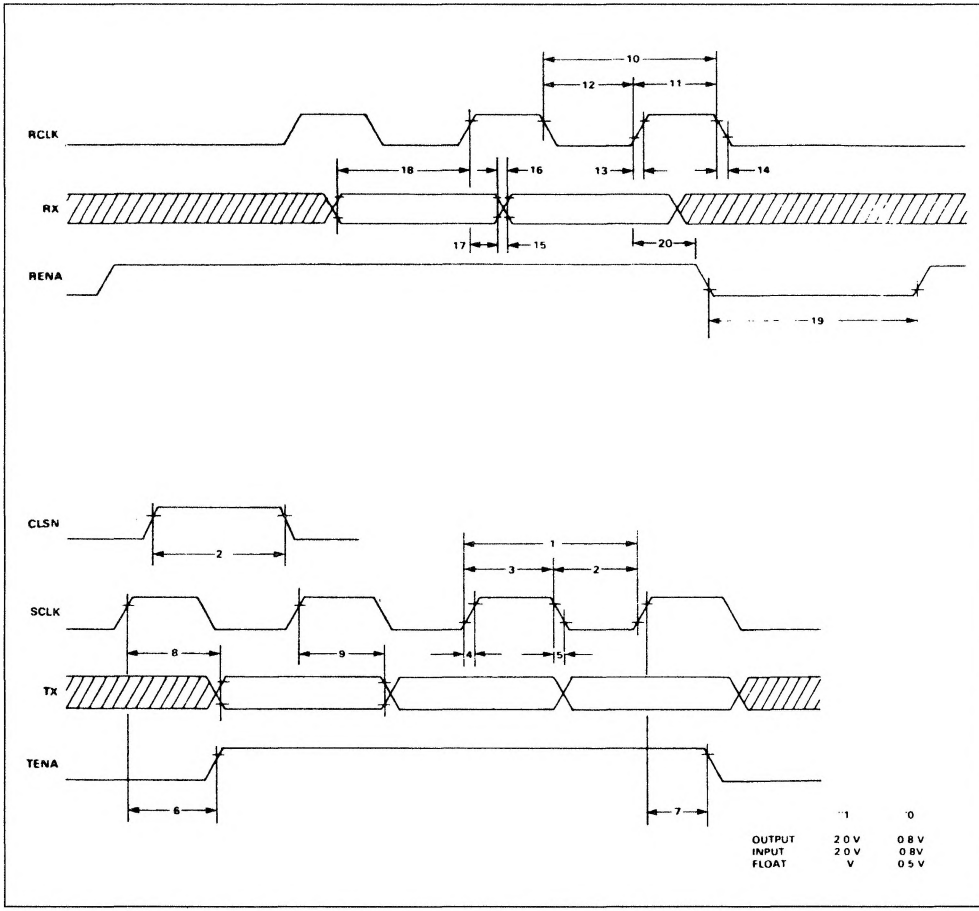
Note : This load is used on DAL00 through DAL15, READ, DALI, DALO, DAS, BM0, BM1 ALE/AS, A16 through A23, TENA, and TX.

Figure 5 : Open Drain Output Load Diagram.



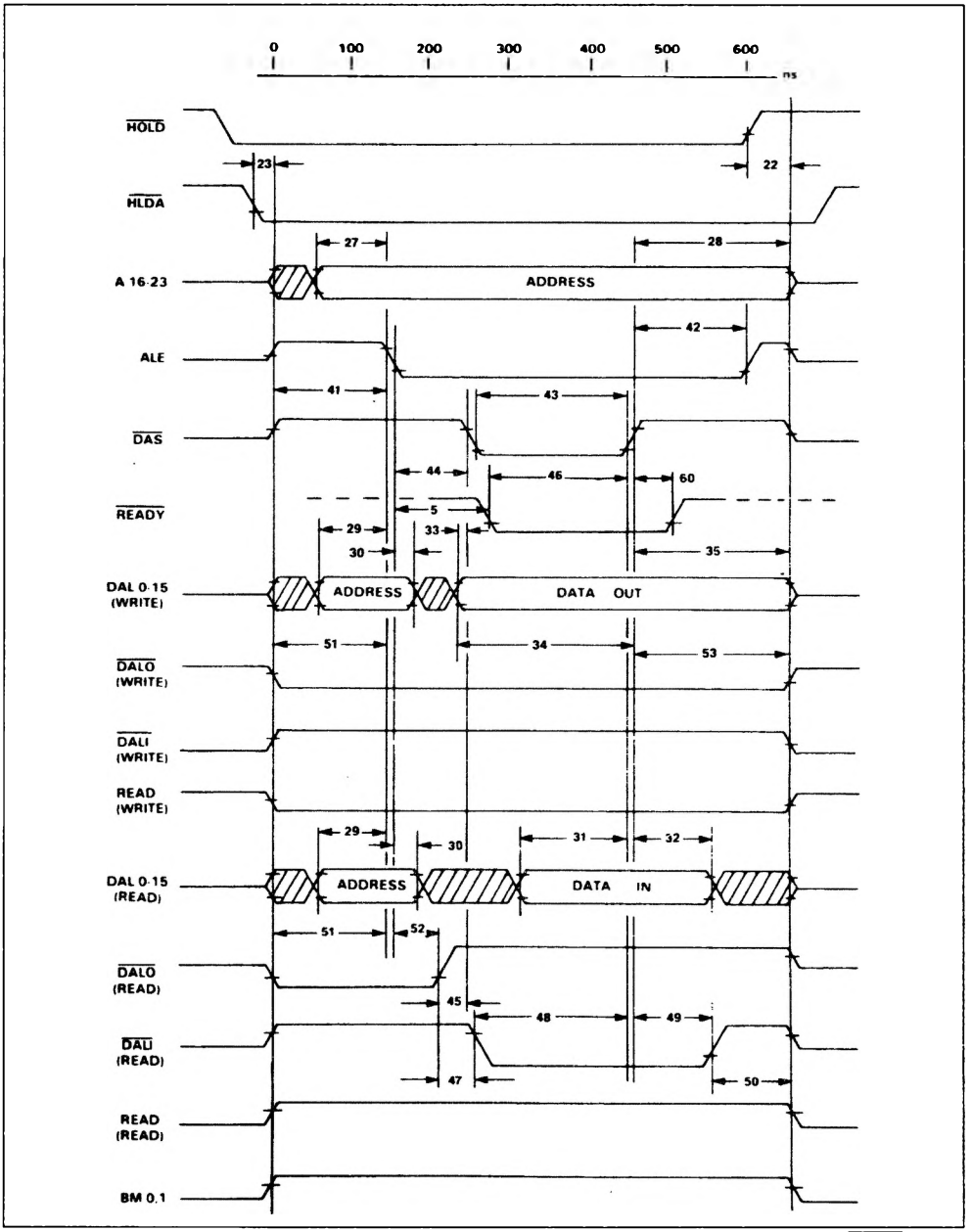
Note : This load is used on open drain outputs $\overline{INTR}$, $\overline{HOLD}$/$\overline{BUSRQ}$, and $\overline{READY}$.

Figure 6 : Physical Link Signaling Timing Diagram - PLS-VMAC Interface Signals.



Note : Timing measurements are made at the following voltages unless otherwise specified.

Figure 7 : MK5032 Bus Master Timing Diagram.



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 8 : MK5032 Bus Slave Timing Diagram.