SGS-THOMSON
MICROELECTRONICS

MK5027

SS7 SIGNALLING
LINK CONTROLLER

- CMOS
- FULLY COMPATIBLE WITH BOTH 8 OR 16 BIT SYSTEMS
- SYSTEM CLOCK RATE TO 10MHz
- DATA RATE UP TO 2.5Mbps FOR SS7 PROTOCOL PROCESSING , 7Mbps FOR TRANSPARENT HDLC MODE
- COMPLETE LEVEL 2 IMPLEMENTATION
- COMPATIBLE WITH 1988 CCITT, AT&T, ANSI, AND BELLCORE SIGNALLING SYSTEM NUMBER 7 LINK LEVEL PROTOCOLS
- 52 PIN PLCC AND 48-PIN DIP PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON X.25 CHIP (MK5025) AND NEARLY PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON VLANCE CHIP (MK5032)
- BUFFER MANAGEMENT INCLUDES :
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- ON CHIP DMA CONTROL WITH PROGRAMMABLE BURST LENGTH
- SELECTABLE BEC OR PCR RETRANSMISSION METHODS, INCLUDING FORCED RETRANSMISSION FOR PCR
- HANDLES ALL 7 SS7 TIMERS
- HANDLES ALL SS7 FRAME FORMATTING :
  - Zero bit insert and delete
  - FCS generation and detection
  - Frame delimiting with flags
- PROGRAMMABLE MINIMUM SIGNAL UNIT SPACING (number of flags between SU's)
- HANDLES ALL SEQUENCING AND LINK CONTROL.
- SELECTABLE FCS OF 16 OR 32 BITS
- TESTING FACILITIES :
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE
- PROGRAMMABLE FOR FULL OR HALF DUPLEX OPERATION

DESCRIPTION

The SGS-Thomson Signalling System #7 Signalling Link Controller (MK5027) is a VLSI semiconductor device which provides a complete link control function conforming to the 1988 CCITT version of SS7. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by two types of retransmission, error monitoring, sequence number control, link status control, and FISU generation. One of the outstanding features of the MK5027 is its buffer management which includes on-chip DMA. This feature allows users to handle multiple packets of receive and transmit data at a time. (A conventional data link control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK5027 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.
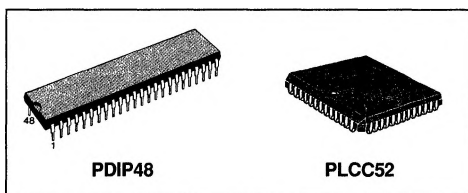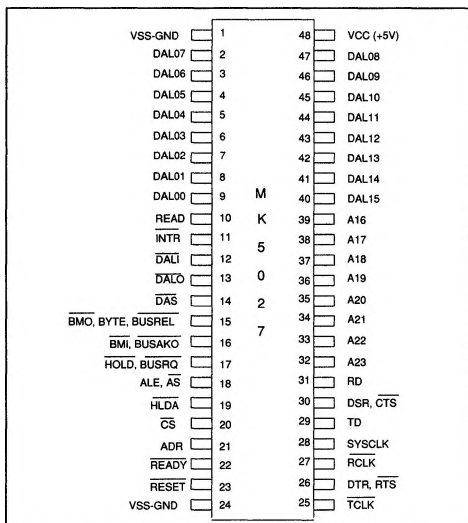

PDIP48   PLCC52

Figure 1 : Pin Connection.

VSS-GND	1	48	VCC (+5V)
DAL07	2	47	DAL08
DAL06	3	46	DAL09
DAL05	4	45	DAL10
DAL04	5	44	DAL11
DAL03	6	43	DAL12
DAL02	7	42	DAL13
DAL01	8	41	DAL14
DAL00	9	40	DAL15
READ	10	39	A16
INTR	11	38	A17
DALI	12	37	A18
DALO	13	36	A19
DAS	14	35	A20
BMO, BYTE, BUSREL	15	34	A21
BMI, BUSAKO	16	33	A22
HOLD, BUSRQ	17	32	A23
ALE, AS	18	31	RD
HLDA	19	30	DSR, CTS
CS	20	29	TD
ADR	21	28	SYSCLK
READY	22	27	RCLK
RESET	23	26	DTR, RTS
VSS-GND	24	25	TCLK

(MK5027 marked in center of pin diagram)

Table 1 : Pin Description.

LEGEND :

I	Input only	O	Output only
IO	Input/Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Signal Name	Pin(s)	Type	Description
DAL<15:00>	2-9 40-47	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.

READ	10	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5027 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times.
			MK5027 as a Bus Slave :
			  READ = HIGH - Data is placed on the DAL lines by the chip.
			  READ = LOW - Data is taken off the DAL lines by the chip.
			MK5027 as a Bus Master :
			  READ = HIGH - Data is taken off the DAL lines by the chip.
			  READ = LOW - Data is placed on the DAL lines by the chip.

$\overline{\text{INTR}}$	11	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set : MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA = 1.
$\overline{\text{DALI}}$	12	O/3S	DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK5027 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.
$\overline{\text{DALO}}$	13	O/3S	DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by the MK5027 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{\text{DAS}}$	14	IO/3S	DATA STROBE defines the data portion of a transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. This signal is driven by the MK5027 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
$\overline{\text{BMO}}$ $\overline{\text{BYTE}}$ $\overline{\text{BUSREL}}$	15	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5027 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear the pin 15 is an output and behaves as described below for pin 16.

Note : Pin out shown is for 48 pin dip.

SGS-THOMSON
MICROELECTRONICS

Table 1 : Pin Description (continued).

Signal Name	Pin(s)	Type	Description

$\overline{BM1}$ $\overline{BUSAKO}$	16	O/3S	Pins 15 and 16 are programmable though bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0,
			 I/O PIN 15 = BM0 (O/3S)
			 I/O PIN 16 = BM1 (O/3S)
			 BYTE MASK<1:0> indicates the byte(s) on the DAL to be read or written during this bus transaction. MK5027 drives these lines only as a Bus Master. MK5027 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table.
			
			 BM1 BM0 TYPE OF TRANSFER
			
			 LOW LOW ENTIRE WORD
			 LOW HIGH UPPER BYTE
			                   (DAL<15:08>)
			 HIGH LOW LOWER BYTE
			                   (DAL<07:00>)
			 HIGH HIGH NONE
			
			 If CSR4<00> BCON = 1,
			 I/O PIN 15 = BYTE (O/3S)
			 I/O PIN 16 = $\overline{BUSAKO}$ (O)
			 Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5027 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table.
			
			 BYTE DAL<00> TYPE OF TRANSFER
			
			 LOW LOW ENTIRE WORD
			 LOW HIGH ILLEGAL CONDITION
			 HIGH LOW LOWER BYTE
			 HIGH HIGH UPPER BYTE
			
			 $\overline{BUSAKO}$ is a bus request daisy chain output. If MK5027 is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If MK5027 is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high.
			 Note : All transfers are entire word unless the MK5027 is configured for 8 bit operation.

Table 1 : Pin Description (continued).

Signal Name	Pin(s)	Type	Description

$\overline{\text{HOLD}}$ $\overline{\text{BUSRQ}}$	17	IO/OD	Pin 17 is configured through bit 0 of CSR4.
			If CSR4<00> BCON = 0,
			  I/O PIN 17 = $\overline{\text{HOLD}}$
			$\overline{\text{HOLD}}$ request is asserted by MK5027 when it requires a DMA cycle, if $\overline{\text{HLDA}}$ is inactive, regardless of the previous state of the $\overline{\text{HOLD}}$ pin. $\overline{\text{HOLD}}$ is held low for the entire ensuing bus transaction.
			If CSR4<00> BCON = 1,
			  I/O PIN 17 = $\overline{\text{BUSRQ}}$
			$\overline{\text{BUSRQ}}$ is asserted by MK5027 when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high and $\overline{\text{HLDA}}$ is inactive. $\overline{\text{BUSRQ}}$ is held low for the entire ensuing bus transaction.

ALE $\overline{\text{AS}}$	18	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK5027 while it is the BUS MASTER. At all other times, the signal is tristated.
			If CSR4<01> ACON = 0,
			  I/O PIN 18 = ALE
			ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion.
			If CSR4<01> ACON = 1,
			  I/O PIN 18 = $\overline{\text{AS}}$
			As $\overline{\text{AS}}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{\text{AS}}$ can be used by a slave device to strobe the address into a register.
			$\overline{\text{AS}}$ is effectively the inversion of ALE.

$\overline{\text{HLDA}}$	19	I	HOLD ACKNOWLEDGE is the response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to MK5027's assertion of $\overline{\text{HOLD}}$, the MK5027 is the Bus Master. $\overline{\text{HLDA}}$ should be desasserted ONLY after $\overline{\text{HOLD}}$ has been released by the MK5027.

SGS-THOMSON
MICROELECTRONICS

Table 1 : Pin Description (continued).

Signal	Pin(s)	Type	Description
$\overline{CS}$	20	I	CHIP SELECT indicates, when low, that the MK5027 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	21	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
$\overline{READY}$	22	IO/OD	When the MK5027 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a bus Slave, the MK5027 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be released after $\overline{DAS}$ or $\overline{CS}$ is negated.
$\overline{RESET}$	23	I	$\overline{RESET}$ is the Bus signal that will cause MK5027 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.
$\overline{TCLK}$	25	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may not be greater than the frequency of SYSCLK.
$\overline{DTR}$ $\overline{RTS}$	26	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5027 will assert this pin if it has data to send and throughout the transmission of a signal unit.
$\overline{RCLK}$	27	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may not be greater than the frequency of SYSCLK.
SYSCLK	28	I	SYSTEM CLOCK. System clock used for internal timing of the MK5027. SYSCLK should be a square wave, of frequency up to 10 MHz.
TD	29	O	TRANSMIT DATA. Transmit serial data output.
$\overline{DSR}$ $\overline{CTS}$	30	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{CTS}$ or as programmable IO pin DSR. If configured as $\overline{CTS}$, the MK5027 will transmit all ones while $\overline{CTS}$ is high.
RD	31	I	RECEIVE DATA. Received serial data input.
A <23:16>	32-39	O/3S	Address bits <23:16> used in conjunction with DAL <15:00> to produce a 24 bit address. MK5027 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4 <7> BAEN bit.
VSS-GND	1, 24		Ground Pins
VCC	48		Power Supply Pin + 5.0 VDC ± 5%

Figure 2 : Possible System Configuration for the MK5027.
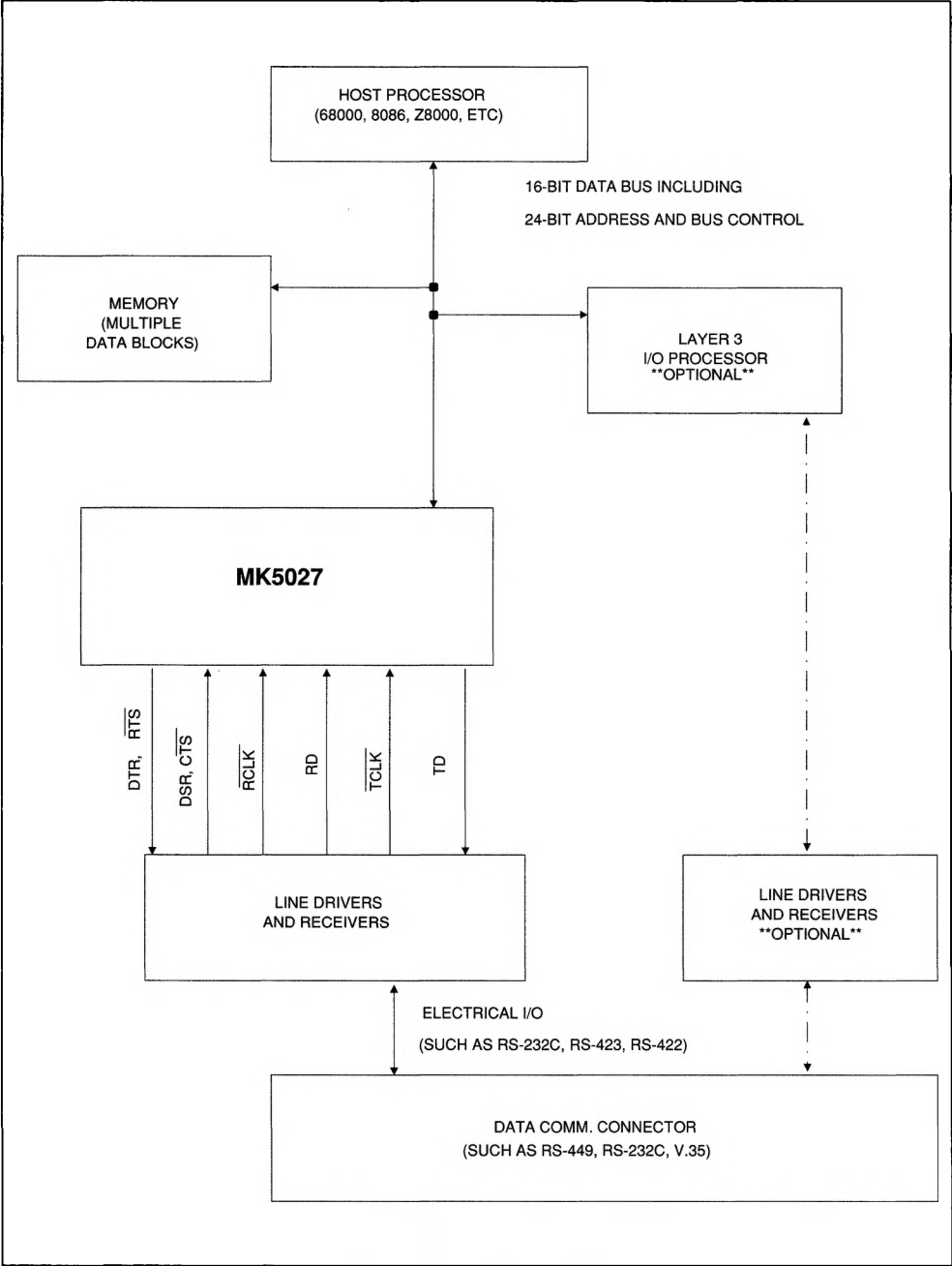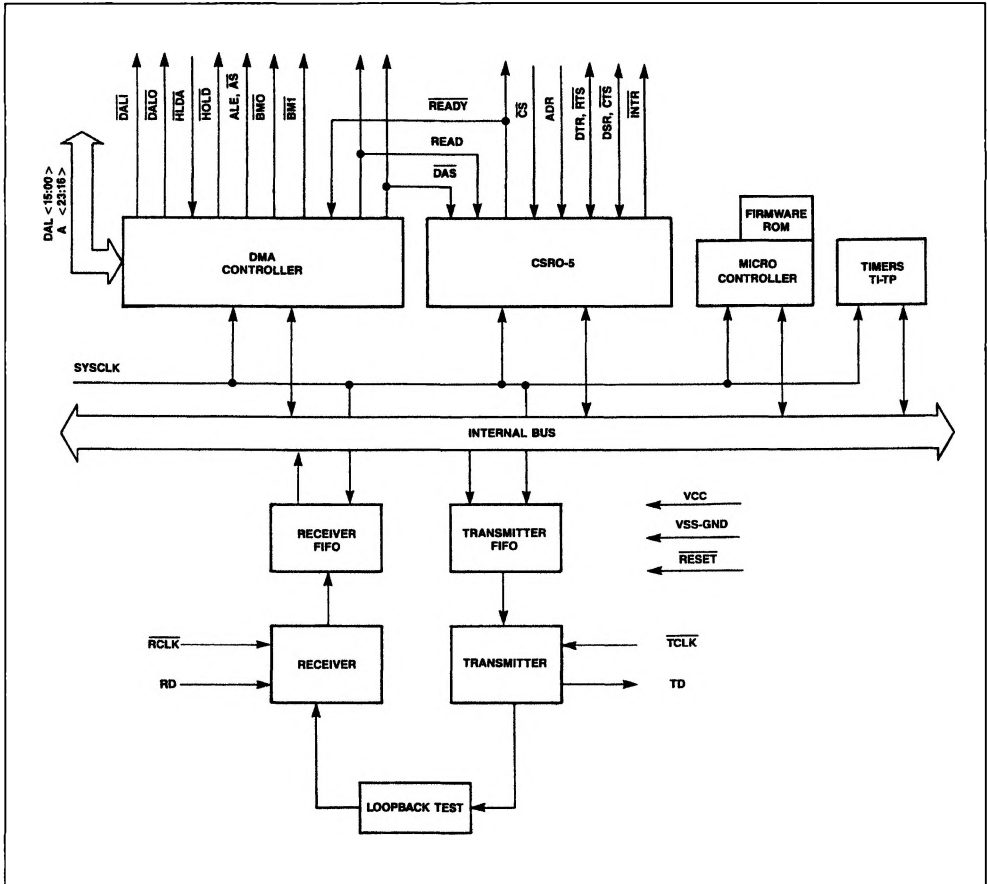
SGS-THOMSON
MICROELECTRONICS

Figure 3 : MK5027 Simplified Block Diagram.

OPERATIONAL DESCRIPTION

The SGS-Thomson Signalling System #7 Signalling Link Controller (MK5027) device is a VLSI product intended for data communication applications requiring SS7 link level control. The MK5027 will perform all frame formatting, such as : frame delimiting with flags, FCS generation and detection. It will also perform all error recovery and link control. The MK5027 also includes a buffer management mechanism that allows the user to transmit and/or receive mutilple MSU's. Contained in the buffer management is an on-chip dual channel DMA : one channel

for receive and one channel for transmit. The MK5027 handles error recovery and link status signalling.

The MK5027 is intended to be used with any popular 16 or 8 bit microprocessor. Possible system configuration for the MK5027 is shown in Figure 2. The MK5027 will move multiple blocks of receive and transmit data directly into and out of memory through the host's bus. An I/O acceleration processor could be used to off-load Higher Level software from the Host. The I/O acceleration processor in Figure 2 is recommended, but not required.

All signal pins on the MK5027 are TTL compatible. This has the advantage of making the MK5027 independent of the physical interface. As shown in Figure 2, line drivers and receivers are used for electrical connection to the physical layer.

SERIAL INTERFACE

The MK5027 provides two seperate serial channels; one for received data and one for transmitted data. These serial channels are completely seperate and may be run at different clock frequencies. The receiver is responsible for recognizing frame boundries, removal of inserted zeroes (for transparency), and checking the incoming FCS. Signal units with incorrect FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring. The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data. The transmitter generates flag sequences for inter-signal unit fill, at least two flags are transmitted between adjacent signal units. The FCS calculations for both directions of serial data optionally follow either the 16-bit CRC-CCITT or the 32-bit CRC-32 algorithms. FCS generation and checking can also be optionally disabled if necessary.

MICROPROCESSOR INTERFACE

The MK5027 contains a dual channel DMA on chip to handle data transfers to and from the host memory. All access to the initialization block and descriptor rings is handled in this way. The address bus is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations, this allows easy interfacing with both 8 and 16 bit processors. DMA transfers can be up to 1, 8 or an unlimited number of words per transfer under program control. During bus slave operation the MK5027 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status, and more. Bus slave mode also allows both 8 and 16 bit accesses.

BUFFER MANAGEMENT

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are seperate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5027. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5027, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5027 owns the buffer, the MK5027 is allowed and commanded to transmit the buffer. When the MK5027 does not own the buffer, it will not transmit that buffer. For receive, when the MK5027 owns a buffer, it may place received data into that buffer. Conversely, when the MK5027 does not own a receive buffer, it will not place received data in that buffer.

The MK5027 buffer management mechanism will handle signal units which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5027 tests the next segment in the descriptor ring in a "look ahead" manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK5027 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on. The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, etc.

Figure 4 : MK5027 Buffer Management.

SGS-THOMSON
MICROELECTRONICS
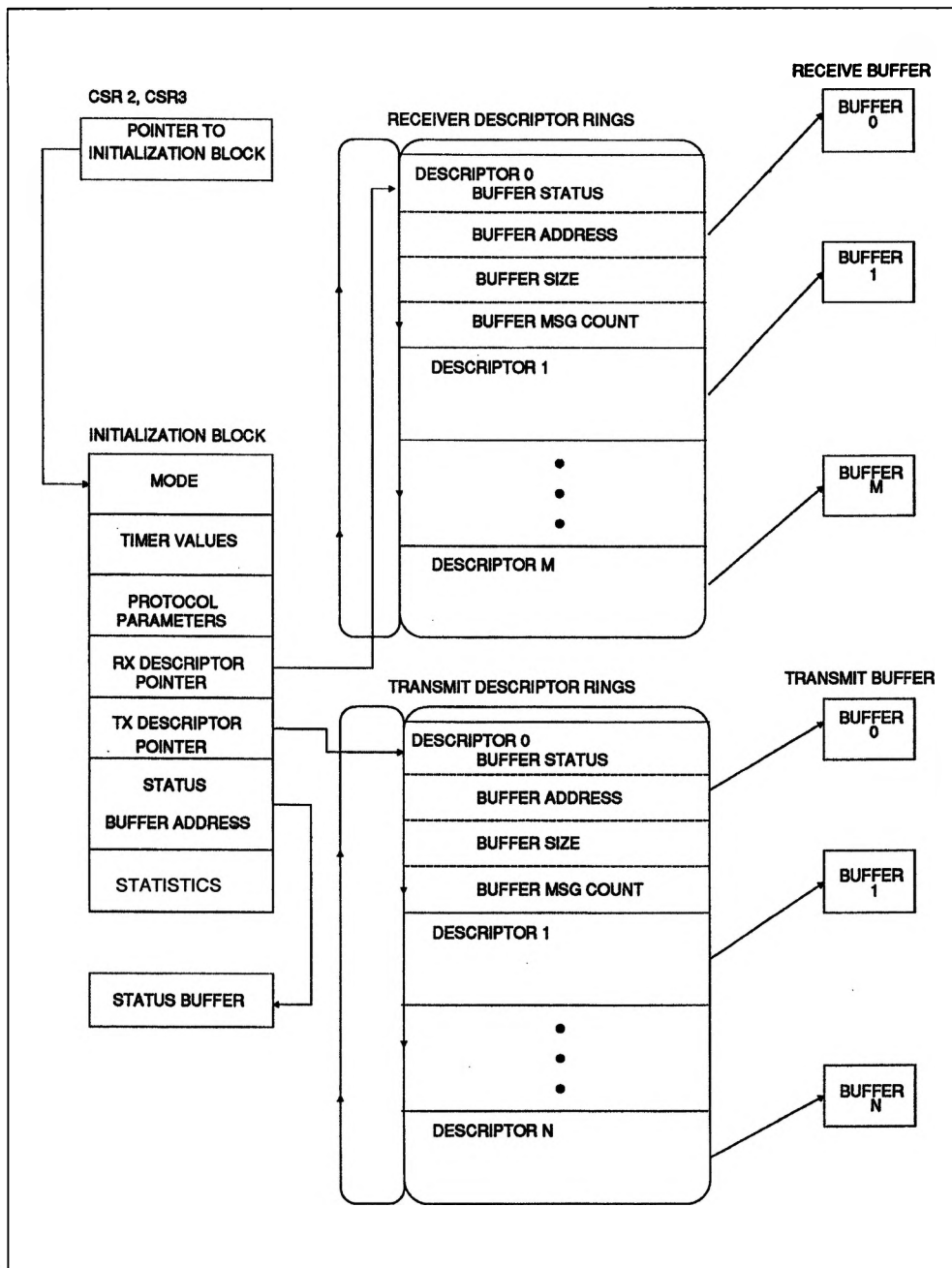
SIGNAL UNIT REPERTOIRE

The signal unit repertoire of the MK5027 is shown in Table 1. This set conforms to the 1988 CCITT specification for level 2 of Signalling System #7.

The definitions for the symbols for the frame types are :

Name	Definition
F	Flag Sequence
FSN	Forward Sequence Number
BSN	Backward Sequence Number
FIB	Forward Indicator Bit
BIB	Backward Indicator Bit
LI	Length Indicator
X	Programmed As Zeroes
SIO	Signalling Information Octet
SIF	Service Information Field
SF	Status Field
FCS	Frame Check Sequence

Table 1 : MK5027 Signal Unit Repertoire.

Message Signal Unit (MSU)

F	FCS	SIF	SIO	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8n,n>=2	8	2	6	1	7	1	7	8

Link Status Signal Unit (LSSU)

F	FCS	SF	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8/16	2	6	1	7	1	7	8

Values for SF:

0 - SIO,	Out of alignment	3 - SIOS,	Out-of-service
1 - SIN,	Normal alignment	4 - SIPO,	Processor outage
2 - SIE,	Emergency	5 - SIB,	Congestion (Busy)

Fill-in Signal Unit (FISU)

F	FCS	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	2	6	1	7	1	7	8

Right-most fields are transmitted first

SGS-THOMSON
MICROELECTRONICS

MK5027 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature under Bias .... − 25°C to + 100°C

Storage Temperature .... − 65°C to + 150°C

Voltage on Any Pin with Respect to Ground .... − 0.5V to VCC + 0.5V

Power Dissipation... 0.50W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect

DC CHARACTERISTICS

$T_A = 0°C$ to 70°C, $V_{CC} = + 5V \pm 5$ percent unless otherwise specified.

Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IL}		− 0.5		+ 0.8	V
V_{IH}		+ 2.0		V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2mA			+ 0.5	V
V_{OH}	@ I_{OH} = − 0.4mA	+ 2.4			V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}			± 10	μA
I_{CC}	@ T_{SCT} = 100ns		50		mA

CAPACITANCE

F = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Capacitance on Input Pins		10	pf
C_{OUT}	Capacitance on Output Pins		10	pf
C_{IO}	Capacitance on I/O Pins		20	pf

AC TIMING SPECIFICATIONS

$T_A = 0°C$ to 70°C, $V_{CC} = + 5V \pm 5$ percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
1	SYSCLK	T_{SCT}	SYSCLK Period		100		2000	ns
2	SYSCLK	T_{SCL}	SYSCLK Low Time		45			ns
3	SYSCLK	T_{SCH}	SYSCLK High Time		45			ns
4	SYSCLK	T_{SCR}	Rise Time of SYSCLK		0		8	ns
5	SYSCLK	T_{SCF}	Fall Time of SYSCLK		0		8	ns
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ Period		140			ns
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ Low Time		63			ns
8	TCLK	T_{TCH}	$\overline{TCLK}$ High Time		63			ns
9	$\overline{TCLK}$	T_{TCR}	Rise Time of $\overline{TCLK}$	CL = 50pF	0		8	ns
10	$\overline{TCLK}$	T_{TCF}	Fall Time of $\overline{TCLK}$		0		8	ns
11	TD	T_{TDP}	TD Data Propagation Delay after the Falling Edge of $\overline{TCLK}$	CL = 50pF			40	ns
12	TD	T_{TDH}	TD Data Hold Time after the Falling Edge of $\overline{TCLK}$		5			ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ Period		140			ns

AC TIMING SPECIFICATIONS (continued)

T_A = 0°C to 70°C, V_{CC} = + 5V ±5 percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ High Time		63			ns
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ Low Time		63			ns
16	$\overline{RCLK}$	T_{RCR}	Rise Time of $\overline{RCLK}$		0		8	ns
17	$\overline{RCLK}$	T_{RCF}	Fall Time of $\overline{RCLK}$		0		8	ns
18	RD	T_{RDR}	RD Data Rise Time		0		8	ns
19	RD	T_{RDF}	RD Data Fall Time		0		8	ns
20	RD	T_{RDH}	RD Hold Time after Rising Edge of $\overline{RCLK}$		5			ns
21	RD	T_{RDS}	RD Setup Time Prior to Rising Edge of $\overline{RCLK}$		30			ns
22	A/DAL	T_{DOFF}	Bus Master Driver Disable after Rising Edge of $\overline{HOLD}$				50	ns
23	A/DAL	T_{DON}	Bus Master Driver Enable after Falling Edge of $\overline{HLDA}$	TSCT=100nS	0		200	ns
24	$\overline{HLDA}$	T_{HHA}	Delay to Falling Edge of $\overline{HLDA}$ from Falling Edge of $\overline{HOLD}$ (bus master)		0			ns
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ Pulse Width		30			ns
26	A/DAL	T_{CYCLE}	Read/write, address/data Cycle Time	TSCT=100nS	600			ns
27	A	T_{XAS}	Address Setup Time to Falling Edge of ALE		100			ns
28	A	T_{XAH}	Address Hold Time after the Rising Edge of $\overline{DAS}$		50			ns
29	DAL	T_{AS}	Address Setup Time to the Falling Edge of ALE		75			ns
30	DAL	T_{AH}	Address Hold Time after the Falling Edge of ALE		20			ns
31	DAL	T_{RDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master read)		55			ns
32	DAL	T_{RDAH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0			ns
33	DAL	T_{DDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master write)		0			ns
34	DAL	T_{WDS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus master write)		250			ns
35	DAL	$\overline{TWDH}$	Data Hold Time to the Rising Edge of $\overline{DAS}$ (bus master write)		35			ns
36	DAL	T_{SRDH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave read)	TSCT=100nS	0		35	ns
37	DAL	T_{SWDH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave write)		0			ns
38	DAL	T_{SWDS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave write)		0			ns
39	ALE	T_{ALEW}	ALE width High		110			ns
40	ALE	T_{DALE}	Delay from Rising Edge of $\overline{DAS}$ to the Rising Edge of ALE		70			ns
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width Low		200			ns

SGS-THOMSON
MICROELECTRONICS

AC TIMING SPECIFICATIONS (continued)

T_A = 0°C to 70°C, V_{CC} = + 5V ±5 percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
42	$\overline{DAS}$	T_{ADAS}	Delay from the Falling Edge of Ale to the Falling Edge of $\overline{DAS}$		80			ns
43	$\overline{DAS}$	T_{RIDF}	Delay from the Rising Edge of $\overline{DALO}$ to the Falling Edge of $\overline{DAS}$ (bus master read)		35			ns
44	$\overline{DAS}$	T_{RDYS}	Delay from the Falling Edge of $\overline{READY}$ to the Falling Edge of $\overline{DAS}$	T_{ARYD}=300ns T_{SCT}=100ns	120		200	ns
45	$\overline{DALI}$	T_{ROIF}	Delay from the Rising Edge of $\overline{DALO}$ to the Falling Edge of $\overline{DALI}$ (bus master read)		70			ns
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ Setup Time to the Rising Edge of $\overline{DAS}$ (bus master read)		150			ns
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0			ns
48	$\overline{DALI}$	T_{RIOF}	Delay from the Rising Edge of $\overline{DALI}$ to the Falling Edge of $\overline{DALO}$ (bus master read)		70			ns
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ Setup Time to the Falling Edge of ALE (bus master read)		110			ns
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ Hold Time after the Falling Edge of ALE (bus master read)		35			ns
51	$\overline{DALO}$	T_{WDSI}	Delay from the Rising Edge of $\overline{DAS}$ to the Rising Edge of $\overline{DALO}$ (bus master write)		50			ns
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
54	$\overline{ADR}$	T_{SAH}	$\overline{ADR}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
55	$\overline{ADR}$	T_{SAS}	$\overline{ADR}$ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
56	$\overline{READY}$	T_{ARYD}	Delay from the Falling Edge of ALE to the Falling Edge of $\overline{READY}$ to Insure a Minimum Bus Cycle Time (600nS)	T_{SCT}=100nS			150	ns
57	$\overline{READY}$	T_{SRDS}	Data Setup Time to the Falling Edge of $\overline{READY}$ (bus slave read)		75			ns
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus master)		0			ns
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)	T_{SCT}=100nS	0		35	ns
60	$\overline{READY}$	T_{RSH}	READ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
61	READ	T_{SRS}	READ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
62	$\overline{READY}$	T_{RDYD}	Delay from Falling Edge of $\overline{DAS}$ to Falling Edge of $\overline{READY}$ (bus slave)	T_{SCT}=100ns		200		ns

Figure 5A : TTL Output Load Diagram.
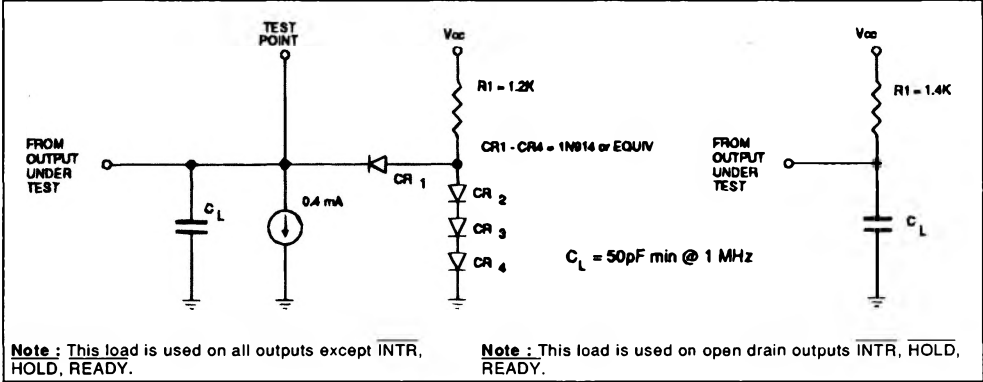
Figure 5AB : Open Drain Output Load Diagram.

Note : This load is used on all outputs except INTR, HOLD, READY.

Note : This load is used on open drain outputs INTR, HOLD, READY.

Figure 6 : MK5027 Serial Link Timing Diagram.

Timing measurements are made at the following voltages, unless otherwise specified :

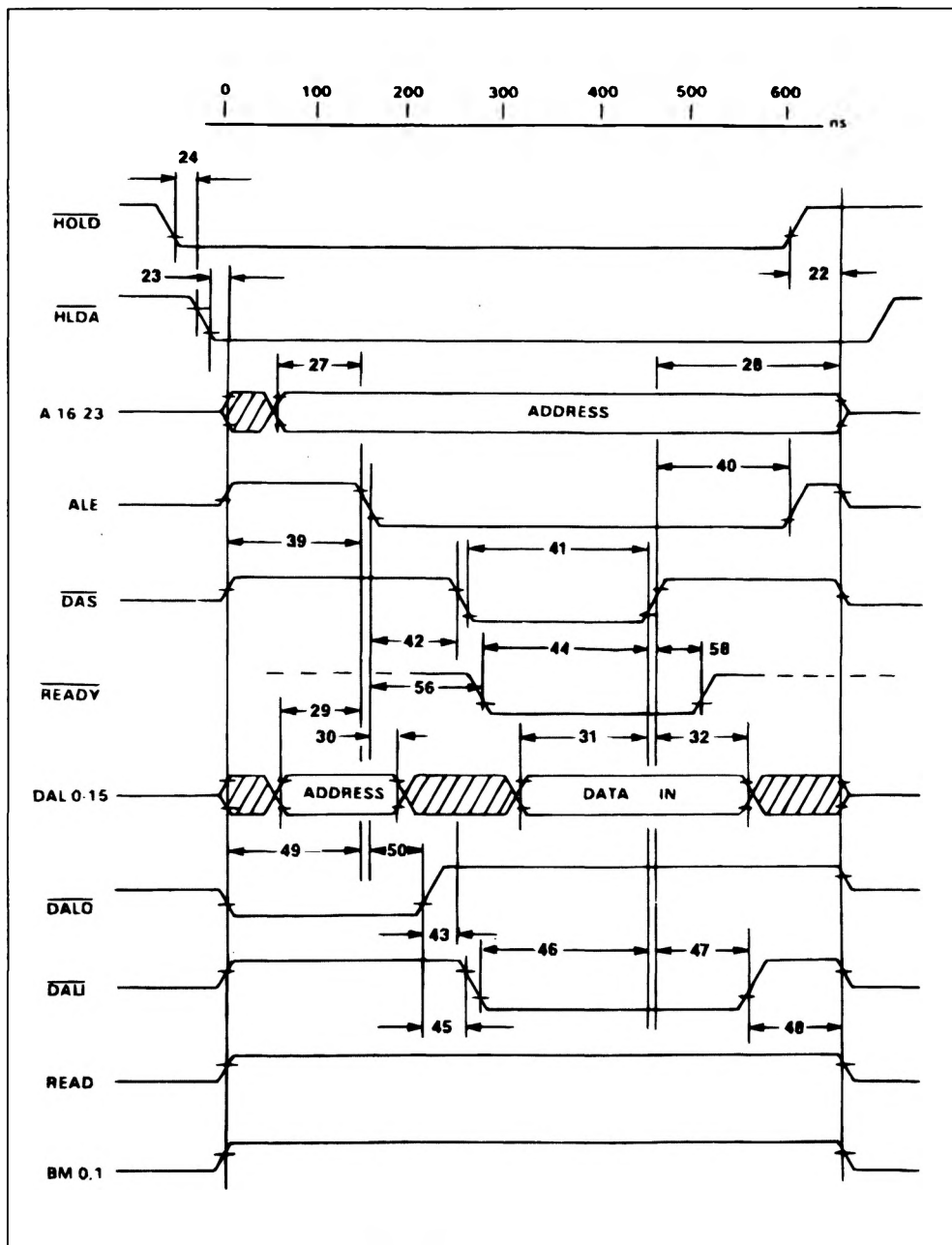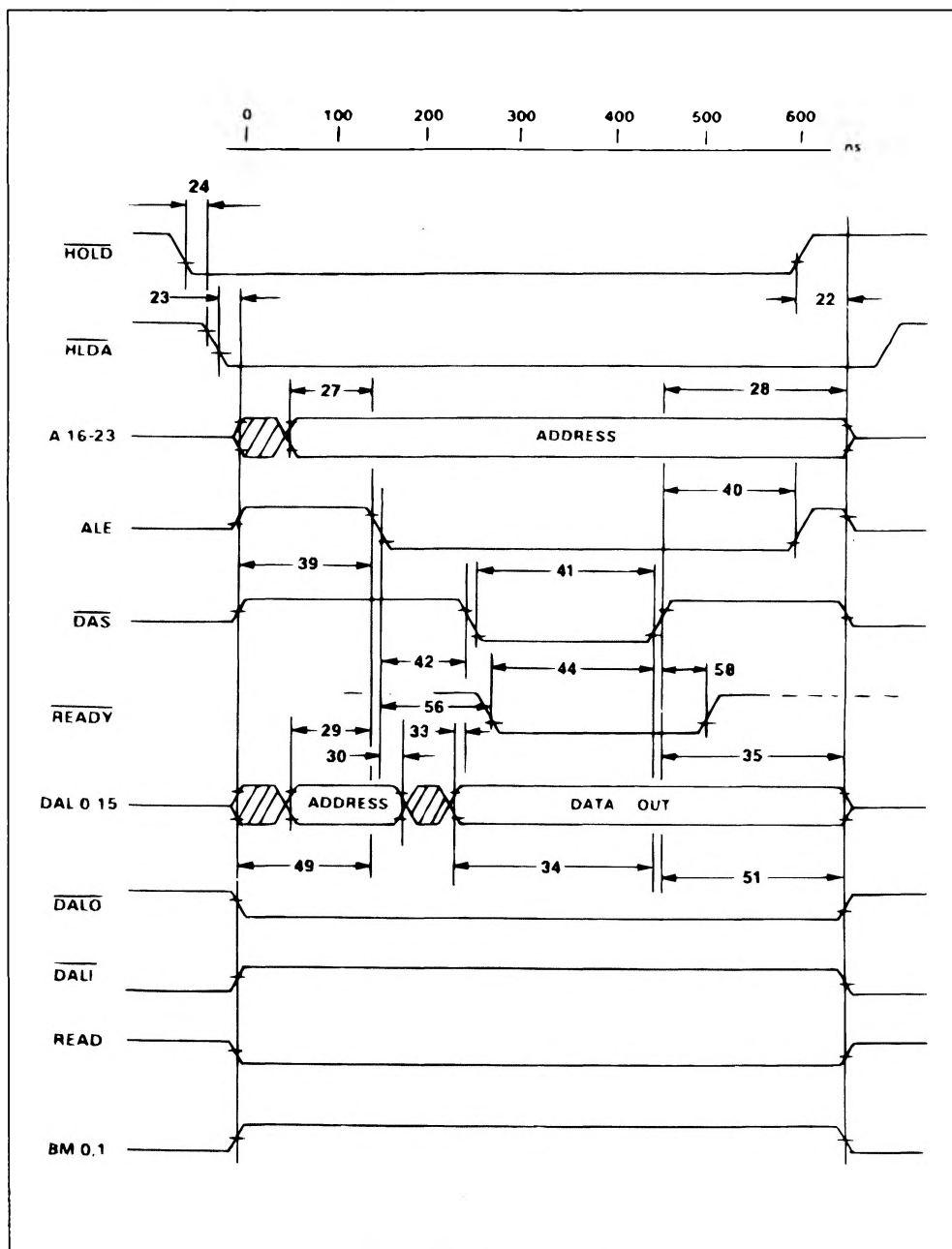|	"1"	"0"
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	10%	90%

SGS-THOMSON
MICROELECTRONICS
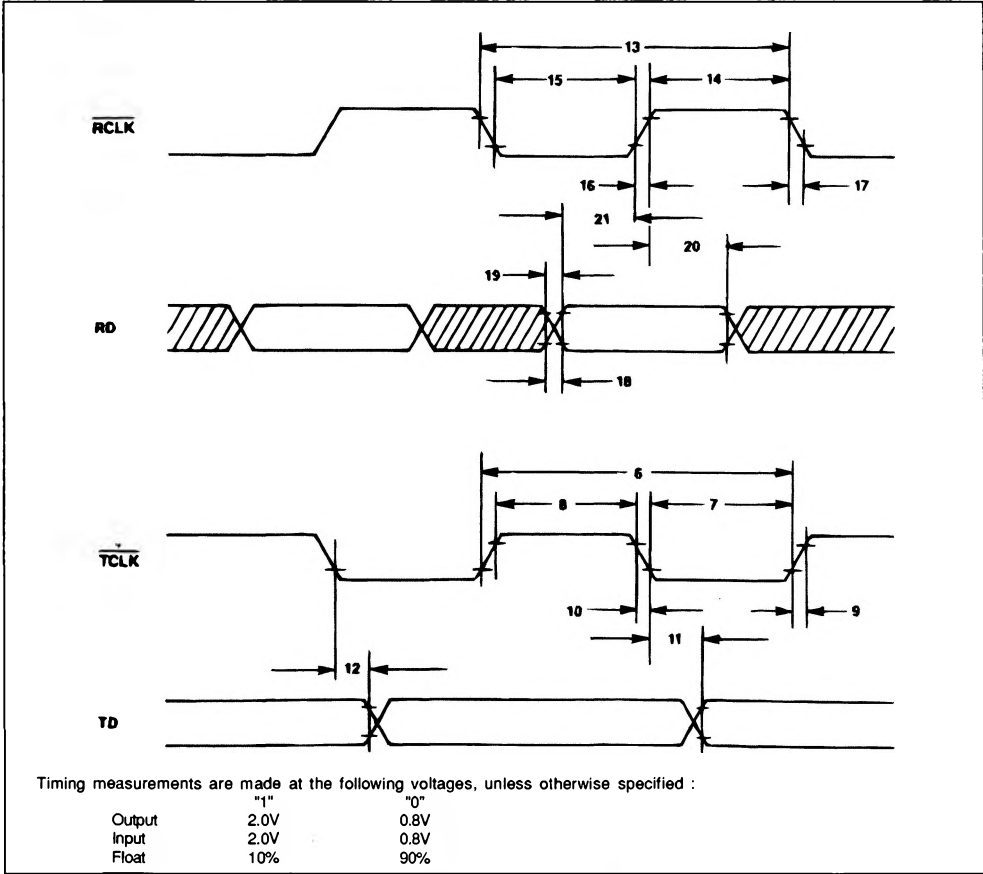
Figure 7 : MK5027 Bus Master Timing Diagram (read).

Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

Figure 8 : MK5027 Bus Master Timing Diagram (write).

Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

SGS-THOMSON
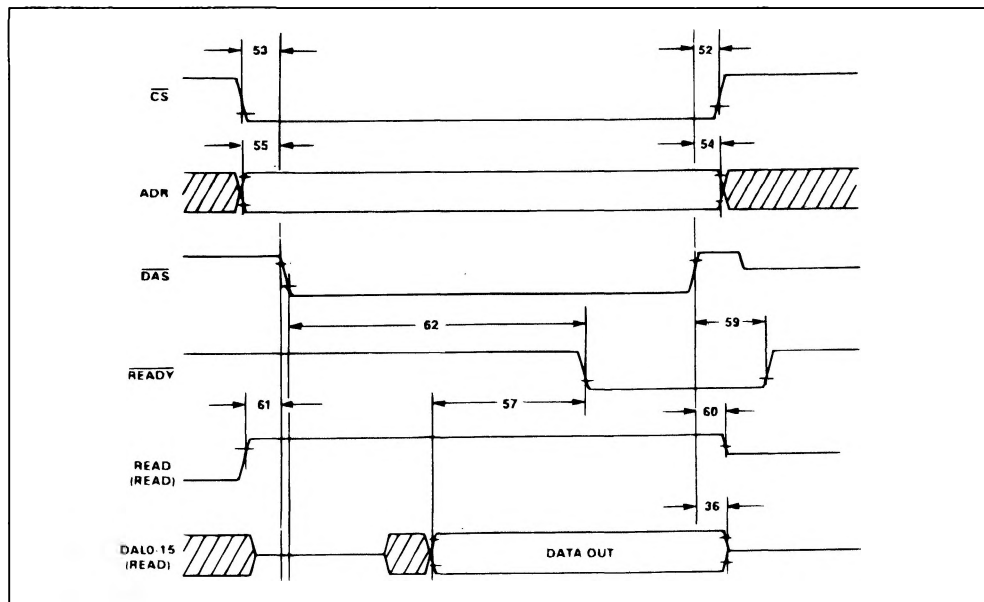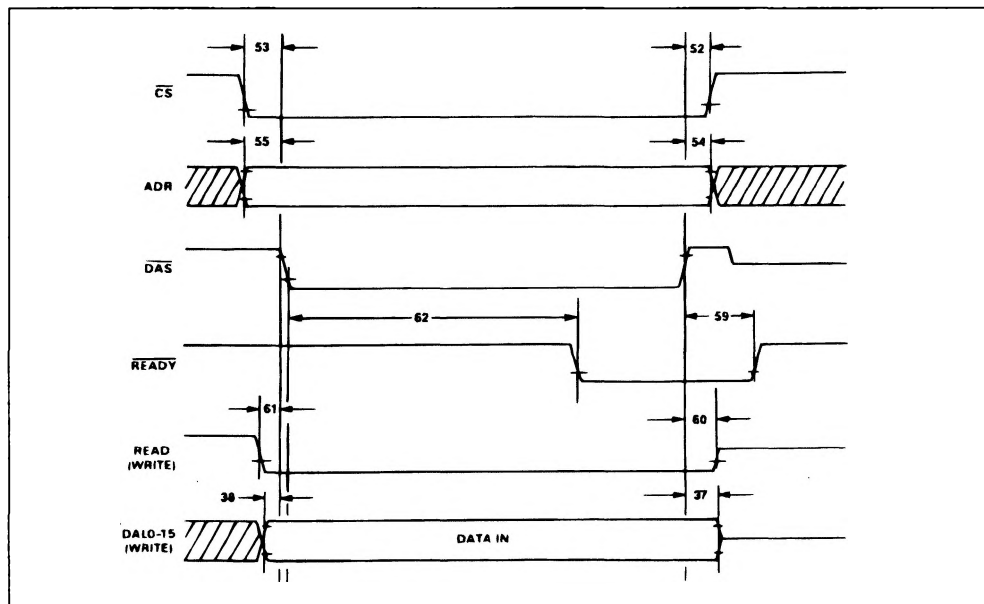**MICROELECTRONICS**

Figure 9 : MK5027 Bus Slave Timing Diagram (read).


Figure 10 : MK5027 Bus Slave Timing Diagram (write).

SGS-THOMSON
MICROELECTRONICS

PACKAGE DESCRIPTION
5027P
SIDE BRAZED CERAMIC

Dim.	Inches		Notes
	Min.	Max.	
A		.175	1
A1	.020		1
A2	.080	.110	
B	.015	.021	2
B1	.038	.057	
C	.008	.012	2
D	2.370	2.430	
D1	.035	.065	
E	.595	.625	
E1	.580	.610	
e1	.090	.110	
eA	.590	.665	
L	.125		
Q	.005		3
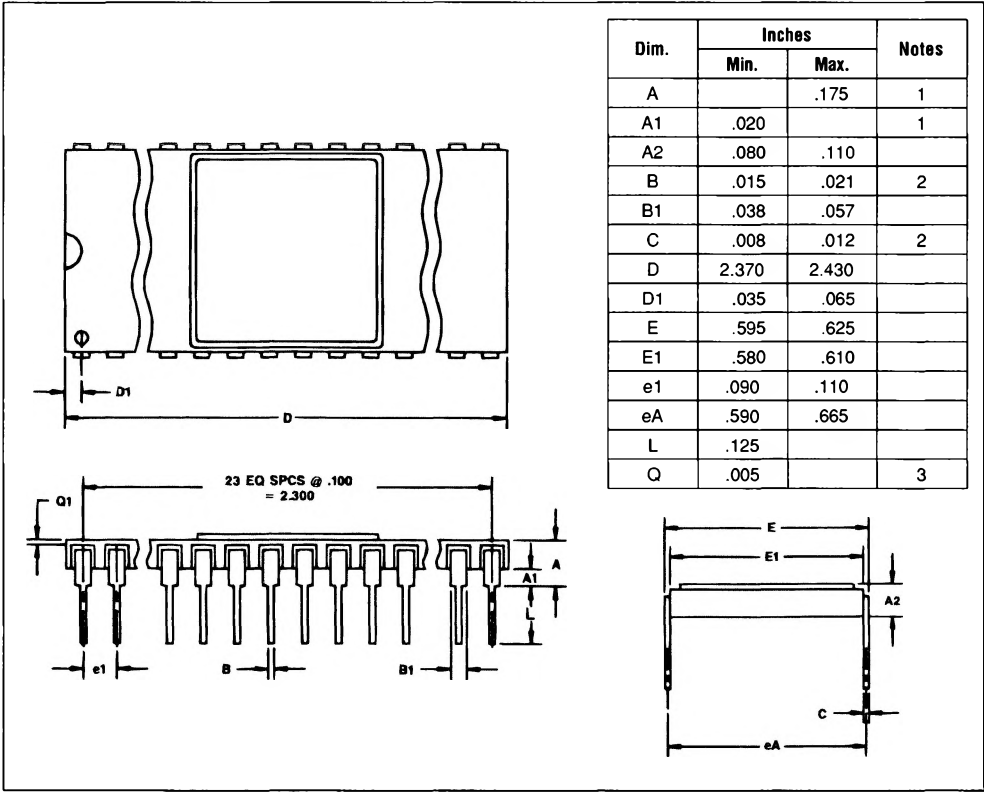
Notes : 1. Package standoff to be measured per JEDEC requirements.
    2. The maximum limit shall be increased by .003 in. when solder lead finish is specified.
    3. Measured from top of ceramic to nearest metallization.

SGS-THOMSON
MICROELECTRONICS

PACKAGE DESCRIPTION
MK5027Q
52 PIN PLCC
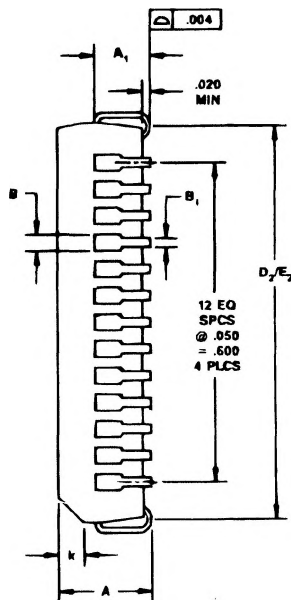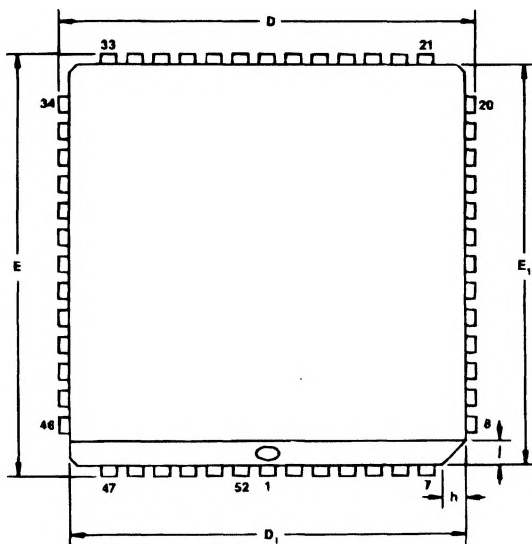
Dim.	Inches		Notes
	Min.	Max.	
A	.165	.185	2
A_1	.090	.120	2
B	.026	.032	2
B_1	.013	.021	2
D	.785	.795	
D_1	.750	.756	
D_2	.690	.730	
E	.785	.795	
E_1	.750	.756	
E_2	.690	.730	
h	.042	.060	
j	.042	.060	
k	.042	.056	

PINOUT :   * = ACTIVE LOW
1   Vss   21 HLDA*   41 ADDRESS 18
2   DAL07   22 CS*   42 ADDRESS 17
3   DAL06   23 ADR   43 ADDRESS 16
4   DAL05   24 READY*   44 DAL15
5   DAL04   25 RESET*   45 DAL14
6   DAL03   26 VSS (GROUND)   46 DAL13
7   DO NOT CONNECT   27 DO NOT CONNECT   47 DAL12
8   DAL02   28 TCLK*   48 DAL11
9   DAL01   29 DTR,RTS*   49 DAL10
10 DAL00   30 RCLK*   50 DAL09
11 READ   31 SYSCLK   51 DAL08
12 INTR*   32 TD   52 VCC
13 DALI*   33 DSR,CTS*
14 DALO*   34 RD
15 DAS*   35 ADDRESS 23
16 BM0*BYTE/BUSREL*   36 DO NOT CONNECT
17 DO NOT CONNECT   37 ADDRESS 22
18 BM1*/BUSAKO   38 ADDRESS 21
19 HOLD*/BURSQ*   39 ADDRESS 20
20 ALE/AS*   40 ADDRESS 19