SGS-THOMSON MICROELECTRONICS

MK48T87(B)

ADDRESS / DATA MULTIPLEX TIMEKEEPER™ RAM

ADVANCE DATA

- DROP-IN REPLACEMENT FOR IBM AT COMPUTER CLOCK/CALENDAR
- PIN COMPATIBLE WITH THE MC146818 A
- TOTALLY NONVOLATILE WITH OVER 10 YEARS OF OPERATION IN THE ABSENCE OF POWER
- SELF-CONTAINED SUBSYSTEM INCLUDES LITHIUM BATTERY, QUARTZ CRYSTAL AND SUPPORT CIRCUITRY
- COUNTS SECONDS, MINUTES, HOURS, DAYS, DAY OF THE WEEK, DATE, MONTH AND YEAR WITH LEAP YEAR COMPENSATION
- BINARY OR BCD REPRESENTATION OF TIME, CALENDAR AND ALARM
- 12 OR 24 HOUR CLOCK WITH AM AND PM IN 12 HOUR MODE
- SELECTABLE BETWEEN MOTOROLA AND INTEL BUS TIMING
- MULTIPLEX BUS FOR PIN EFFICIENCY
- INTERFACED WITH SOFTWARE AS 64 RAM LOCATIONS
  - 14 Bytes Of Clock And Control Registers
  - 50 Bytes Of General Purpose Ram
- PROGRAMMABLE SQUARE WAVE OUTPUT SIGNAL
- BUS COMPATIBLE INTERRUPT SIGNALS (IRQ)
- THREE INTERRUPTS ARE SEPARATELY SOFTWARE-MASKABLE AND TESTABLE
  - Time-of-day Alarm Once/second To Once/day
  - Periodic Rates From 122 us To 500 ms
  - End Of Clock Update Cycle

B
DIP-24
(Plastic with battery top Hat)

PIN CONNECTIONS

PIN NAMES

A/D0 - A/D7	ADDRESS / DATA
MOT	BUS TYPE SELECTION
E	CHIP SELECT
AS	ADDRESS STROBE
W	READ / WRITE
SQW	SQUARE WAVE OUT
IRQ	INTERRUPT REQUEST
RESET	RESET
DS	DATA STROBE
V_{CC}	+5 VOLTS
GND	GROUND
NF*	NO FUNCTION

* This pin serves no function and may be connected to other signals without affecting device operation. The electrical characteristics are the same as the other inputs pins.

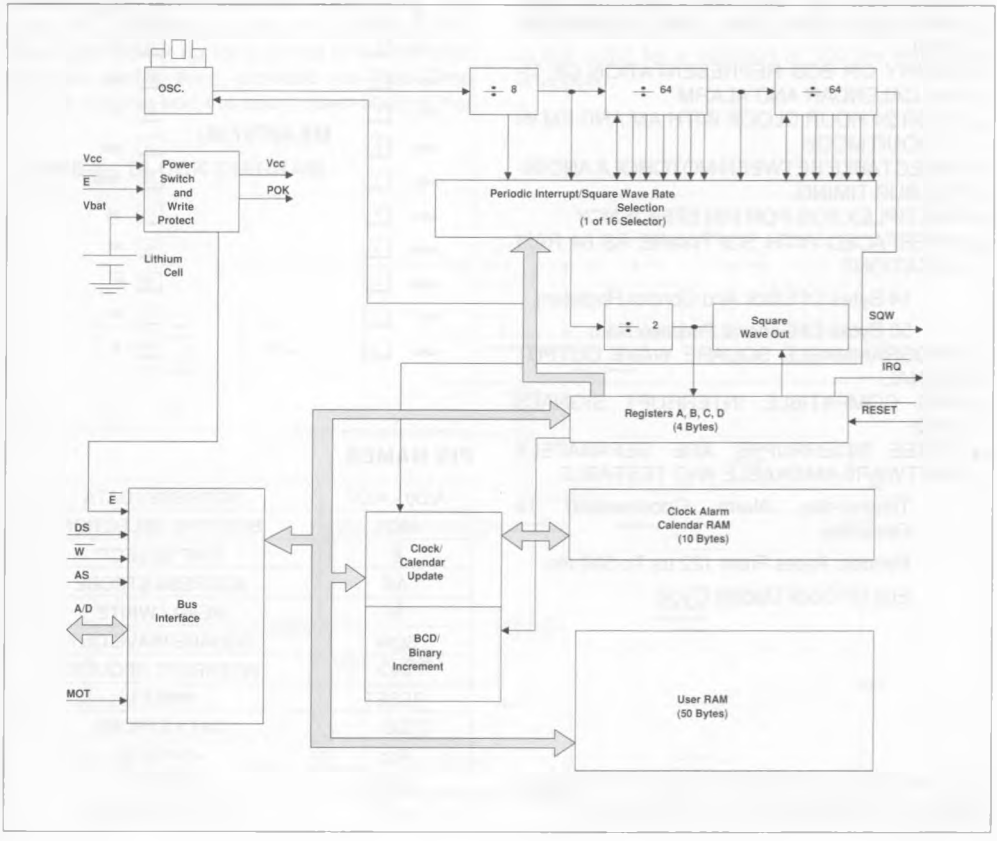
DESCRIPTION

The MK48T87 RealTime Clock and RAM is designed to be a compatable replacement for the MC146818. A lithium energy source, a quartz crystal and write-protection circuitry are contained within a 24-pin dual in-line package. The MK48T87 is, therefore, a complete subsystem replacing as many as 16 components in a typical application. The functions available to the user include a nonvolatile time-of-day clock, an alarm, a one-hundred-year calendar, programmable interrupt, square wave generator, and 50 bytes of nonvolatile static RAM. The Real Time Clock/RAM is unique in that the time-of-day and memory are maintained even in the absence of power.

Automatic deselection of the device provides insurance that data integrity is not compromised should V_{CC} fall below specified (V_{PFD}) levels. The automatic deselection of the device remains in effect upon power up for a period of 100ms after V_{CC} rises above V_{PFD}, provided the Real Time Clock is running and the count down chain is not in reset, allowing sufficient time for V_{CC} to stabilize and giving the system clock a wake up period so that a valid system reset can be established.

The block diagram in Figure 1 shows the pin connection with the major internal functions of MK48T87 (Real Time Clock/RAM). The following paragraphs describe the function of each pin.

FIGURE 1 . BLOCK DIAGRAM



SIGNAL DESCRIPTIONS

GND, V_{CC} - D.C. power is provided to the device on these pins. V_{CC} is the +5 volt input. When V_{CC} is applied and is above V_{PFD}, the device is fully accessible and the data can be written and read. When V_{CC} is below V_{PFD}, reads and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage. As V_{CC} falls below V_{SO}, the RAM and timekeeper are switched over to an internal Lithium energy source. The timekeeping function maintains an accuracy of ± 1 minute per month at 25 ° C regardless of the voltage input on the V_{CC} pin.

MOT (Mode Select) - The MOT pin offers the flexibility to choose between two bus types. When connected to V_{CC}, Motorola bus timing is selected. When connected to GND or left disconnected, Intel bus timing is selected. The pin has an internal pull-down resistance of approximately 20 K .

SQW (Square Wave Output) - The SQW pin can output a signal from one of 13 taps provided by the 15 internal divider stages of the Real Time Clock. The frequency of the SQW pin may be changed by programming Register A. As shown in Table 1, the SQW signal may be turned on and off using the SQWE bit in Register B. The SQW signal is not available when V_{CC} is less than V_{PFD}.

TABLE 1 . PERIODIC INTERRUPT RATE AND SQUARE WAVE FREQUENCY

SELECT BITS REGISTER A				t_{PI} PERIODIC INTERRUPT RATE	SQW OUTPUT FREQUENCY
RS3	RS2	RS1	RS0		
0	0	0	0	None	None
0	0	0	1	3.90625 ms	256 Hz
0	0	1	0	7.8125 ms	128 Hz
0	0	1	1	122.070 µs	8.192 KHz
0	1	0	0	244.141 µs	4.096 KHz
0	1	0	1	488.281 µs	2.048 KHz
0	1	1	0	976.5625 µs	1.024 KHz
0	1	1	1	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz

AD0-AD7 (Multiplexed Bi-Directional Address/Data Bus) - Multiplexing the bus reduces the device pin count because address information and data information time share the same signal paths. The addresses are presented during the first portion of the bus cycle and the same pins and signal paths are used for data transfer during the second portion of the cycle. Address/data multiplexing does not slow the access time of the MK48T87 since the bus change from address to data occurs during the internal RAM access time. Addresses must be valid prior to the falling edge of AS/ALE, at which time the MK48T87 latches the address from ADO toAD5. Valid write data must be present and held stable during the latter portion of the DS or RD pulses. The read cycle is terminated and the bus returns to a high impedance state as DS transitions low in the case of Motorola timing or as RD transitions high in the case of Intel timing.

AS (Address Strobe Input) - A positive going address strobe pulse serves to demultiplex the bus. The falling edge of AS/ALE causes the address to be latched within the MK48T87.

DS (Data Strobe or Read Input) - The DS/RD pin has two modes of operation depending on the level of the MOT pin. When the MOT pin is connected to V_{CC}, Motorola bus timing is selected. In this mode DS is a positive pulse during the latter portion of the bus cycle and is called Data Strobe. During read cycles, DS signifies the time that the MK48T87 is to drive the bi-directional bus. In write cycles the trailing edge of DS causes the MK48T87 to latch the written data. When the MOT pin is connected to GND, Intel bus timing is selected. In this mode the DS pin is called Read (RD). RD identifies the time period when the MK48T87 drives the bus with read data. The RD signal is the same definition as the Output Enable ($\overline{G}$) signal on a typical memory.

W (Read/Write Input) - The $\overline{W}$ pin also has two modes of operation. When the MOT pin is connected to V_{CC} for Motorola timing, $\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a high level on $\overline{W}$ while DS is high. A write cycle is indicated when $\overline{W}$ is low during DS. When the MOT pin is connected to GND for Intel timing, the $\overline{W}$ signal is an active low signal called WR. In this mode the $\overline{W}$ pin has the same meaning as the Write Enable signal ($\overline{W}$) on generic RAMs.

E (Chip Select Input) - The Chip Select signal ($\overline{E}$) must be asserted low for a bus cycle in which the MK48T87 is to be accessed. $\overline{E}$ must be kept in the active state during DS and AS for Motorola timing and during RD and $\overline{W}$ for Intel timing. Bus cycles which take place without asserting $\overline{E}$ will latch addresses but no access will occur. When V_{CC} is below V_{PFD}, the MK48T87 internally inhibits access cycles by internally disabling the $\overline{E}$ input. This action protects both the Real Time Clock data and RAM data during power outages.

IRQ (Interrupt Request Output) - The $\overline{IRQ}$ pin is an active low output of the MK48T87 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains low as long as the status bit causing the interrupt is present and the corresponding interrupt- enable bit is set. To clear the $\overline{IRQ}$ pin the processor program normally reads the C register. The $\overline{RESET}$ pin also clears pending interrupts. When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high impedance state. Multiple interrupt devices may be connected to an $\overline{IRQ}$ bus. The $\overline{IRQ}$ bus is an open drain output and requires an external pull-up resistor.

RESET (Reset Input) - The $\overline{RESET}$ pin has no effect on the clock, calendar, or RAM. On power-up the $\overline{RESET}$ pin may be held low for a time in order to allow the power supply to stabilize. The amount of time that $\overline{RESET}$ is held low is dependent on the application. However, if $\overline{RESET}$ is used on power up, the time $\overline{RESET}$ is low should exceed 200 ms to make sure that the internal timer which controls the MK48T87 on power-up has timed out. When $\overline{RESET}$ is low and V_{CC} is above V_{PFD}, the following occurs:

A. Periodic Interrupt Enable (PIE) bit is cleared to zero.

B. Alarm Interrupt Enable (AIE) bit is cleared to zero.

C. Update Ended Interrupt Flag (UF) bit is cleared to zero.

D. Interrupt Request Status Flag (IRQF) bit is cleared to zero.

E. Periodic Interrupt Flag (PF) bit is cleared to zero.

F. The device is not accessible until $\overline{RESET}$ is returned high.

G. Alarm Interrupt Flag (AF) bit is cleared to zero.

H. $\overline{IRQ}$ pin is in the high impedance state.

I. Square Wave Output Enable (SQWE) bit is cleared to zero.

J. Updated Ended Interrupt Is Cleared To Zero.

In a typical application $\overline{RESET}$ may be connected to Vcc. This connection will allow the MK48T87 to go in and out of power fail without affecting any of the control registers.

ADDRESS MAP

The Address Map of the MK48T87 is shown in Figure 2. The address map consists of 50 bytes of user RAM, 10 bytes of RAM which contain the RTC time, calendar and alarm data, and 4 bytes which are used for control and status. All 64 bytes can be directly written or read except for the following:

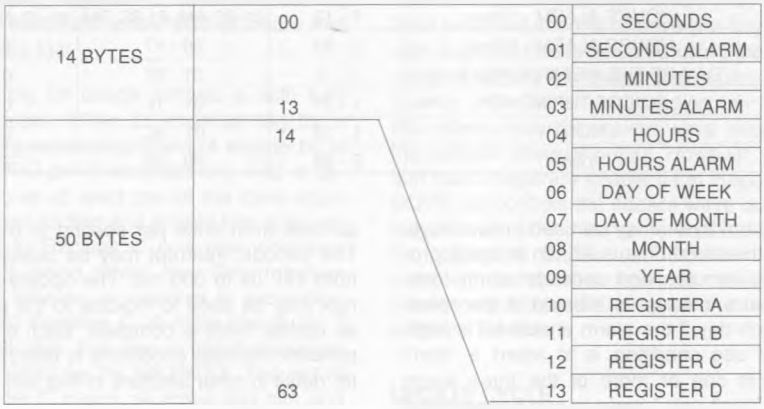
1. Registers C and D are read-only.

2. Bit 7 of Register A is read-only.

3. The high order bit of the seconds byte is read-only.

The contents of four control registers (A,B,C,D) are described in the "Register" section.

FIGURE 2 . ADDRESS MAP



TIME, CALENDAR AND ALARM LOCATIONS

The time and calendar information is obtained by reading the appropriate memory bytes. The time, calendar and alarm are set or initialized by writing the appropriate RAM bytes. The contents of the ten time, calendar and alarm bytes may be either Binary or Binary-Coded (BCD) format. Before writing the internal time, calendar, and alarm registers, the SET bit in Register B should be written to a Logic one to prevent updates from occuring while access is being attempted. In addition to writing the ten time, calendar and alarm registers in a selected format (Binary or BCD), the data mode bit (DM) of Register B must be set to the appropriate logic level. All ten time, calendar and alarm bytes must be used the same data mode. The set bit in Register B should be cleared after the data mode bit has been written to allow the Real Time Clock to update the time and calendar bytes. Once initialized, the Real Time Clock makes all updates in the selected mode. The data mode cannot be changed without reinitializing the ten data bytes. Table 2 shows the Binary and BCD formats of the ten time, calendar and alarm locations. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected, the high order bit of the hours byte represents PM when it is a logic one. The time, calendar and alarm bytes are always accessible because they are double buffered. Once per second the ten bytes are advanced by one second and checked for an alarm condition. If a read of the time and calendar data occurs during an update, a problem exits that seconds, minutes, hours, etc., may not correlate. The probability of reading incorrect time and calendar data is low. Several methods of avoiding any possible incorrect time and calendar reads are covered later in this text.

TABLE 2 . CALANDAR AND ALARM DATA MODES

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE	
			BINARY DATA MODE	BCD DATA MODE
0	SECONDS	00 - 59	00 - 3B	00 - 59
1	SECONDS ALARM	00 - 59	00 - 3B	00 - 59
2	MINUTES	00 - 59	00 - 3B	00 - 59
3	MINUTES ALARM	00 - 59	00 - 3B	00 - 59
4	HOURS - 12hrs MODE	1 - 12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS - 24hrs MODE	0 - 23	00 - 17	00 - 23
5	HOURS ALARM - 12hrs	1 - 12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS ALARM - 24hrs	0 - 23	00 - 17	00 - 23
6	DAY OF THE WEEK (SUNDAY=1)	1 - 7	01 - 07	01 - 07
7	DAY OF THE MONTH	1 - 31	01 - 1F	01 - 31
8	MONTH	1 - 12	01 - 0C	01 - 12
9	YEAR	0 - 99	00 - 63	00 - 99

The three alarm bytes may be used in two ways. First, when the alarm time is written in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second use condition is to insert a "don't care" state in one or more of the three alarm bytes. The "don't care" code is any hexadecimal value from C0 to FF. The two most significant bits of each byte set the "don't care" condition when at Logic 1. An alarm will be generated each hour when the "don't care" bits are set in the hours byte. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minute alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

NONVOLATILE RAM

The 50 general purpose nonvolatile RAM bytes are not dedicated to any special function within the MK48T87. They can be used by the processor program as nonvolatile memory and are fully available during the update cycle.

INTERRUPTS

The RTC plus RAM includes three separate, fully automatic sources of interrupt for a processor. The alarm interrupt may be programmed to occur at rates from once per second to once per day. The periodic interrupt may be selected for rates from 122 us to 500 ms. The update-ended interrupt may be used to indicate to the program that an update cycle is complete. Each of these independent interrupt conditions is described in greater detail in other sections of this text.

The processor program can select which interrupts, if any, are going to be used. Three bits in Register B enable the interrupts. Writing a Logic 1 to an interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in an interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted from that interrupt condition. If an interrupt flag is already set when an interrupt is enabled, $\overline{IRQ}$ is immediately set at an active level although the interrupt initiating the event may have occurred much earlier. As a result, there are cases where the program should clear such earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs, the relating flag bit is set to Logic 1 in Register C. These flag bits are set independent of the state of the corresponding enable bit in Register B. The flag bit can be used in a polling mode without enabling the corresponding enable bits. The interrupt flag bit is a status bit which software can interrogate as necessary.

When a flag is set, an indication is given to software that an interrupt event has occurred since the flag bit was last read; however, care should be taken when using the flag bits as they are cleared each time Register C is read. Double latching is included with Register C so that bits which are set remain stable throughout the read cycle. All bits which are set (high) are cleared when read and new interrupts which are pending during the read cycle are held until after the cycle is completed. One, two or three bits may be set when reading Register C. Each utilized flag bit should be examined when read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt flag bit is set and the corresponding interrupt enable bit is also set, the $\overline{IRQ}$ pin is asserted low. $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The $\overline{IRQF}$ bit in Register C is a one whenever the $\overline{IRQ}$ pin is being driven low. Determination that the RTC initiated an interrupt is accomplished by reading Register C. A logic one in Bit 7 (IRQF bit) indicates that one or more interrupts have been initiated by the MK48T87. The act of reading Register C clears all active flag bits and the IRQF bit.

OSCILLATOR CONTROL BITS

When the MK48T87 is shipped from the factory, the internal oscillator is turned off. This feature prevents the lithium energy cell from being used until it is installed in system. A pattern of 010 in bits 4 through 6 of Register A will turn the oscillator on and enable the countdown chain. A pattern of 11X will turn the oscillator on, but holds the countdown chain of the oscillator in reset. All other combinations of bits 4 through 6 keep the oscillator off.

SQUARE WAVE OUTPUT SELECTION

Thirteen of the 15 divider taps are made available to a 1-of-15 selector, as shown in the block diagram of Figure 1. The first purpose of selecting a divider tap is to generate a square wave output signal on the SQW pin. The RS0-RS3 bits in Register A establish the square wave output frequency. These frequencies are listed in Table 1. The SQW frequency selection shares its 1-of-15 selector with the periodic interrupt generator. Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square wave enable bit (SQWE).

PERIODIC INTERRUPT SELECTION

The periodic interrupt will cause the IRQ pin to go to an active state from once every 500 ms to once every 122 us. This function is separate from the alarm interrupt which may be output from once per second to once per day. The periodic interrupt rate is selected using the same Register A bits which select the square wave frequency (see Table 1). Changing the Register A bits affects both the square wave frequency and the periodic interrupt output. However, each function has a separate enable bit in Register B. The SQWE bit controls the square wave output. Similarly, the periodic interrupt is enabled by the PIE bit in Register B. The periodic interrupt can be used with software counters to measure inputs, create output intervals, or await the next needed software function.

UPDATE CYCLE

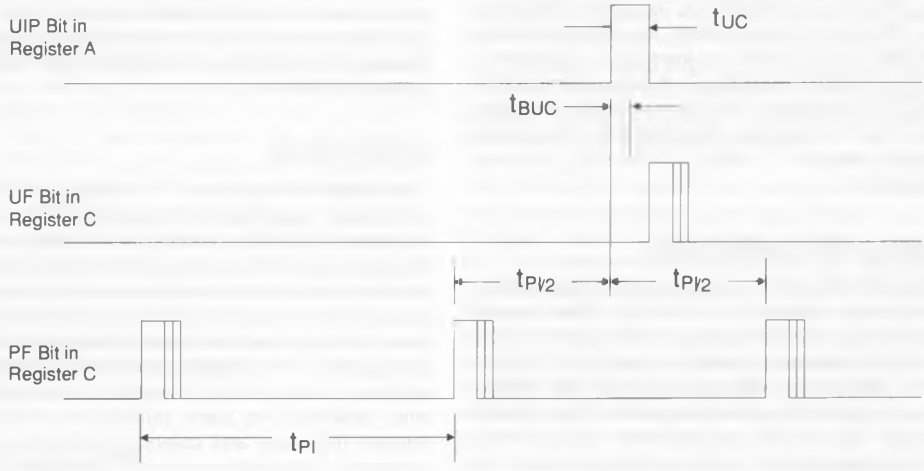
The MK48T87 executes an update cycle once per second regardless of the set bit in Register B. When the SET bit in Register B is set to one, the user copy of the double buffered time, calendar and alarm bytes if frozen and will not update as the time increments. However, the time countdown chain continues to update the internal copy of the buffer. This feature allows time to maintain accuracy indep endent of reading or writing the time, calendar, and alarm buffers and also guarantees that time and calendar information are consistent. The update cycle also compares each alarm byte with the corresponding time byte and issues and alarm if a match or if a "don't care" code is present in all three positions.

There are three methods which can be employed to handle access of the Real Time Clock which avoids any possibility of accessing inconsistent time and calendar data. The first method uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 998 ms are available to read valid time and date information. If this interrupt is used, the IRQF bit in Register C should be cleared before leaving the interrupt routine.

A second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress. The UIP bit will pulse once per second. After the UIP bit goes high, the update transfer occurs 244 us later. If a low is read on the UIP bit, the user has at least 244 us before the time/calendar data will be changed. Therefore, the user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 us.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set high between the setting of the PF bit in Register C (see Figure 3). Periodic interrupts that occur at a rate of greater than t_{BUC} allow valid time and date information to be reached at each occurrence of the periodic interrupt. The reads should be complete within ($T_{PI/2}$+t_{BUC}) to insure that data is not read during the update cycle.

FIGURE 3 . UPDATE ENDED AND PERIODIC INTERRUPT RELATIONSHIP



t_{PI} = Periodic Interrupt Time Interval Per Table 1.

t_{BUC} = Delay Time Before Update Cycle = 244 µs.

t_{UC} = 2 ms.

REGISTERS:

REGISTER A

MSB LSB

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The Update in Progress (UIP) bit is a status flag that can be monitored. When the UIP bit is one. the update transfer will soon occur. The UIP is a zero, the update transfer will not occur for at least 244 us. The time, calendar, and alarm information in RAM is fully available for access when the UIP bit is zero. The UIP bit is read only and is not affected by $\overline{\text{RESET}}$. Writing the SET bit in Register B to a "1" inhibits any update transfer and clears the UIP status bit.

DVO, DV1, DV2

These three bits are used to turn the oscillator on or off and to reset the countdown chain. A pattern of 010 is the only combination of bits which will turn the oscillator on and allow the RTC to keep time. A pattern of 11X will enable the oscillator but holds the countdown chain in reset. The next update will occur at 1second after a pattern of 010 is written to DV0, DV1 and DV2.

RS3, RS2, RS1, RS0

These four rate-selection bits select one of the 13 taps on the 15-stage divider or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The user may do one of the following:

1. Enable the interrupt with the PIE bit;

2. Enable the SQW output pin with the SQWE bit;

3. Enable both at the same time and the same rate; or

4. Enable neither.

REGISTER B

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET

When the SET bit is a zero, the update transfer functions normally by advancing the counts once per second. When the SET bit is written to a one, any update transfer is inhibited and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. Read cycles can be executed in a similar manner. SET is a read/write bit which is not modified by RESET or internal functions of the MK48T87.

PIE

The periodic interrupt enable PIE bit is a read/write bit which allows the Periodic Interrupt Flag (PF) bit in Register C to cause the IRQ pin to be driven low. When the PIE bit is set to one, periodic interrupts are generated by driving the IRQ pin low at a rate specified by the RS3 through RS0 bits of Register A. A zero in the PIE bit blocks the IRQ output from being driven by a periodic interrupt, but the Periodic Flag (PF) bit is still set at the periodic rate. PIE is not modified by any internal MK48T87 functions, but is cleared to zero on RESET.

AIE

The Alarm Interrupt Enable (AIE) bit is a read/write bit which when set to a one permits the Alarm Flag (AF) bit in register C to assert IRQ. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes including a "don't care" alarm code of binary 11XXXXXX. When the AIE bit is set to zero, the AF bit does not initiate the IRQ signal. The RESET pin clears AIE to zero. The internal functions of the MK48T87 do not affect the AIE bit.

UIE

The Update Ended Interrupt Enable (UIE) bit is a read/write bit which enables the Update End Flag (UF) bit in Register C to assert IRQ. The RESET pin going low or the SET bit going high clears the UIE bit.

SQWE

When the Square Wave Enable (SQWE) bit is set to a one, a square wave signal at the frequency set by the rate-selection bits RS3 through RS0 is driven out on the SQW pin. When the SQWE bit is set to zero, the SQW pin is held low; the state of SQWE is cleared by the RESET pin. SQWE is a read/write bit.

DM

The Data Mode (DM) bit indicates whether time and calendar information are in binary or BCD format. The DM bit is set by the program to the appropriate format and can be read as required. This bit is not modified by internal functions or RESET. A one in DM signifies binary data and a zero in DM specifies Binary Coded Decimal (BCD) data.

24/12

The 24/12 control bit establishes the format of the hours byte. A one indicates the 24-hour mode and a zero indicates the 12-hour mode. This bit is a read/write and is not affected by internal functions or RESET.

DSE

The Daylight Savings Enable (DSE) bit is a read/write bit which enables two special updates when DSE is set to one. On the first Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a zero. This bit is not affected by internal functions or RESET.

REGISTER C

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The Interrupt Request Flag (IRQF) bit is set to a one when one or more of the following are true:

PF=PIE=1

AF=AIE=1

UF=UIE=1

i.e.,IRQF=PF•PIE+AF•AIE+UF•UIE

Any time the IRQF bit is a one the $\overline{IRQ}$ pin is driven low. All flag bits are cleared after Register C is read by the program or when the $\overline{RESET}$ pin is low.

PF

The Periodic Interrupt Flag (PF) is a read-only bit which is set to a one when an edge is detected on the selected tap of the divider chain. The RS3 through RS0 bits establish the periodic rate. PF is set to a one independent of the state of the PIE bit. When both PF and PIE are one, the $\overline{IRQ}$ signal is active and will set the IRQF bit. The PF bit is cleared by a $\overline{RESET}$ or a software read of Register C.

AF

A one in the AF (Alarm Interrupt Flag) bit indicates that the current time has matched the alarm time. If the AIE bit is also a one, the $\overline{IRQ}$ pin will go low and a one will appear in the IRQF bit. A $\overline{RESET}$ or a read of Register C will clear AF.

UF

The Update Ended Interrupt Flag (UF) bit is set after each update cycle. When the UIE bit is set to one, the one in the UF bit causes the IRQF bit to be a one which will assert the $\overline{IRQ}$ pin. UF is cleared by reading Register C or a $\overline{RESET}$.

BIT 0 THROUGH BIT 3

These are unused bits of the status Register C. These bits always read zero and cannot be written.

REGISTER D

MSB							LSB
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRT	0	0	0	0	0	0	0

VRT

The Valid RAM and Time (VRT) bit is set to the one state by SGS-THOMSON prior to shipment. This bit is not writable and should always be a one when read. If a zero is ever present, an exhausted internal lithium energy source is indicated and both the contents of the RTC data and RAM data are questionable. This bit is unaffected by $\overline{RESET}$.

BIT 6 THROUGH BIT 0

The remaining bits of Register D are not usable. They cannot be written and when read, they will always read zero.

ABSOLUTE MAXIMUM RATING*

PARAMETER	VALUE	UNIT
Voltage On Any Pin Relative To GND	-0.3 to +7.0	V
Ambient Operating (V_{CC} Off, Oscilator Off) Temperature	0 to +70	°C
Ambient Storage (V_{CC} Off, Oscilator Off) Temperature	-40 to +85	°C
Total Device Power Dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanrnt damage to the device. This is a stress rating only and functional operation of the device at these or any conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMENDED DC OPERATIONING CONDITIONS (0°C ≤ TA ≤ 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.5	V	
GND	Supply Voltage	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.3	V	

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≤ 70°C) ($V_{CC(MAX)} \leq V_{CC} \leq V_{CC(MIN)}$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		15	mA	
I_{mot}	Input Current	-1.0	500	µA	
I_{IL}	Input Leakage Current	-1	+1	µA	
I_{OL}	Output Leakage Current	-5	+5	µA	
V_{OH}	Output Logic "1" Voltage (I_{OUT}=1.0 mA)	2.4		V	

CAPACITANCE (TA = 25°C)

SYMBOL	PARAMETER	MIN	MAX	NOTES
C_L	Capacitance on All Pins (Except DQ)	5.0	pF	
C_{DQ}	Capacitance on DQ Pins	7.0	pF	

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C, V_{CC} = 4.5V to 5.5 V)

		SYMBOL	MIN	MAX	UNITS	NOTES
1	Cycle Time	t_{CYC}	953	D.C.	ns	
2	Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ High	PW_{EL}	300		ns	
3	Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ Low	PW_{EH}	325		ns	
4	Input Rise and Fall Time	t_R, t_F		30	ns	
8	R/$\overline{W}$ Hold Time	t_{RWH}	10		ns	
13	R/$\overline{W}$ Set-up Time Before DS/E	t_{RWS}	80		ns	
14	Chip Select Set-up Time Before DS, $\overline{WR}$ or $\overline{RD}$	t_{CS}	25		ns	
15	Chip Select Hold Time	t_{CH}	0		ns	
18	Read Data Hold Time	t_{DHR}	10	100	ns	
21	Write Data Hold Time	t_{DWH}	0		ns	
24	Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50		ns	
25	Muxed Address Hold Time	t_{AHL}	20		ns	
26	Delay Time DS/E to AS/ALE Fall	t_{ASD}	50		ns	
27	Pulse Width AS/ALE High	PW_{ASH}	135		ns	
28	Delay Time, AS/ALE to DS/E Rise	t_{ASED}	60		ns	
30	Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	20	240	ns	
31	Data Set-up Time	t_{DSW}	200		ns	
32	Reset Pulse Width	t_{RWL}	5		µs	
33	$\overline{IRQ}$ Release from DS	t_{IRDS}		2	µs	
34	$\overline{IRQ}$ Release from $\overline{RESET}$	t_{IRR}		2	µs	

FIGURE 4 . BUS TIMING FOR MOTOROLA INTERFACE

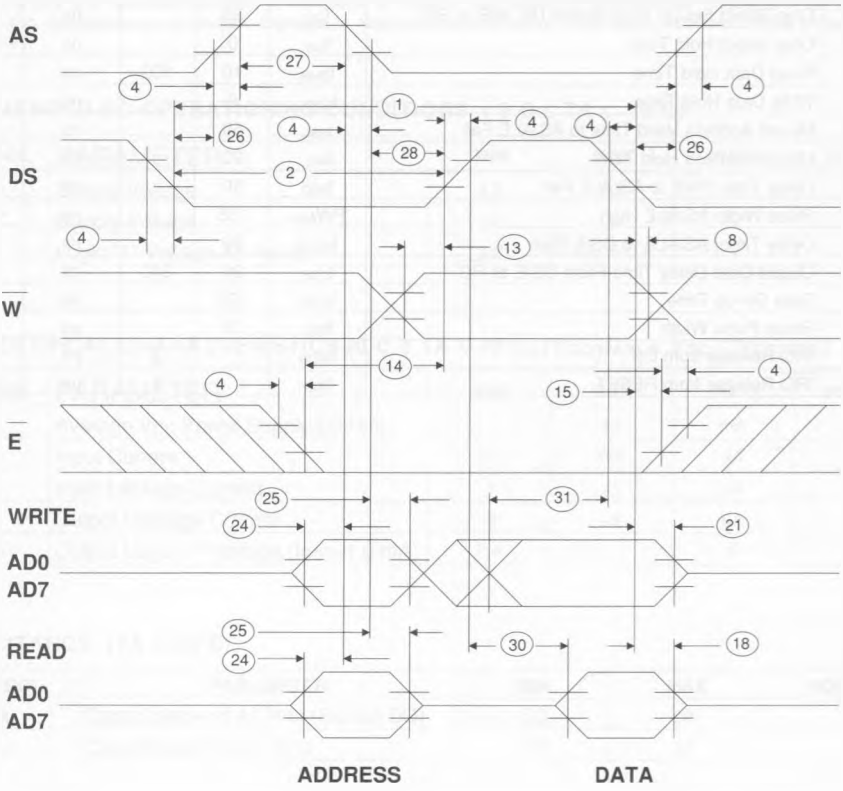


FIGURE 5 . BUS TIMING FOR INTEL INTERFACE READ CYCLE

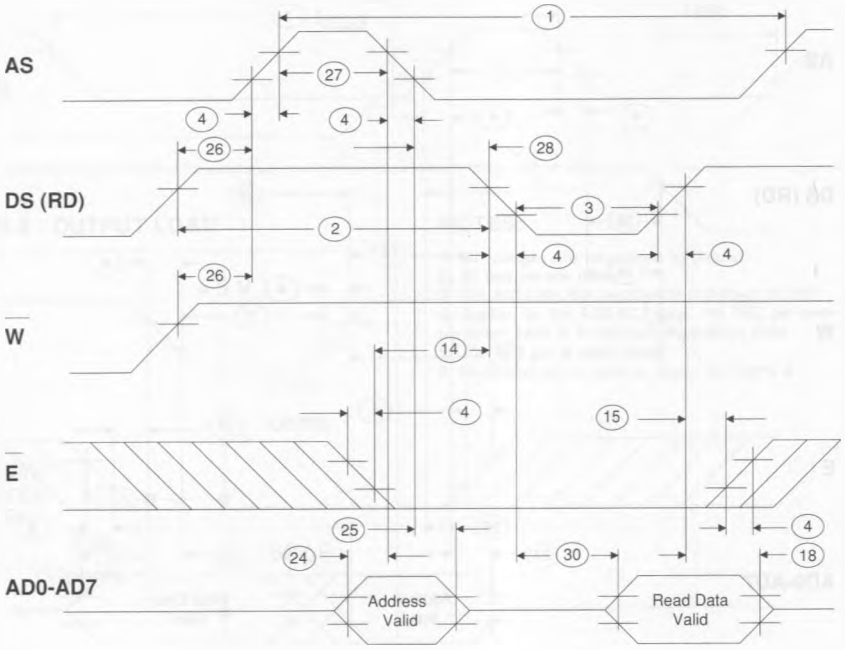


FIGURE 6 . BUS TIMING FOR INTEL INTERFACE WRITE CYCLE

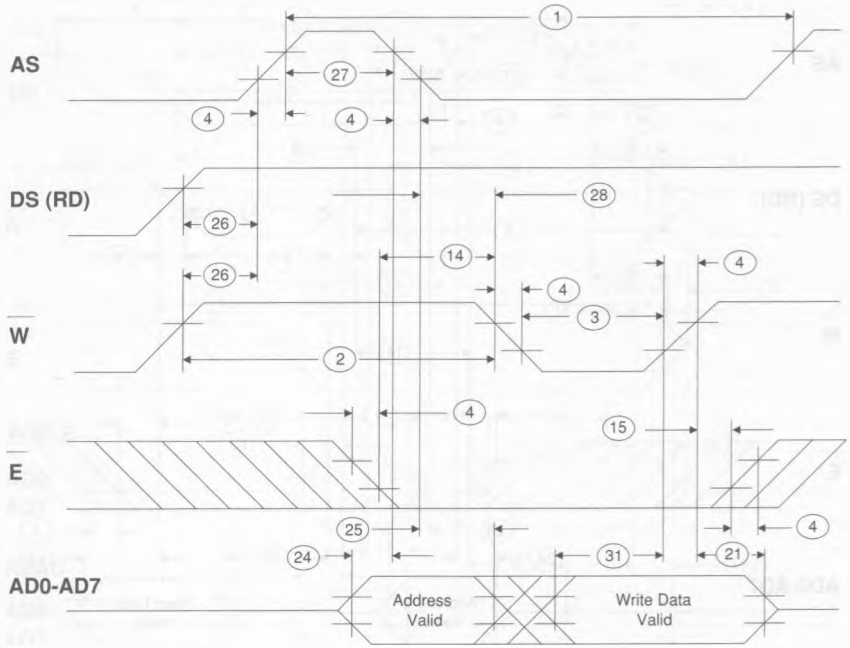


FIGURE 7 . IRQ RELEASE TIMING

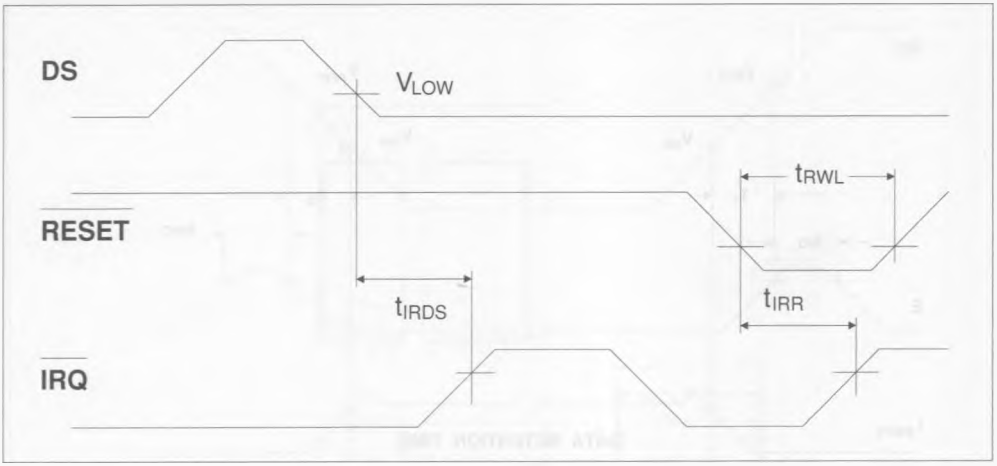
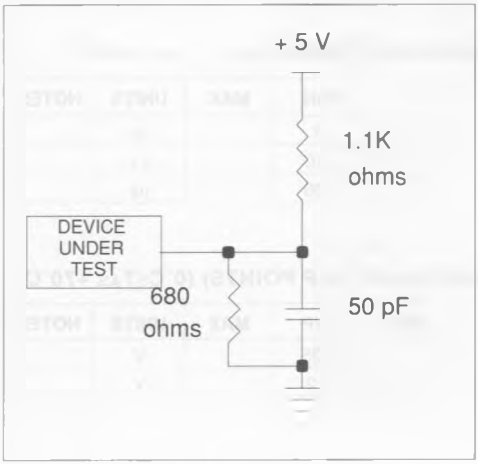


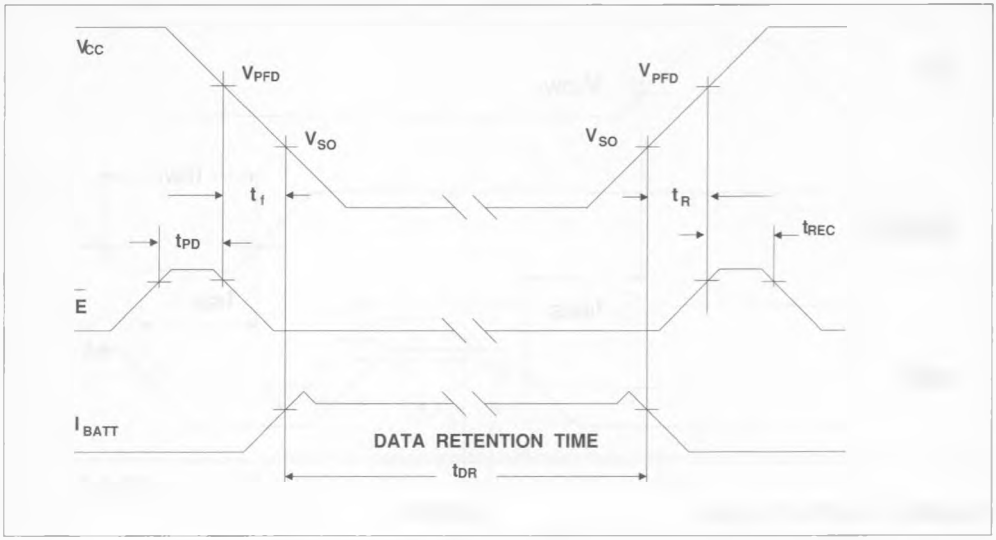
FIGURE 8 . OUTPUT LOAD



NOTES:

1. All voltages are referenced to ground.
2. All outputs are open.
3. The MOT pin has an internal pull-down of 20K.
4. Applies to the AD0-AD7 pins, the IRQ pin and the SQW pin when each is in the high impedance state.
5. The IRQ pin is open drain.
6. Measured with a load as shown in Figure 8.

FIGURE 9 . POWER-UP / POWER-DOWN CONDITIONS



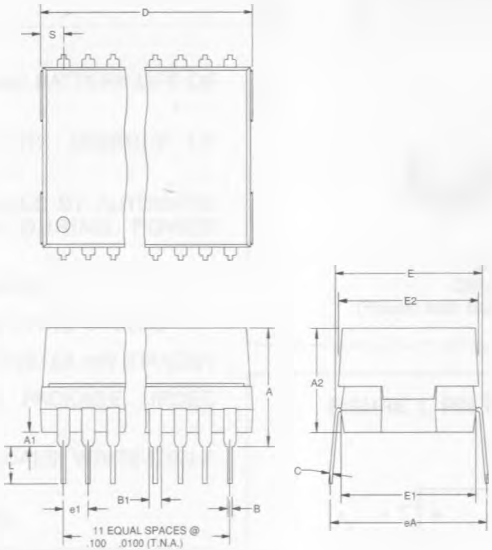
AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (0°C ≤ T_A ≤ +70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	E or W at V_{IH} Before Power Down	0		ns	
t_F	V_{PFD} to V_{SO} V_{CC} Fall Time	310		µs	
t_R	V_{SO} to V_{PFD} V_{CC} Rise Time	100		µs	

DC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TRIP POINTS) (0°C≤T_A≤ +70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{PFD}	Power-fail Deselect Voltage		4.25		V	
V_{SO}	Battery Back-up Switchover Voltage		3.2		V	

FIGURE 10 . PACKAGE DESCRIPTION 24 PIN "B" PACKAGE



DIM	INCHES		NOTES
	MIN	MAX	
A	.320	.380	2
A1	.015	.030	2
A2	.300	.360	
B	.015	.021	3
B1	.045	.070	
C	.008	.012	3
D	-	1.295	1
E	.530	.640	
E1	.530	.550	
E2	.550	.570	
e1	.090	.110	
eA	.600	.700	
L	.120	.150	
S	.060	.090	

NOTES

1 OVERALL LENGTH INCLUDES FLASH AND PROJECTIONS ON EITHER END OF PACKAGE.

2 PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.

3 THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN WHEN SOLDER LEAD FINISH IS SPECIFIED.