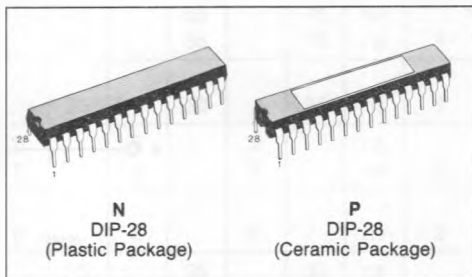
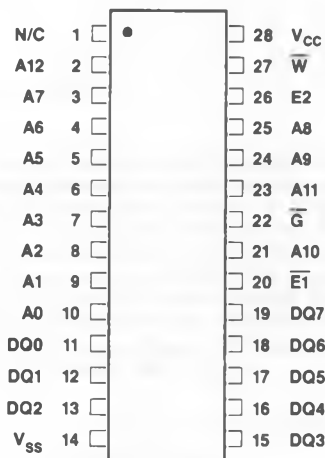


64K (8K × 8-BIT) CMOS FAST STATIC RAM

ADVANCED DATA

- 35, 45, 55, AND 70 ns ADDRESS ACCESS TIME
- EQUAL ACCESS AND CYCLE TIMES
- STATIC OPERATION - NO CLOCKS OR TIMING STROBES REQUIRED
- LOW V_{CC} DATA RETENTION 2 VOLTS
- ALL INPUTS AND OUTPUTS ARE CMOS AND TTL COMPATIBLE
- LOW POWER OPERATION, 10 μ A CMOS STANDBY CURRENT UTILIZING FULL CMOS 6-T CELL
- THREE STATE OUTPUT
- STANDARD 28-PIN PACKAGE IN 600 MIL PLASTIC OR 600 MIL CERAMIC DIP. MK48H65 AVAILABLE IN 300 MIL PLASTIC DIP.


FIGURE 1. PIN CONNECTIONS

MK48H64/MK48H65 TRUTH TABLE

| W | E1 | E2 | G | MODE | DQ | POWER |
|---|----|----|---|----------|-----------|---------|
| X | H | X | X | Deselect | High-Z | Standby |
| X | X | L | X | Deselect | High-Z | Standby |
| H | L | H | H | Read | High-Z | Active |
| H | L | H | L | Read | Q_{OUT} | Active |
| L | L | H | X | Write | D_{IN} | Active |

DESCRIPTION

The MK48H64 and MK48H65 are 65,536-bit fast static RAMs organized as 8K × 8 bits. They are fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The devices feature fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. They require a single +5V ± 10 % supply, and are fully TTL compatible.

The MK48H64 and MK48H65 have a Chip Enable power down feature which sustains an automatic standby mode whenever either Chip Enable goes inactive (E1 goes high or E2 goes low). An Output

PIN NAMES

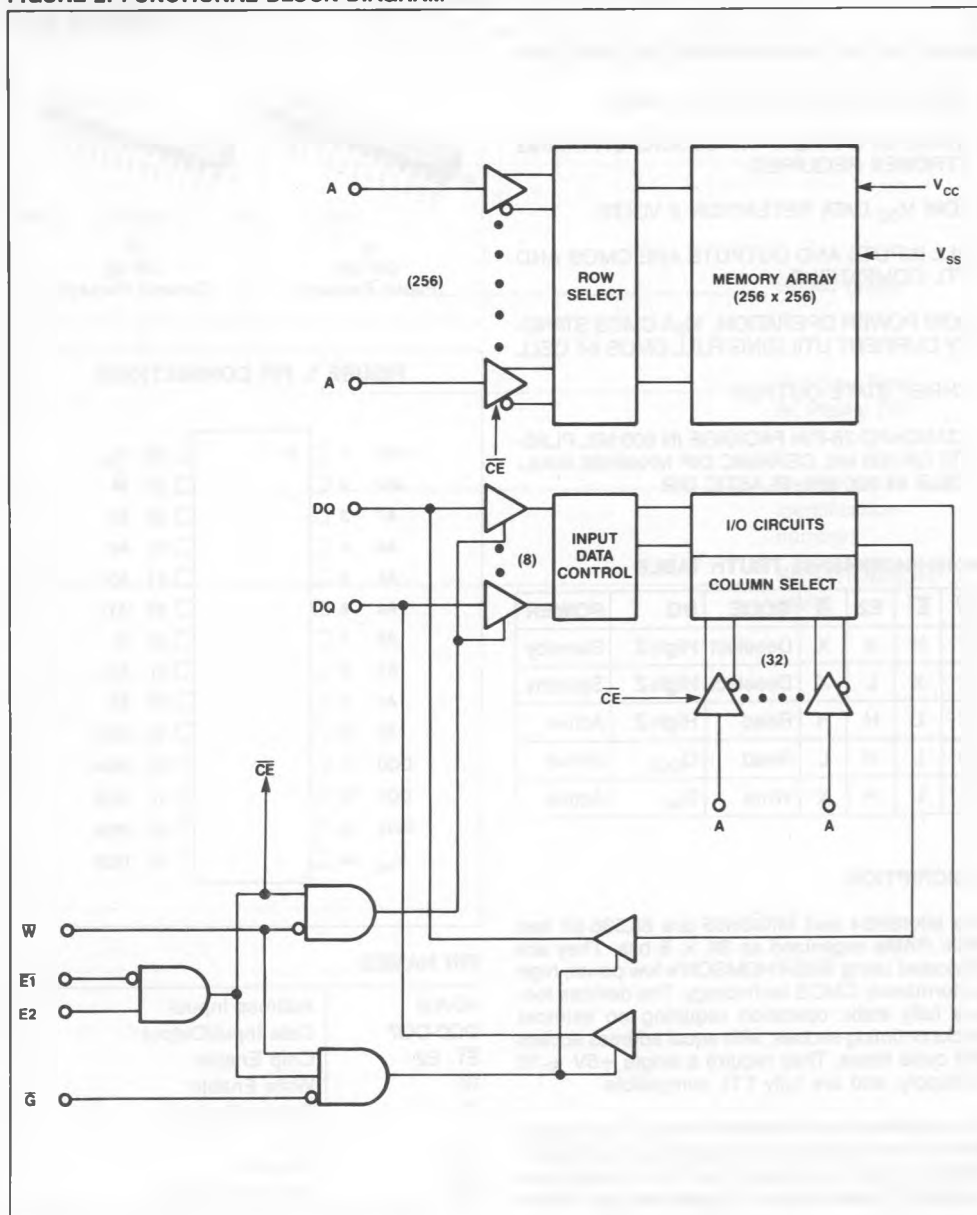
| | |
|----------|-------------------|
| A0-A12 | Address Inputs |
| DQ0-DQ7 | Data Input/Output |
| E1, E2 | Chip Enable |
| W | Write Enable |
| G | Output Enable |
| V_{CC} | +5V |
| V_{SS} | Ground |
| N/C | No Connection |

Enable (\bar{G}) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs \bar{W} , \bar{G} , $\bar{E}1$,

and $\bar{E}2$, as summarized in the truth table.

The MK48H65 is a space saving 300 mil plastic DIP. The MK48H64 offers the standard 600 mil Plastic or Ceramic DIP.

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM



READ CYCLE TIMING

| SYMBOLS | | PARAMETER | 48H6X-35 | | 48H6X-45 | | 48H6X-55 | | 48H6X-70 | | UNITS | NOTES |
|--------------------|-------------|--------------------------------------|----------|-----|----------|-----|----------|-----|----------|-----|-------|-------|
| ALT. | STD. | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t_{RC} | t_{AVAV} | Read Cycle Time | 35 | | 45 | | 55 | | 70 | | ns | |
| t_{AA} | t_{AVQV} | Address Access Time | | 35 | | 45 | | 55 | | 70 | ns | 1 |
| t_{CEA} 1 & 2 | t_{E1LQV} | Chip Enable 1 & 2 Access Time | | 35 | | 45 | | 55 | | 70 | ns | 1 |
| | t_{E2HQV} | | | 35 | | 45 | | 55 | | 70 | ns | |
| t_{OEA} | t_{GLQV} | Output Enable Access Time | | 20 | | 25 | | 30 | | 35 | ns | 1 |
| t_{CEL} 1 & 2 | t_{E1LQX} | Chip Enable 1 & 2 to Output Low-Z | 5 | | 5 | | 5 | | 5 | | ns | 2 |
| | t_{E2HQX} | | 5 | | 5 | | 5 | | 5 | | ns | |
| t_{OEL} | t_{GLQX} | Output Enable to Low-Z | 0 | | 0 | | 0 | | 0 | | ns | 2 |
| t_{CEZ} 1 & 2 | t_{E1HQZ} | Chip Enable 1 & 2 to High-Z | | 15 | | 20 | | 25 | | 30 | ns | 2 |
| | t_{E2LQZ} | | | 15 | | 20 | | 25 | | 30 | ns | |
| t_{OEZ} | t_{GHQZ} | Output Enable to High-Z | | 15 | | 20 | | 25 | | 30 | ns | 2 |
| t_{OH} | t_{AXQX} | Output Hold From Address Change | 5 | | 5 | | 5 | | 5 | | ns | 1 |

OPERATIONS

READ MODE

The MK48H64 and MK48H65 are in the read mode whenever Write Enable (\bar{W}) is high with Output Enable (\bar{G}) low, and both Chip Enables ($\bar{E}1$ and $\bar{E}2$) are active. This provides access to data from eight of 65,536 locations in the static memory array. The unique address specified by the 13 Address Inputs defines which one of the 8192 8-bit bytes is to be accessed.

Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing \bar{G} is low, $\bar{E}1$ is low, and $\bar{E}2$ is high. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{E1LQV} , t_{E2HQV} , or t_{GLQV}) rather than the address. The state of the DQ pins is controlled by the $\bar{E}1$, $\bar{E}2$, \bar{G} , and \bar{W} control signals. Data out may be indeterminate at t_{E1LQX} , t_{E2HQX} , and t_{GLQX} , but data lines will always be valid at t_{AVQV} .

FIGURE 3. READ TIMING NO. 1 (ADDRESS ACCESS)

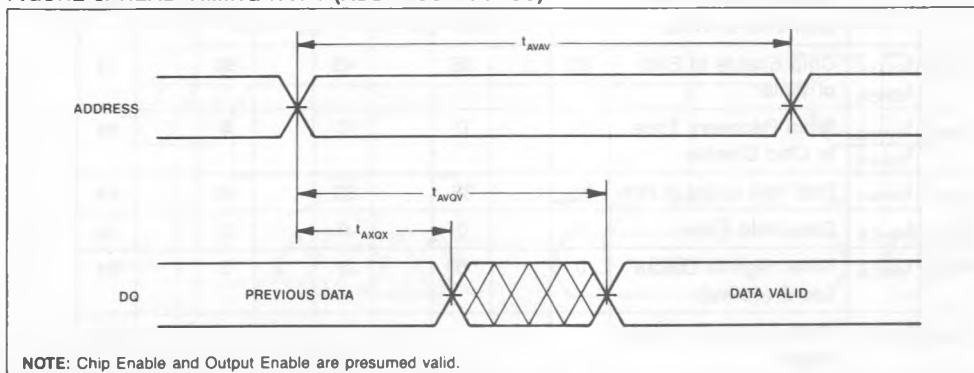
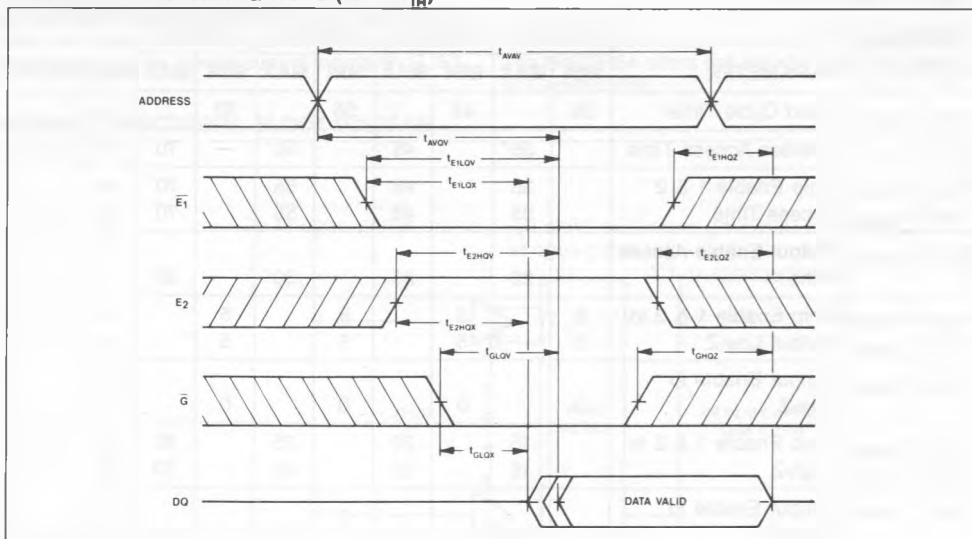


FIGURE 4. READ TIMING NO. 2 ($\bar{W} = V_{IH}$)

WRITE CYCLE TIMING

| SYMBOLS | | PARAMETER | 48H6X-35 | | 48H6X-45 | | 48H6X-55 | | 48H6X-70 | | UNITS | NOTES |
|-----------|------------------------------|---|----------|-----|----------|-----|----------|-----|----------|-----|-------|-------|
| ALT. | STD. | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| t_{WC} | t_{AVAV} | Write Cycle Time | 35 | | 45 | | 55 | | 70 | | ns | |
| t_{AS} | t_{AVWL} | Address Set-up Time to Write Enable Low | 0 | | 0 | | 0 | | 0 | | ns | |
| t_{AS} | t_{AVE1L} t_{AVE2H} | Address Set-up Time to Chip Enable | 0 | | 0 | | 0 | | 0 | | ns | |
| t_{AW} | t_{AVWH} | Address Valid to End of Write | 25 | | 35 | | 45 | | 60 | | ns | |
| t_{WEW} | t_{WLWH} | Write Pulse Width | 25 | | 35 | | 45 | | 60 | | ns | |
| t_{AH} | t_{WHAX} | Address Hold Time after End of Write | 0 | | 0 | | 0 | | 0 | | ns | |
| t_{CEW} | t_{E1LE1H} t_{E2HE2L} | Chip Enable to End of Write | 25 | | 35 | | 45 | | 60 | | ns | |
| t_{WR} | t_{E1HAX} t_{E2LAX} | Write Recovery Time to Chip Disable | 0 | | 0 | | 0 | | 0 | | ns | |
| t_{DW} | t_{DVWH} | Data Valid to End of Write | 25 | | 30 | | 30 | | 40 | | ns | |
| t_{DH} | t_{WHDX} | Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns | |
| t_{WEL} | t_{WHQX} | Write High to Output Low-Z (Active) | 0 | | 0 | | 0 | | 0 | | ns | 2 |
| t_{WEZ} | t_{WLQZ} | Write Enable to Output High-Z | | 15 | | 20 | | 25 | | 30 | ns | 2 |

WRITE MODE

The MK48H64 and MK48H65 are in the Write mode whenever the \overline{W} and $\overline{E1}$ pins are low, with $E2$ high. Either Chip Enable pin or \overline{W} must be inactive during Address transitions. The Write begins with the concurrence of both Chip Enables being active with \overline{W} low. Therefore address setup times are referenced to Write Enable and both Chip Enables as t_{AVWL} , t_{AVE1L} , and t_{AVE2H} respectively, and is determined to the latter occurring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$ or \overline{W} , or the falling edge of $E2$.

If the Output is enabled ($\overline{E1}$ = low, $E2$ = high, \overline{G} = low), then \overline{W} will return the outputs to high impedance within t_{WLOZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E1}$ or the falling edge of $E2$, whichever occurs first, and remain valid t_{WHDX} after the rising edge of $\overline{E1}$ or \overline{W} , or the falling edge of $E2$.

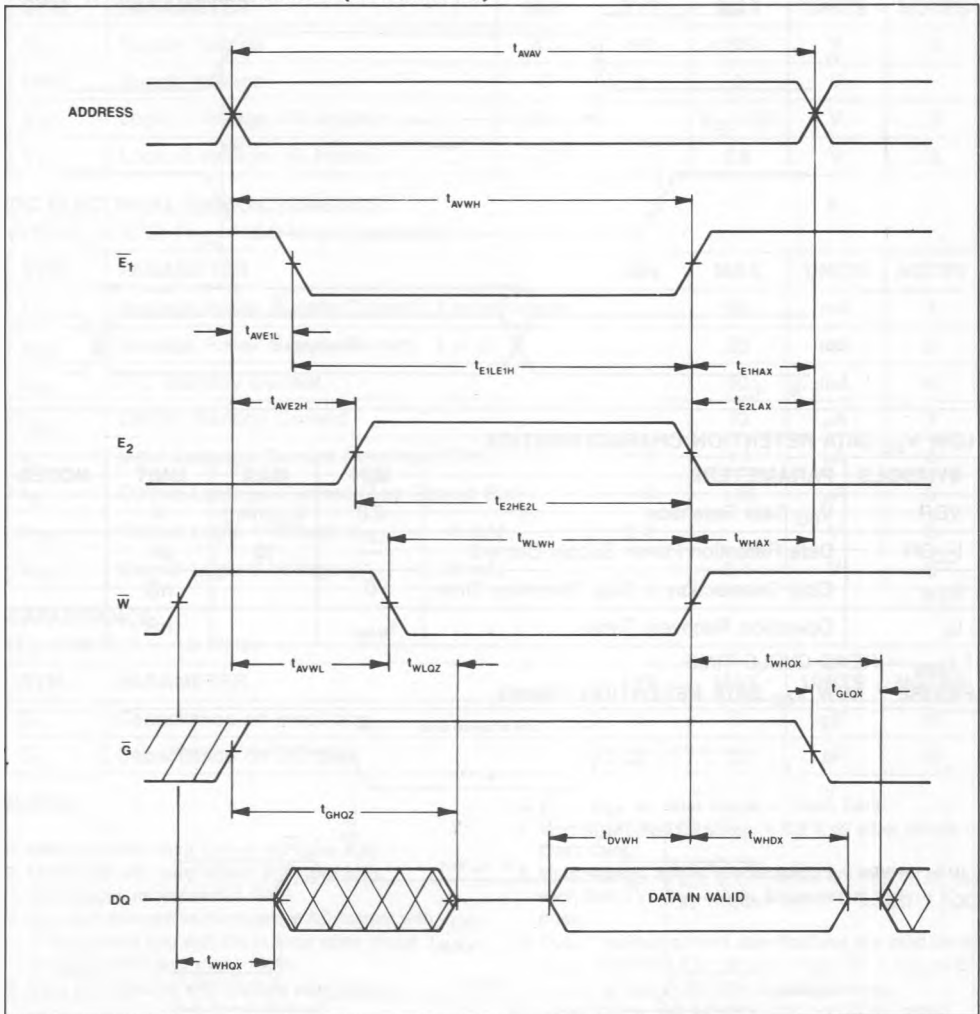
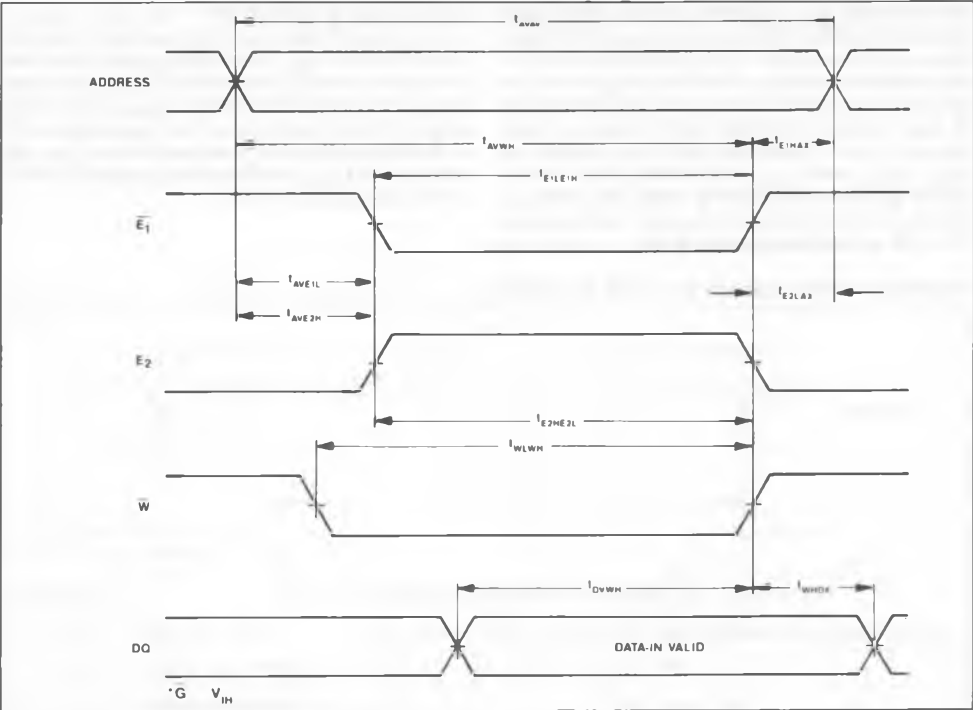
FIGURE 5. WRITE TIMING NO. 1 (\overline{W} CONTROL)

FIGURE 6. WRITE TIMING NO. 2 (E₁, E₂ CONTROL)

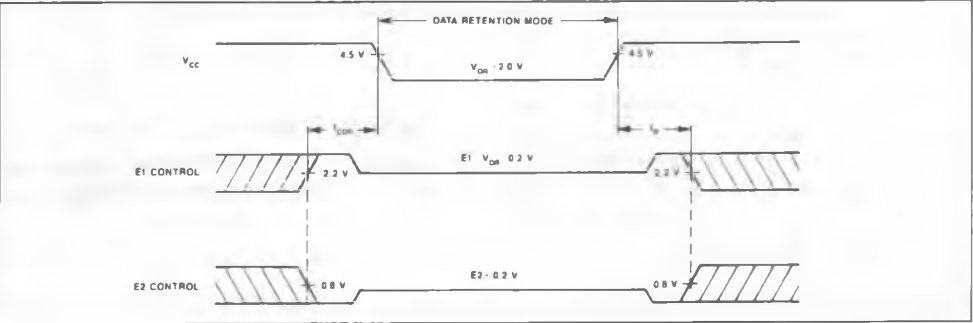


LOW V_{CC} DATA RETENTION CHARACTERISTICS

| SYMBOLS | PARAMETERS | MIN | MAX | UNIT | NOTES |
|-------------------|---|---------------------|-----------------------|------|-------|
| VDR | V _{CC} Data Retention | 2.0 | V _{CC} (min) | V | |
| I _{CCDR} | Data Retention Power Supply Current | — | 10 | μA | |
| t _{CDR} | Chip Deselection to Data Retention Time | 0 | | nS | |
| t _R | Operation Recovery Time | t _{AVAV} * | | nS | |

* t_{AVAV} = READ CYCLE TIME

FIGURE 7. LOW V_{CC} DATA RETENTION TIMING



ABSOLUTE MAXIMUM RATINGS

| | |
|---|------------------|
| Voltage on any pin relative to GND | -1.0 V to +7.0 V |
| Ambient Operating Temperature (T_A) | 0°C to +70°C |
| Ambient Storage Temperature (Plastic) | -55°C to +125°C |
| Ambient Storage Temperature (Ceramic) | -65°C to +150°C |
| Total Device Power Dissipation | 1 Watt |
| Output Current per Pin | 50 mA |

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

| SYM | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|-----------------|-----------------------------|------|-----|----------------------|-------|-------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V | 3 |
| GND | Supply Voltage | 0 | 0 | 0 | V | |
| V _{IH} | Logic 1 Voltage, All Inputs | 2.2 | | V _{CC} +0.3 | V | 3 |
| V _{IL} | Logic 0 Voltage, All Inputs | -0.3 | | 0.8 | V | 3 |

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

| SYM | PARAMETER | MIN | MAX | UNITS | NOTES |
|------------------|---|-----|-----|-------|-------|
| I _{CC1} | Average Power Supply Current $f = \text{min cycle}$ | | 90 | mA | 4 |
| I _{CC2} | Average Power Supply Current $f = 0$ | | 20 | mA | 5 |
| I _{SB1} | TTL Standby Current | | 10 | mA | 6 |
| I _{SB2} | CMOS Standby Current | | 10 | μA | 7 |
| I _{IL} | Input Leakage Current (Any Input Pin) | -1 | +1 | μA | 8 |
| I _{OL} | Output Leakage Current (Any Output Pin) | -10 | +10 | μA | 9 |
| V _{OH} | Output Logic 1 Voltage (I _{OUT} = -4 mA) | 2.4 | | V | 3 |
| V _{OL} | Output Logic 0 Voltage (I _{OUT} = +8 mA) | | 0.4 | V | 3 |

CAPACITANCE

($T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

| SYM | PARAMETER | TYP | MAX | UNITS | NOTES |
|----------------|---------------------------|-----|-----|-------|-------|
| C ₁ | Capacitance on input pins | 4 | 5 | pF | 10 |
| C ₂ | Capacitance on DQ pins | 8 | 10 | pF | 10 |

NOTES

- Measured with load shown in Figure 8(A).
- Measured with load shown in Figure 8(B).
- All voltages referenced to GND.
- I_{CC1} is measured as the average AC current with V_{CC} = V_{CC} (max) and with the outputs open circuit. $t_{AVAV} = t_{AVAV} \text{ (min) duty cycle } 100\%$.
- I_{CC2} is measured with outputs open circuit.
- $\overline{E1} = V_{IH}$, all other Inputs = Don't Care.
- V_{CC} (max), and E2 ≤ V_{SS} + 0.3 V, all other Inputs = Don't Care.
- Input leakage current specifications are valid for all V_{IN} such that 0 V < V_{IN} < V_{CC}. Measured at V_{CC} = V_{CC} (max).
- Output leakage current specifications are valid for all V_{OUT} such that 0 V < V_{OUT} < V_{CC}. $\overline{E1} = V_{IH}$ or E2 = V_{IL}, and V_{CC} in valid operating range.
- Capacitances are sampled and not 100% tested.

AC TEST CONDITIONS

| | |
|--|--------------------|
| Input Levels | GND to 3.0 V |
| Transition Times | 5 ns |
| Input and Output Signal Timing Reference Level | 1.5 V |
| Ambient Temperature | 0°C to 70°C |
| V _{CC} | 5.0 V ± 10 percent |

FIGURE 8. OUTPUT LOAD CIRCUITS

