

(64×5)×2

CMOS BIDIRECTIONAL BiPORT FIFO/TRANSCIEVER

ADVANCED DATA

- DUAL 64x5 FIFOs PLUS A '245-TYPE TRANSCIEVER FUNCTION
- FULLY ASYNCHRONOUS DUAL PORT OPERATION
- EMPTY, FULL, ALMOST FULL AND ALMOST EMPTY STATUS FLAGS
- SPARE BITS FOR PARITY AND BEGINNING/END-OF-MESSAGE FLAGS
- +/- 12mA OUTPUT DRIVE CAPABILITY
- DUAL V_{CC} AND V_{SS} FOR IMPROVED MARGIN AND DRIVE
- 300 MIL DIP PACKAGE
- APPLICATION: ARBITRATION-FREE μ P-TO- μ P MESSAGE PASSING

PART NUMBER	ACCESS TIME	CYCLE TIME	CYCLE RATE
MK45264N-55	55 ns	75 ns	13.3 MHz
MK45264N-70	70 ns	95 ns	10.5 MHz
MK45265N-55	55 ns	75 ns	13.3 MHz
MK45265N-70	70 ns	95 ns	10.5 MHz

PIN NAMES

V_{CC} , V_{SS} = +5V, GND
 DQ_{X0} - DQ_{X4} = X Port Data I/O
 DQ_{Y0} - DQ_{Y4} = Y Port Data I/O
 $\overline{W}_X$, $\overline{W}_Y$ = X & Y Port Write Enables
 $\overline{R}_X$ /DIR = X Port Read Enable and Transceiver Direction Control
 $\overline{G}$ = Transceiver Enable
 $\overline{R}_Y$ = Y Port Read Enable
 $\overline{RS}$ = Master Reset
 $\overline{EF}_X$, $\overline{FF}_Y$ = Y-to-X FIFO Empty/Full Flag
 $\overline{EF}_Y$, $\overline{FF}_X$ = X-to-Y FIFO Empty/Full Flag
 $\overline{AE}_Y$, $\overline{AF}_X$ = X-to-Y FIFO Almost Empty/Full
 $\overline{AE}_X$, $\overline{AF}_Y$ = Y-to-X FIFO Almost Empty/Full

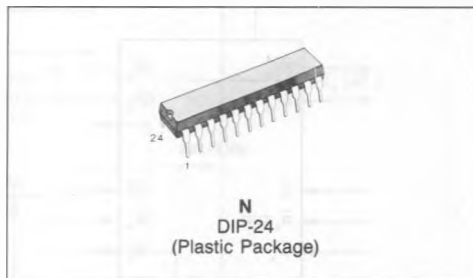


FIGURE 1. PINOUT. 24 PIN, 300 MIL DIP

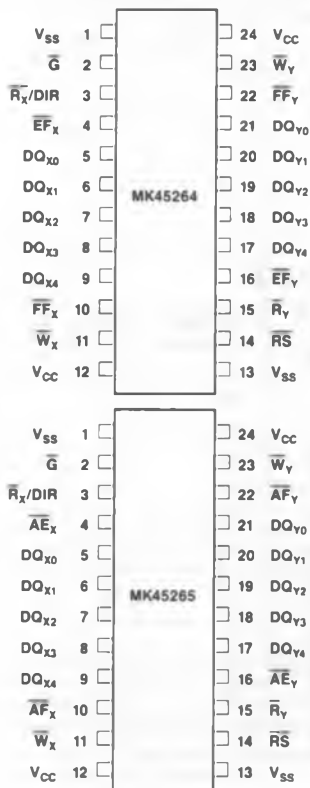
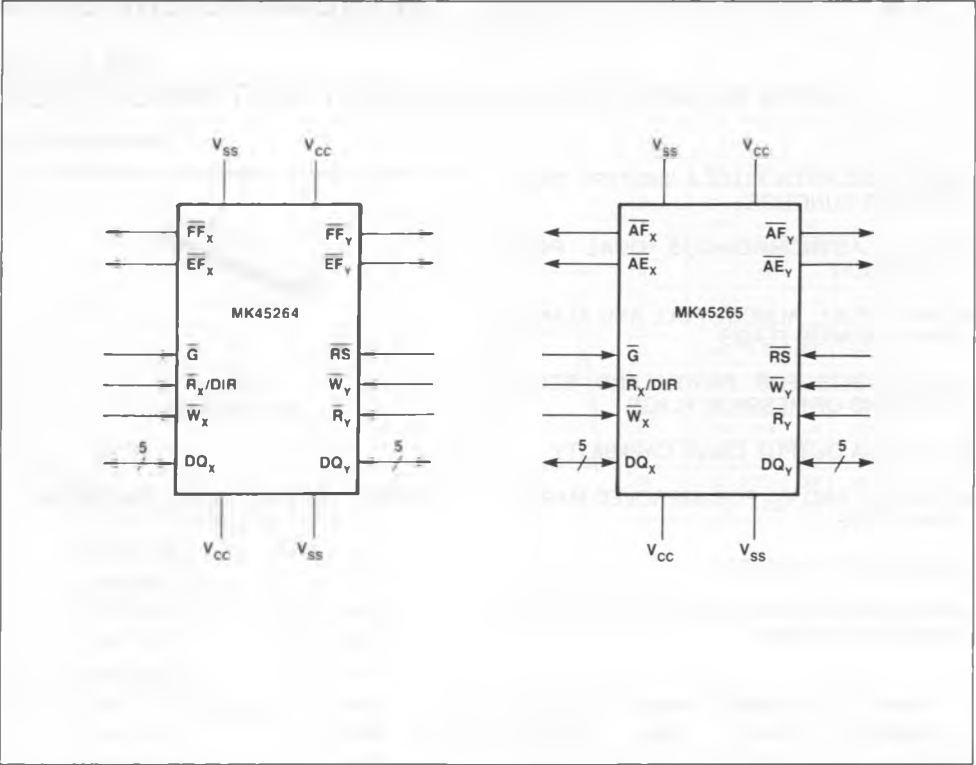


FIGURE 2. DEVICE LOGIC SYMBOL



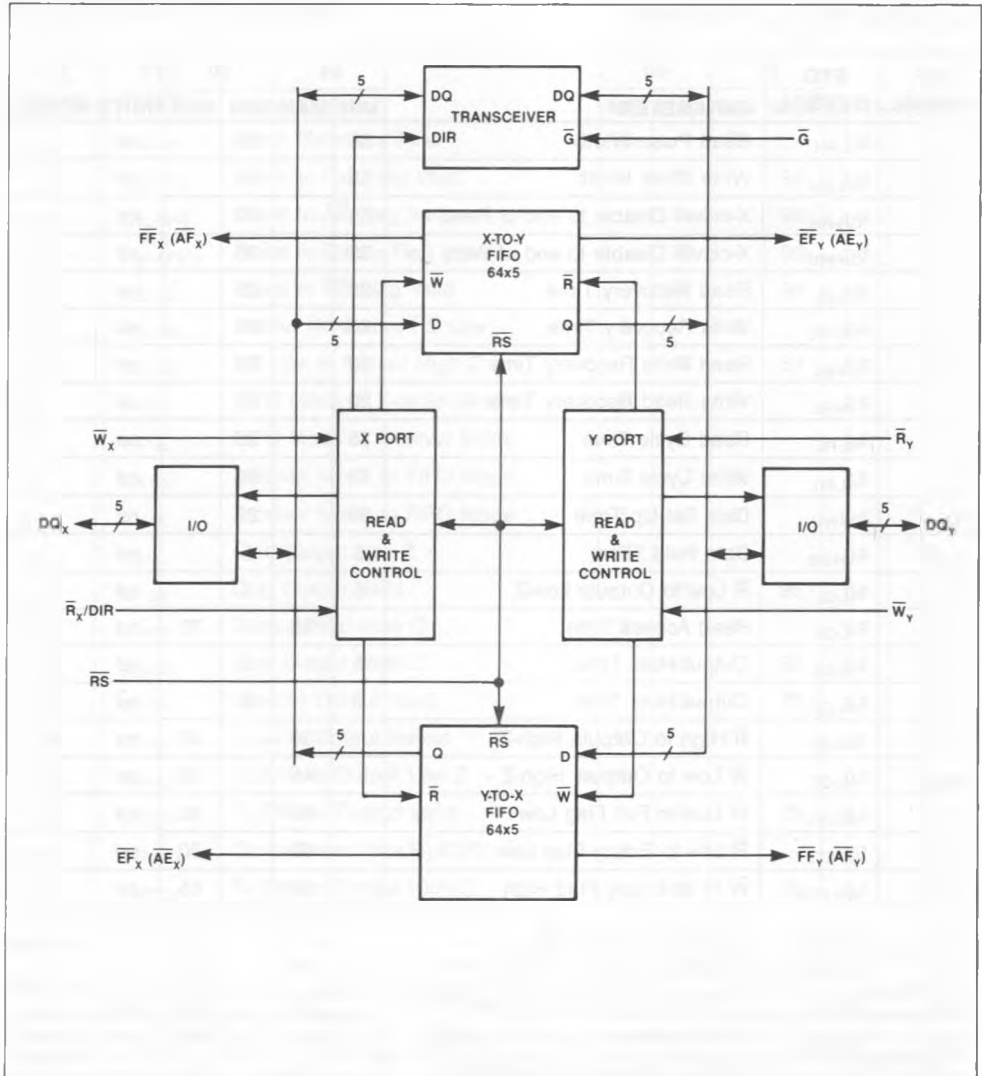
TRUTH TABLE

RS	G	R _x /DIR	W _x	R _y	W _y	MOE	DQ _x	DQ _y
Lo	X	X	X	X	X	Master Reset	High Z	High Z
Hi	Lo	Hi	X	X	X	Transparent X-Y	Data In	DQ _x
Hi	Lo	Lo	X	X	X	Transparent Y-X	DQ _y	Data In
Hi	Hi	Hi	Hi	Hi	Hi	Sby X / Sby Y	High Z	High Z
Hi	Hi	Hi	Hi	Lo	Hi	Sby X / Read Y	High Z	Data Out
Hi	Hi	Hi	Hi	X	Lo	Sby X / Write Y	High Z	Data In
Hi	Hi	Lo	Hi	Hi	Hi	Read X / Sby Y	Data Out	High Z
Hi	Hi	Lo	Hi	Lo	Hi	Read X / Read Y	Data Out	Data Out
Hi	Hi	Lo	Hi	X	Lo	Read X / Write Y	Data Out	Data In
Hi	Hi	X	Lo	Hi	Hi	Write X / Sby Y	Data In	High Z
Hi	Hi	X	Lo	Lo	Hi	Write X / Read Y	Data In	Data Out
Hi	Hi	X	Lo	X	Lo	Write X / Write Y	Data In	Data In

X = Don't Care

NOTE: Truth Table logic states presume all status flags to be inactive.

FIGURE 3. BLOCK DIAGRAM



DEVICE APPLICATION/FUNCTION

The MK45264/65 contains two independent single direction FIFOs, and a bidirectional transceiver, connected via two internal three state busses to I/O drive circuits. One FIFO is pointed X-to-Y, and the other pointed Y-to-X. Either port's FIFOs can be read or written asynchronous with FIFO read or write operations on the other port. The transceiver is activated with a low on $\overline{G}$.

Once the transceiver is activated, direction is controlled by the $\overline{R}_x/\text{DIR}$ pin. A high on $\overline{R}_x/\text{DIR}$ points the transceiver X-to-Y; a low points it Y-to-X. A low on $\overline{G}$ disables FIFO operations. Activating the Transceiver during FIFO operations may result in invalid or unpredictable FIFO operation.

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t _P	t _{RL-RH}	Read Pulse Width	55		70		ns	
t _P	t _{WL-WH}	Write Pulse Width	55		70		ns	
t _P	t _{GH-RH}	X-ceiver Disable to end of Read	55		70		ns	
t _P	t _{GH-WH}	X-ceiver Disable to end of Write	55		70		ns	
t _R	t _{RH-RL}	Read Recovery Time	20		25		ns	
t _R	t _{WH-WL}	Write Recovery Time	20		25		ns	
t _R	t _{RH-WL}	Read Write Recovery Time	20		25		ns	
t _R	t _{WH-RL}	Write Read Recovery Time	20		25		ns	
t _C	t _{RL-RL}	Read Cycle Time	75		95		ns	
t _C	t _{WL-WL}	Write Cycle Time	75		95		ns	
t _{DS}	t _{DV-WH}	Data Set Up Time	20		25		ns	
t _{DH}	t _{WH-DX}	Data Hold Time	5		5		ns	
t _{QL}	t _{RL-QL}	$\bar{R}$ Low to Outputs Low-Z	5		5		ns	2
t _A	t _{RL-QV}	Read Access Time		55		70	ns	3
t _{OH}	t _{RH-QX}	Output Hold Time	5		5		ns	3
t _{OH}	t _{WL-QX}	Output Hold Time	5		5		ns	3
t _{QZ}	t _{RH-QZ}	$\bar{R}$ High to Outputs High-Z		30		40	ns	2
t _{WQZ}	t _{WL-QZ}	$\bar{W}$ Low to Outputs High-Z		45		55	ns	2
t _{FL1}	t _{WL-FFL}	$\bar{W}$ Low to Full Flag Low		60		80	ns	4
t _{FL1}	t _{RL-EFL}	$\bar{R}$ Low to Empty Flag Low		60		80	ns	4
t _{FH1}	t _{WH-EFH}	$\bar{W}$ Hi to Empty Flag High		50		65	ns	4
t _{FH1}	t _{RH-FFH}	$\bar{R}$ Hi to Full Flag High		50		65	ns	4
t _{FL2}	t _{WL-AFL}	$\bar{W}$ Low to Almost Full Flag Low		60		80	ns	5
t _{FL2}	t _{RL-AEL}	$\bar{R}$ Low to Almost Empty Flag Low		60		80	ns	5
t _{FH2}	t _{WH-AEH}	$\bar{W}$ Hi to Almost Empty Flag High		75		95	ns	5
t _{FH2}	t _{RH-AFH}	$\bar{R}$ Hi to Almost Full Flag High		75		95	ns	5
t _I	t _{WL-FFH}	Write Protect Indeterminate		25		30	ns	6
t _I	t _{RL-EFH}	Read Protect Indeterminate		25		30	ns	7
t _{FR}	t _{FFH-WL}	Full Flag Recovery	0		0		ns	6
t _{FR}	t _{EFH-RL}	Empty Flag Recovery	0		0		ns	7
t _{RS}	t _{RSL-RSH}	Reset Pulse Width	55		70		ns	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0° to 70°C, V_{CC} = 5.0 ±10%)

ALT. SYMBOL	STD. SYMBOL	PARAMETER	55		70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
t _{RSR}	t _{RSR-WH}	Reset Recovery Time	75		95		ns	
t _{RFV}	t _{RSL-FFH}	Reset to Full Flag Valid		70		90	ns	3
t _{RFV}	t _{RSL-AFH}	Reset to $\overline{AF}$ Flag Valid		70		90	ns	3
t _{RFV}	t _{RSL-EFL}	Reset to Empty Flag Valid		70		90	ns	3
t _{RFV}	t _{RSL-AEL}	Reset to $\overline{AE}$ Flag Valid		70		90	ns	3
t _{RQX}	t _{RSL-QX}	Outout Hold from $\overline{RS}$ Low	0		0		ns	3
t _{RQZ}	t _{RSL-QZ}	RS Low to Output High Z		40		50	ns	2
t _{FG}	t _{WH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t _{FG}	t _{RH-GL}	FIFO Mode to X-ceiver Mode	0		0		ns	
t _{GF}	t _{GH-WL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t _{GF}	t _{GH-RL}	X-ceiver Mode to FIFO Mode	5		5		ns	
t _{GQL}	t _{GL-QL}	$\overline{G}$ to Output Low Z	0		0		ns	2
t _{GQV}	t _{GL-QV}	$\overline{G}$ to Output Valid		75		95	ns	3
t _{GQX}	t _{GH-QX}	Output Hold from $\overline{G}$	0		0		ns	3
t _{GQZ}	t _{GH-QZ}	$\overline{G}$ to Output High Z		40		50	ns	2
t _{DQV}	t _{DV-QV}	Input to Output Valid		55		70	ns	3
t _{DXQX}	t _{DX-QX}	Input to Output Invalid	10		10		ns	3
t _{DQL}	t _{DIRV-QL}	$\overline{R}_X$ /DIR to Output Low Z	0		0		ns	2
t _{DQV}	t _{DIRV-QV}	$\overline{R}_X$ /DIR to Output Valid		55		70	ns	3
t _{DQX}	t _{DIRV-QX}	Output Hold from $\overline{R}_X$ /DIR	0		0		ns	3
t _{DQZ}	t _{DIRV-QZ}	$\overline{R}_X$ /DIR to Output High Z		40		50	ns	2

NOTES

1. All AC Electrical Characteristics measured under conditions specified in "AC Test Conditions".
2. Measured w/5pf Output Load. See Equivalent Load Circuit B.
3. Measured w/30pf Output Load. See Equivalent Load Circuit A.
4. Applies to $\overline{EF}_X$, $\overline{FF}_X$, $\overline{FF}_Y$, $\overline{EF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
5. Applies to $\overline{AE}_X$, $\overline{AF}_X$, $\overline{AE}_Y$, $\overline{AF}_Y$. Measured w/30pf Output Load. See Equivalent Load Circuit C.
6. Writes beginning a) more than t_I (max) before $\overline{FF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{FF}$ goes high may be performed. c) t_{FR} (min) after $\overline{FF}$ goes high will be performed.
7. Reads beginning a) more than t_I (max) before $\overline{EF}$ goes high will be blocked. b) less than t_I (max) before and less than t_{FR} (min) after $\overline{EF}$ goes high may be performed. c) t_{FR} (min) after $\overline{EF}$ goes high will be performed.

Read/Write

The FIFOs utilize separate Read and Write enable inputs to control port activity and direction. A low on a Read Enable reads a port's receive FIFO. A high on a Read Enable or a low on a Write Enable disables a port's data outputs to a high impedance state. A low on a Write Enable initiates a write to a port's transmit FIFO, regardless of the state of Read Enable. Input data is latched into the FIFO on the rising edge of a Write Enable.

Full/Empty Flags

An active Full Flag indicates that a port's transmit FIFO is full and will accept no more data. Writes done to a FIFO while full are blocked. Once a read has occurred on a full FIFO, clearing a location in the FIFO, the Full Flag will go inactive, allowing another write to begin on the next falling edge of Write Enable.

An active Empty Flag indicates a port's receive FIFO is empty and can send no more data. Any reads done on a FIFO while empty are blocked. Once a write to an empty FIFO has occurred, the Empty Flag will go inactive, allowing another read to begin on the next falling edge of Read Enable.

Almost Flags

An inactive Almost Full flag indicates a port's transmit FIFO has room for at least four (4) more bytes, which is to say the flag will go active during the fourth write from full and stay active until after the fourth location from full has been vacated (read). An inactive Almost Empty flag indicates a port's receive FIFO has at least four (4) bytes of data in memory, ready to be read, which is to say that the flag will go active while reading the fourth remaining byte and remain active until after the fourth byte has been stored (written).

Reset

Reset is initiated by a low on the Master Reset ($\overline{RS}$) input. A reset returns all data outputs to a high impedance state, taking precedence over the read strobes ($\overline{R_X}/\overline{DIR}$ and $\overline{R_Y}$) and $\overline{G}$. The states of the FIFO control inputs ($\overline{R_X}/\overline{DIR}$, $\overline{W_X}$, $\overline{R_Y}$ and $\overline{W_Y}$) are a Don't Care throughout reset. The read strobes are a Don't Care at the end of reset because the Empty Flag becomes active (goes low) during reset, blocking any attempted reads. The write strobes ($\overline{W_X}$ and $\overline{W_Y}$) may fall any time during or after reset, but must not go high until t_{RSR} after $\overline{RS}$ goes high.

FIGURE 4. WRITE TIMING

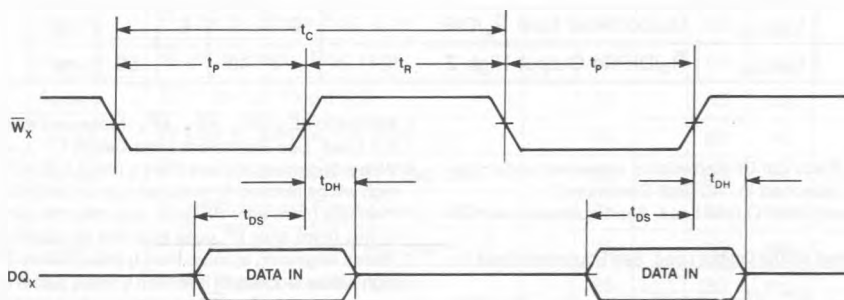


FIGURE 5. READ TIMING

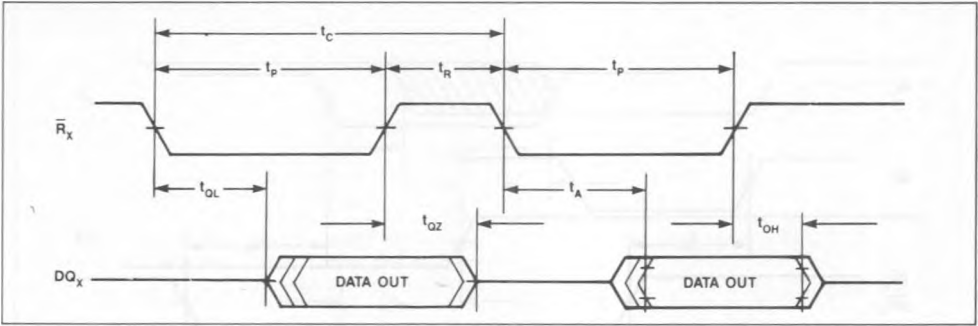


FIGURE 6. WRITE/READ TIMING

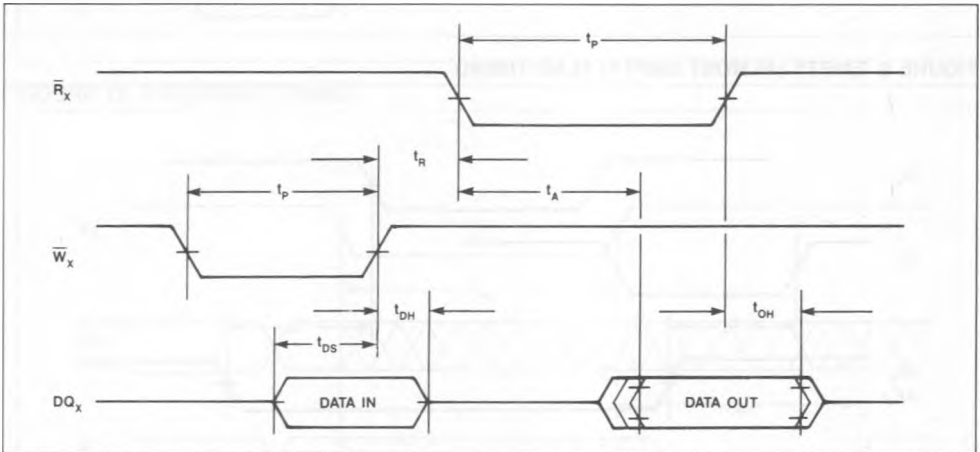


FIGURE 7. READ/WRITE TIMING

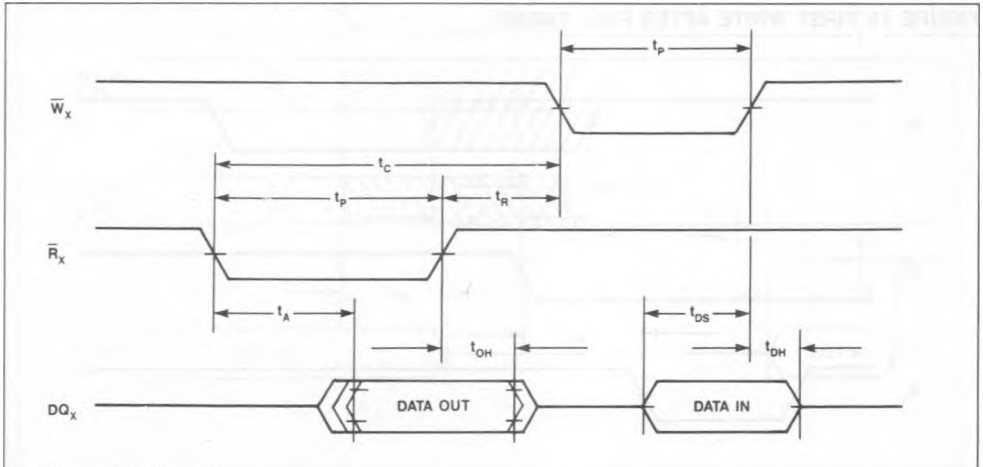


FIGURE 8. FULL (ALMOST FULL) FLAG TIMING

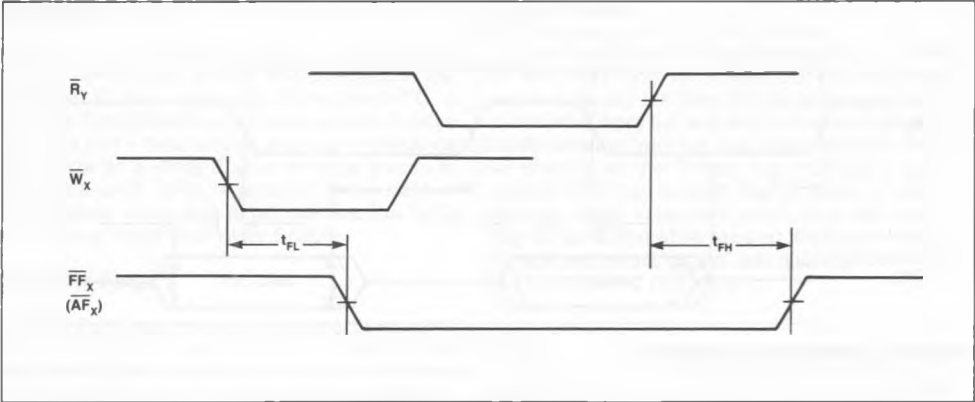


FIGURE 9. EMPTY (ALMOST EMPTY) FLAG TIMING

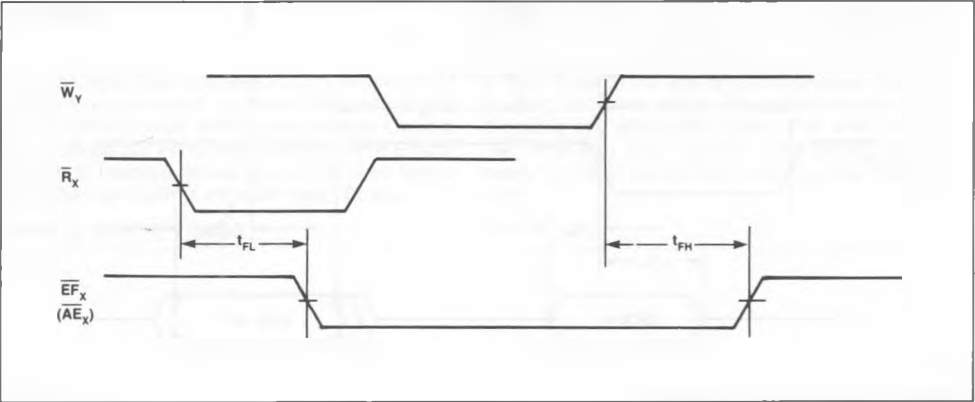


FIGURE 10. FIRST WRITE AFTER FULL TIMING

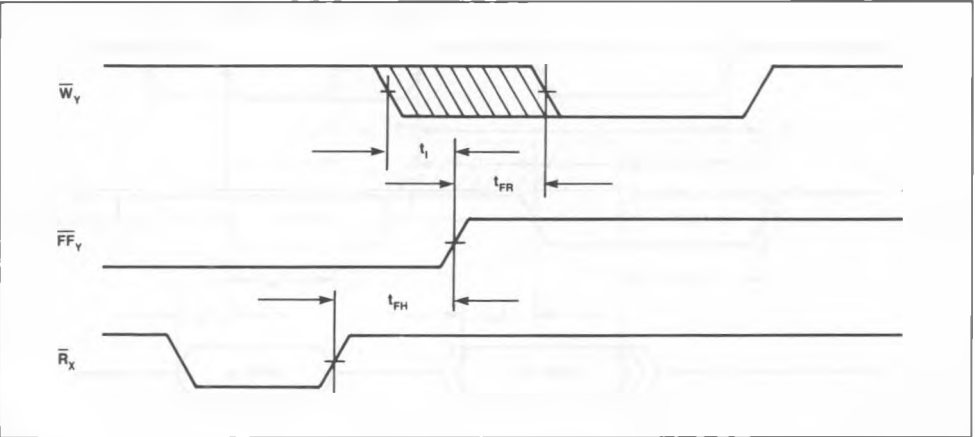


FIGURE 11. FIRST READ AFTER EMPTY TIMING

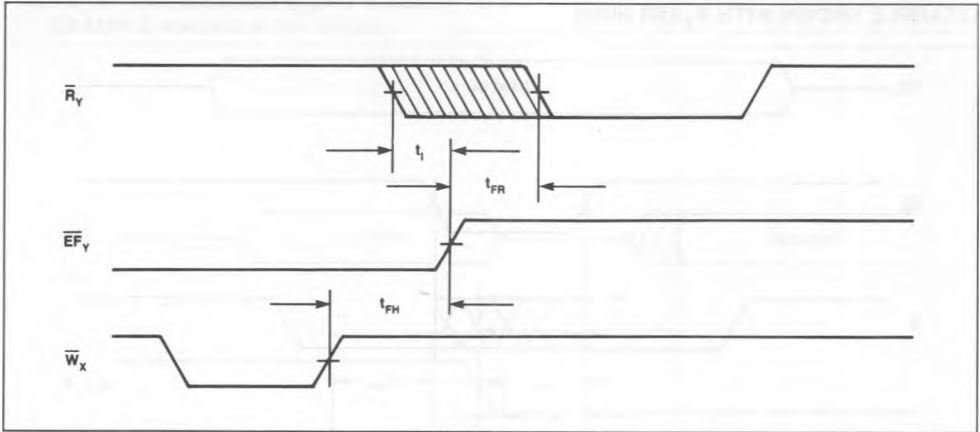


FIGURE 12. FIFO RESET TIMING

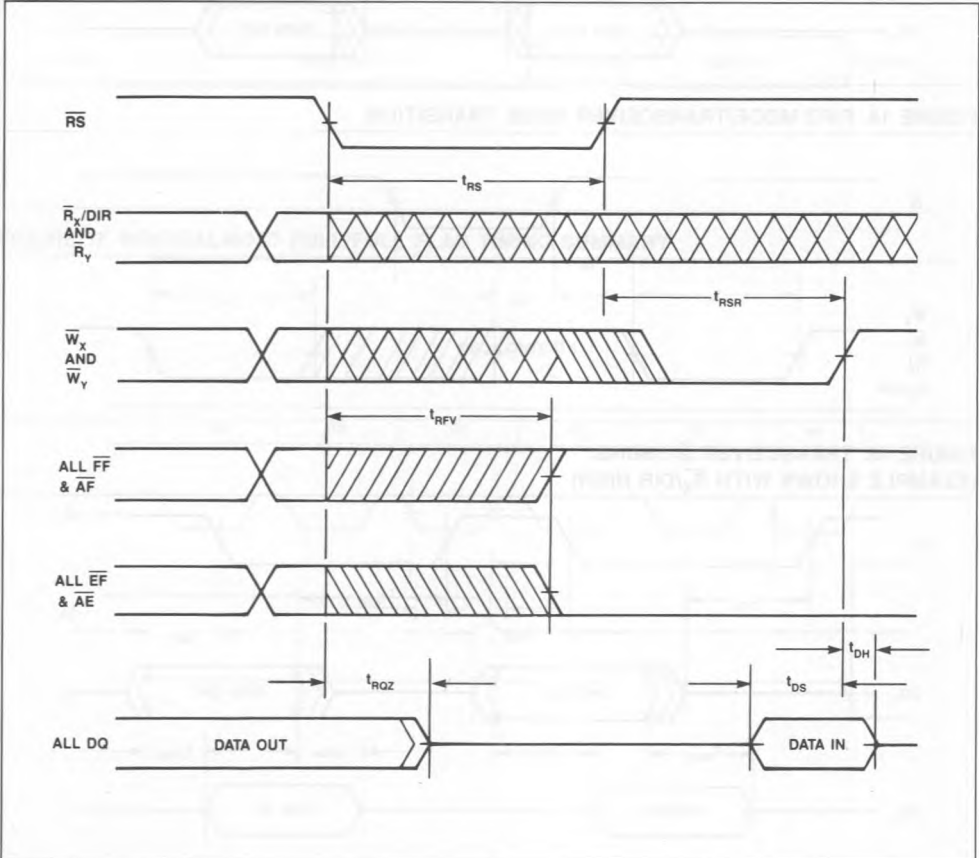


FIGURE 13. TRANSCEIVER RESET TIMING
(EXAMPLE SHOWN WITH $\overline{R}_X/\text{DIR}$ HIGH)

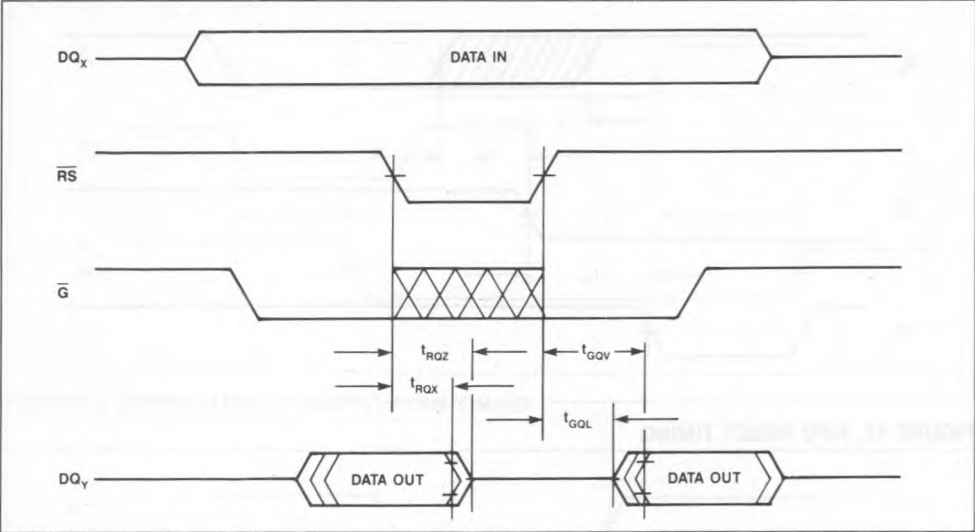


FIGURE 14. FIFO MODE/TRANSCEIVER MODE TRANSITION

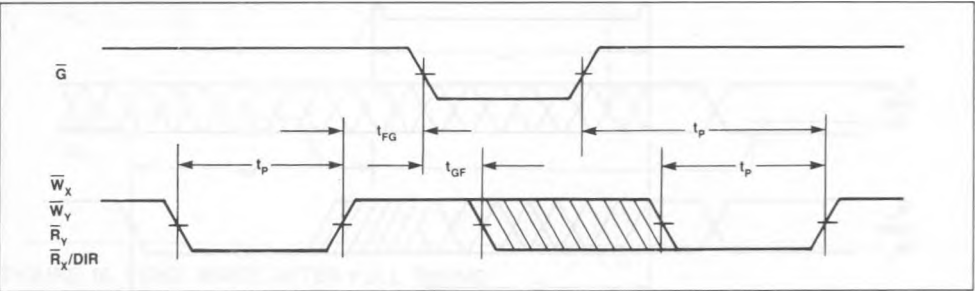


FIGURE 15. TRANSCEIVER $\overline{G}$ TIMING
(EXAMPLE SHOWN WITH $\overline{R}_X/\text{DIR}$ HIGH)

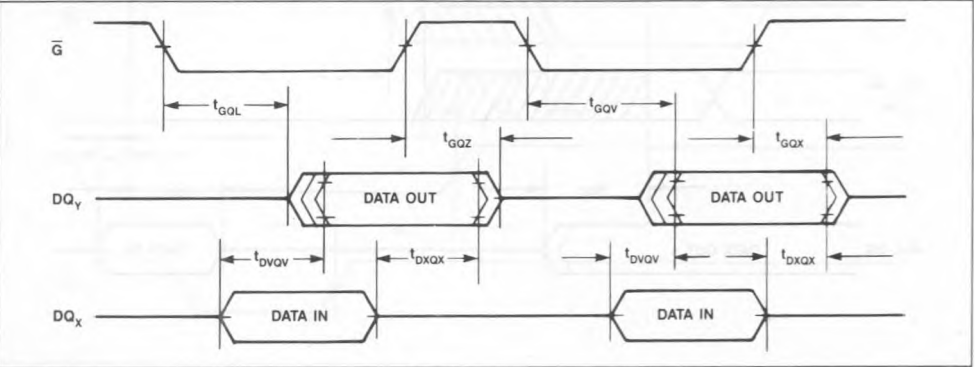


FIGURE 16. TRANSCEIVER $\overline{R}_X/\text{DIR}$ TIMING
(EXAMPLE SHOWN WITH $\overline{G}$ LOW)

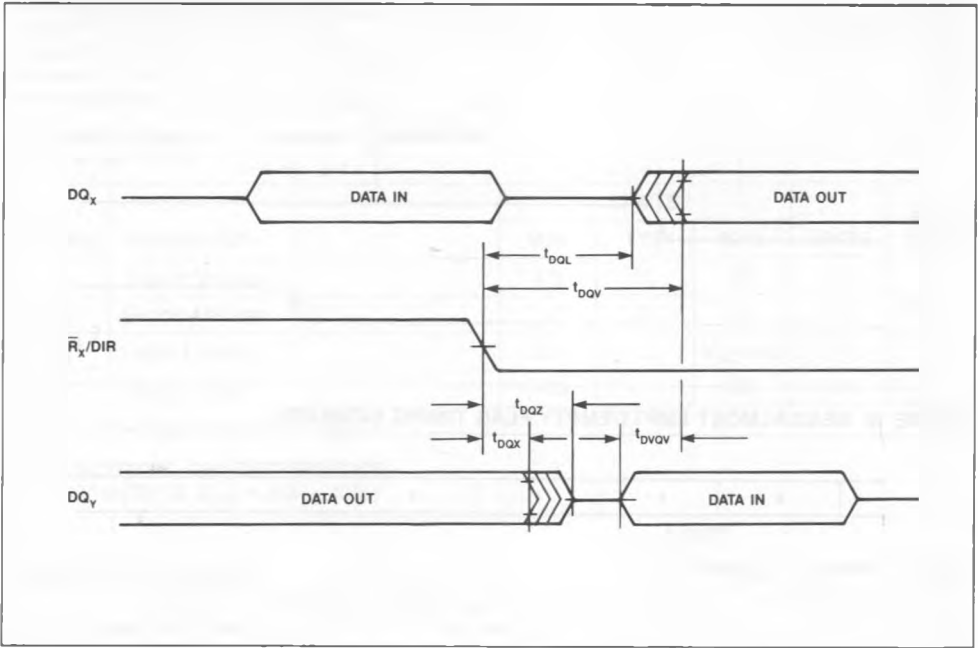


FIGURE 17. WRITE/ALMOST FULL/FULL FLAG TIMING SUMMARY

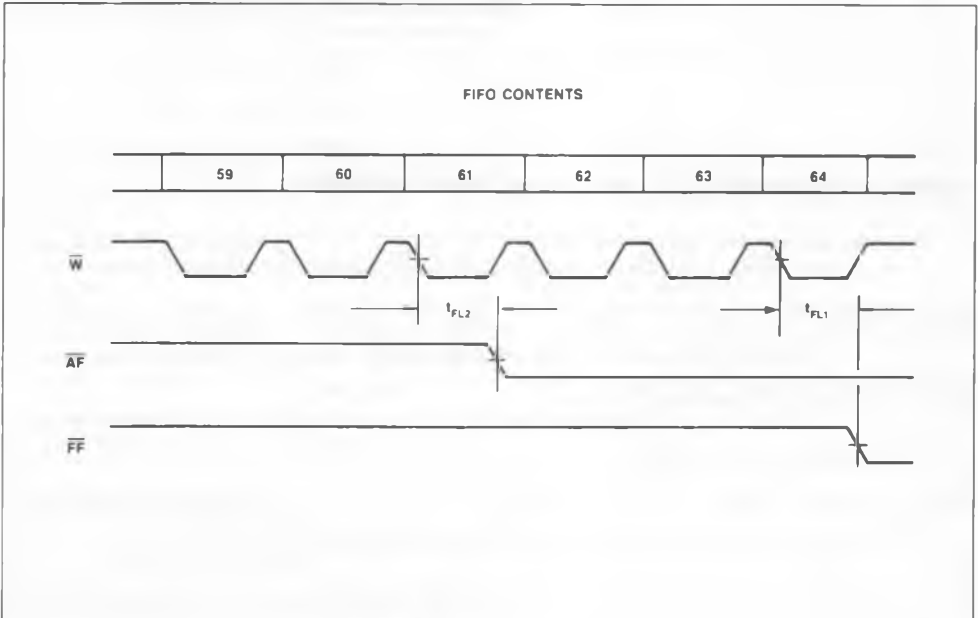


FIGURE 18. WRITE/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

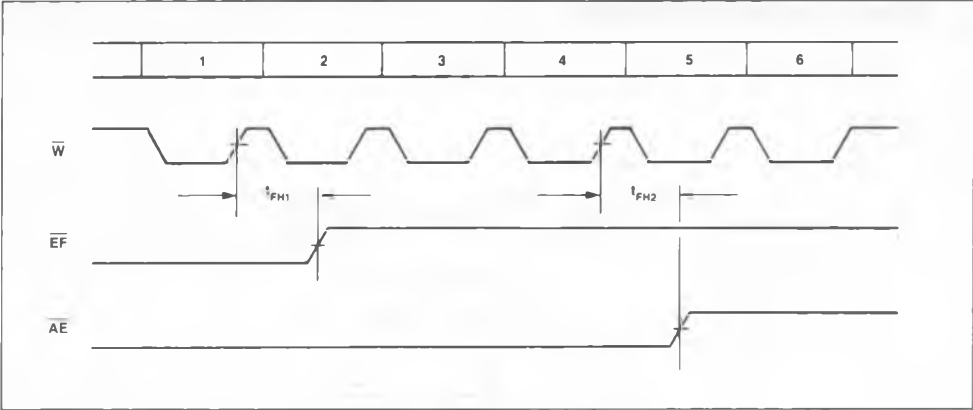


FIGURE 19. READ/ALMOST EMPTY/EMPTY FLAG TIMING SUMMARY

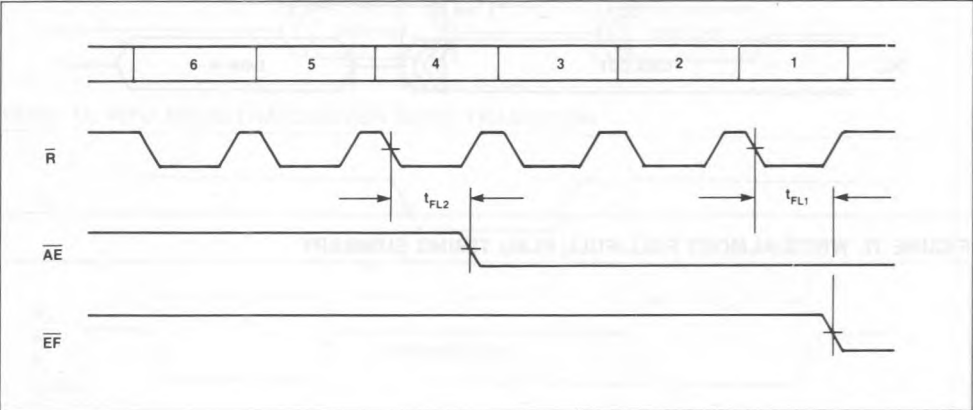
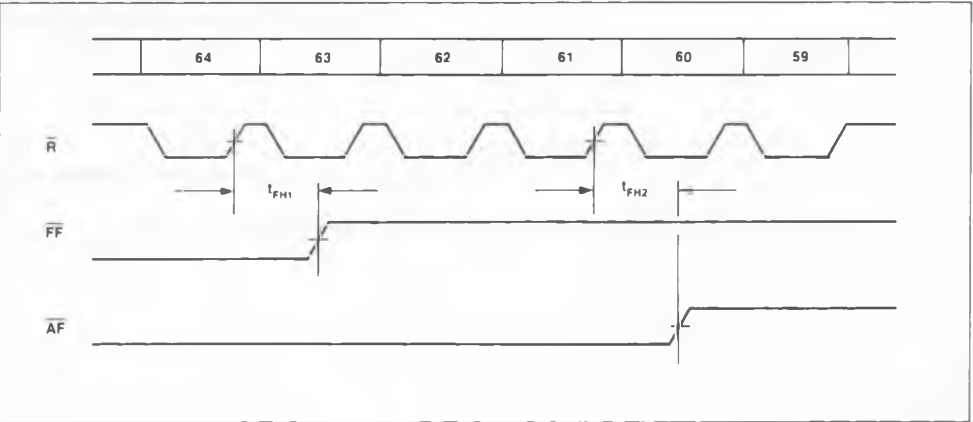


FIGURE 20. READ/ALMOST FULL/FULL FLAG TIMING SUMMARY



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	-1.5V to +7.0V
Ambient Operating Temperature (T_A)	0° to +70°C
Ambient Temperature under Bias	-55° to +125°C
Ambient Storage Temperature (Plastic)	-55° to +125°C
Allowable Total Device Power Dissipation	1 Watt
Allowable RMS Output Current per pin	80 mA

RECOMMENDED DC OPERATING CONDITIONS($T_A = 0^\circ$ to +70°C)

SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic 1 Input	2.2		$V_{CC} + 0.3$	V	1
V_{IL}	Logic 0 Input	-0.3		0.8	V	1

NOTE: 1. All voltages referenced to V_{SS} .**DC ELECTRICAL CHARACTERISTICS**($T_A = 0^\circ$ to 70° C, $V_{CC} = 5.0 \pm 10\%$)

SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
I_{CCQ}	Quiescent Power Supply Current, per Port			5	mA	1,2
I_{CCA}	Active Power Supply Current, per Port			10	mA	1,3
I_{CCD}	Dynamic Power Supply Current, per Port			1.2	mA/MHz	1,4
I_{CCT}	Total Power Supply Current, both Ports			60	mA	1,5
I_{IL}	Input Leakage Current	-1		+1	μ A	6
I_{OL}	Output Leakage Current	-10		+10	μ A	7
V_{OH}	Logic 1 Output Voltage	2.4			V	7,8
V_{OL}	Logic 0 Output Voltage			0.4	V	7,9

NOTES

- Measured with outputs open.
- Measured with opposite port quiescent; $\bar{R}$, $\bar{W}$ and $\bar{G} \geq V_{IH}$ (Min.).
- Measured with opposite port quiescent; $\bar{R}$ or $\bar{W} \leq V_{IL}$ (Max) and $\bar{G} \geq V_{IH}$ (Min.).
- Measured with opposite port quiescent; $\bar{R}$ or $\bar{W}$ toggling and $\bar{G} \geq V_{IH}$ (Min.).
- Measured with both ports operating at t_C (Min.).
- Measured with $V_{IN} = 0.0V$ to V_{CC} .
- All voltages referenced to V_{SS} .
- Data Output Pins (DQ_{X0} - DQ_{X4} and DQ_{Y0} - DQ_{Y4}) $I_{OUT} = -12mA$; Flag Output Pins EF_X , EF_Y , FF_X , FF_Y , AE_X , AE_Y , AF_X , AF_Y) $I_{OUT} = -1mA$.
- Data Outputs (DQ_{X0} - DQ_{X4} and DQ_{Y0} - DQ_{Y4}) $I_{OUT} = 12mA$; Flag Output Pins EF_X , EF_Y , FF_X , FF_Y , AE_X , AE_Y , AF_X , AF_Y) $I_{OUT} = 4mA$.

CAPACITANCE($T_A = 0^\circ$ to 70°C, $V_{CC} = 5.0 \pm 10\%$)

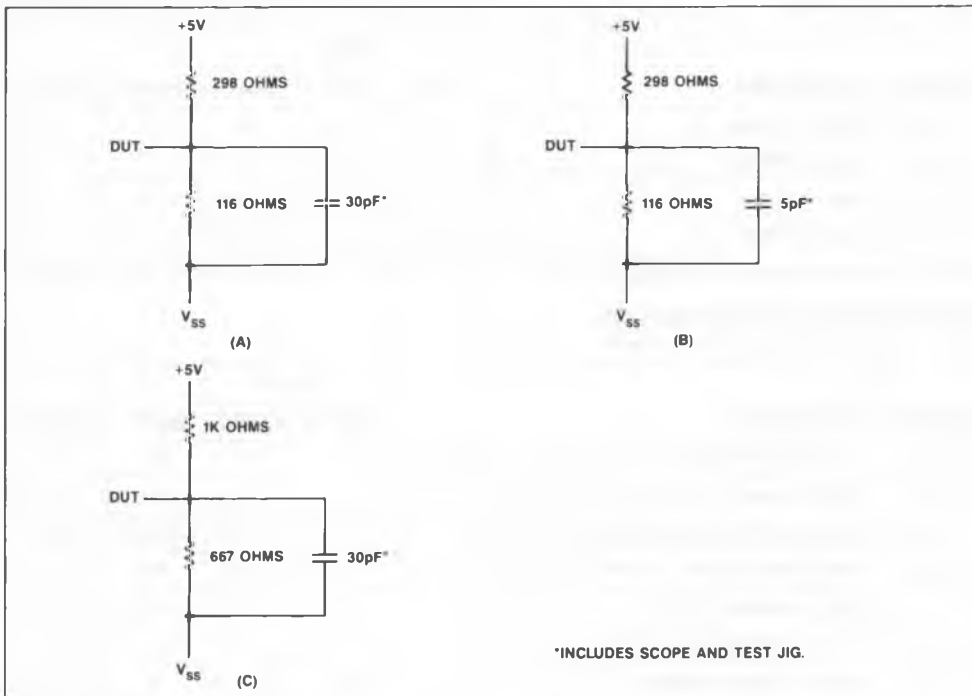
SYMBOL	PARAMETER	LIMITS			UNITS	NOTE
		MIN	TYP	MAX		
C_I	Input Capacitance		4	5	pf	1
C_O	Output Capacitance		8	10	pf	1

NOTE: 1. Sampled, not 100% tested. Measured at 1MHz.

AC TEST CONDITIONS

Input Levels	0 to 3 Volts
Transition Times	5 ns
Input and Output Reference Levels	1.5 Volts
Ambient Temperature	0° to 70 °C
$V_{CC} = 5.0 \text{ Volts} \pm 10\%$	

FIGURE 21. EQUIVALENT OUTPUT LOAD CIRCUIT



APPLICATION ISSUES

Width Expansion

The MK45264/65 is designed to be used in sets of two or more, as shown below. The MK45264/65 is supplied in two configurations, MK45264 and MK45265; the MK45264 having Empty and Full Flags, the MK45265 having Almost Empty and Almost Full Flags. This scheme allows a pair of devices to be connected in such a way as to assure that the PAIR present a full complement of status flags in BOTH directions, that is, both to the left and to the right.

The resulting 10 bit wide configuration allows both parity AND beginning or end of message flag bits

to be carried along with an 8 bit byte of data. The 20 bit wide configuration allows carrying 2 bits of parity AND separate message start and stop bits in 16 bit applications.

The MK45264/65 was designed as a 5 bit wide device in order to allow the use of a 300 mil DIP package; allowing the MK45264/65 to: a) achieve the highest function/board space ratio possible for a fully featured bidirectional BiPORT FIFO, b) provide higher performance with improved noise margins than would be possible in higher pin count packages, and c) provide greater flexibility to users of various bus widths.

FIGURE 22. (64x10)x2 WIDTH EXPANSION

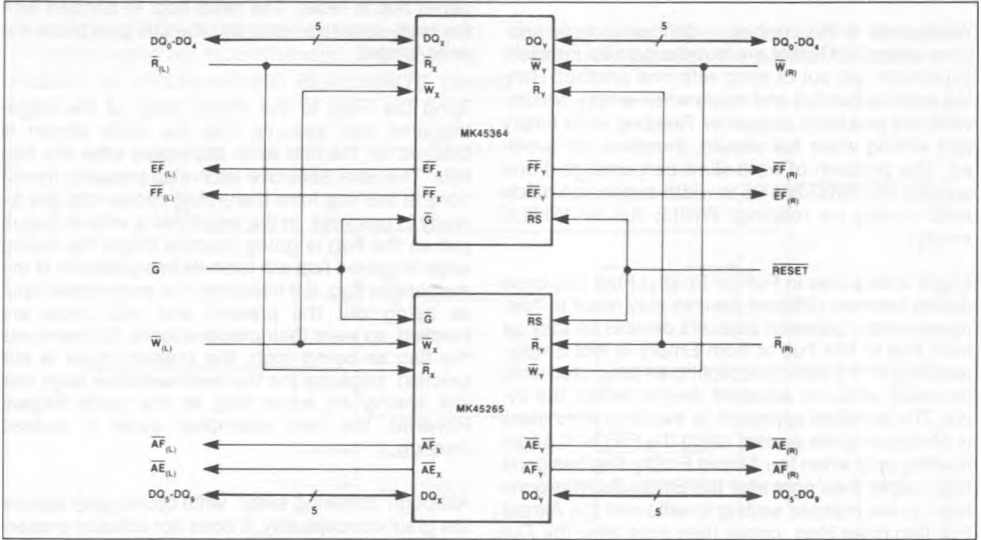
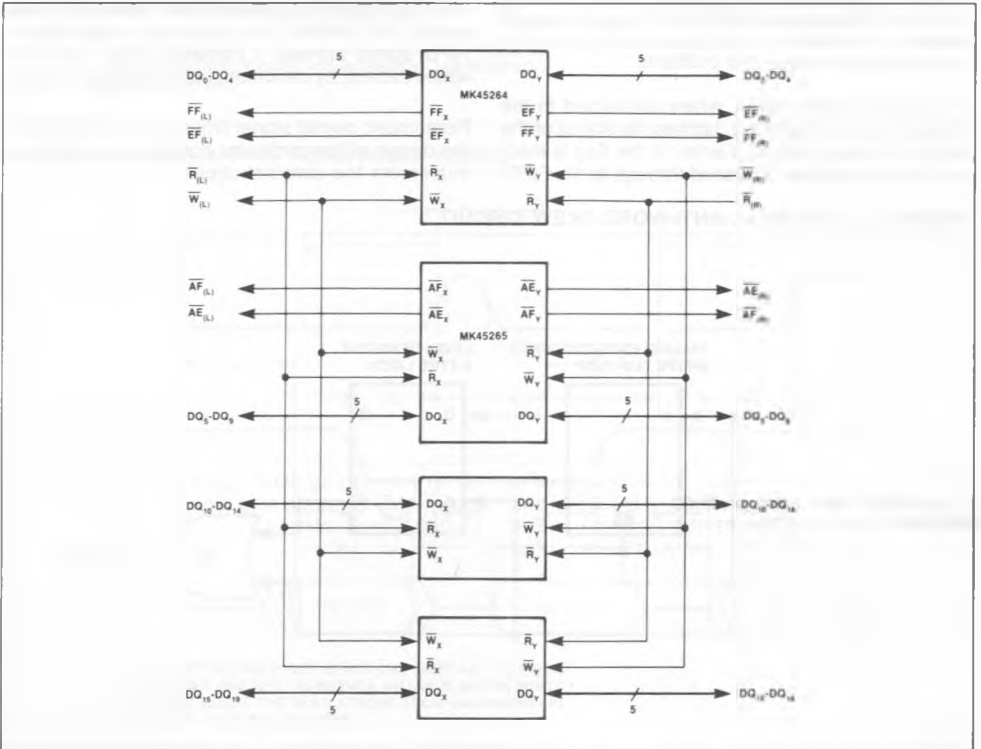


FIGURE 23. (64x20)x2 WIDTH EXPANSION



Width Expansion and Word-Skew

Word-skew, in this context, is defined as what happens when FIFOs that are wired in parallel for width expansion get out of sync with one another. Halting writes when full and reads when empty circumvents the problems altogether. Reading while empty and writing while full should, therefore, be avoided. The problem of word-skew can emerge if one is using the MK45264/65 in width expansion mode AND writing (or reading) WHILE full (or WHILE empty).

Slight differences in Full (or Empty) Flag response delays between different devices may result in "disagreements" between adjacent devices as they go from Full to Not Full or from Empty to Not Empty; resulting in one device accepting an attempted write (or read) while an adjacent device blocks the cycle. The simplest approach to avoiding word skew is configuring the system using the FIFOs to begin reading only when the Almost Empty flag has gone high, rather than right after the Empty flag has gone high. In like manner, waiting to write until the Almost Full flag goes high, rather than right after the Full flag goes high will prevent the problem, which is why the Almost flags are provided. However, should such a scheme prove unworkable in a particular application, the addition of an external flag latching circuit can also solve the problem.

The circuit shown below, when connected to the Write strobe and Full Flag, latches the status of the flag at the beginning of a write. If the flag is inactive, the Write strobe is passed through to the FIFO.

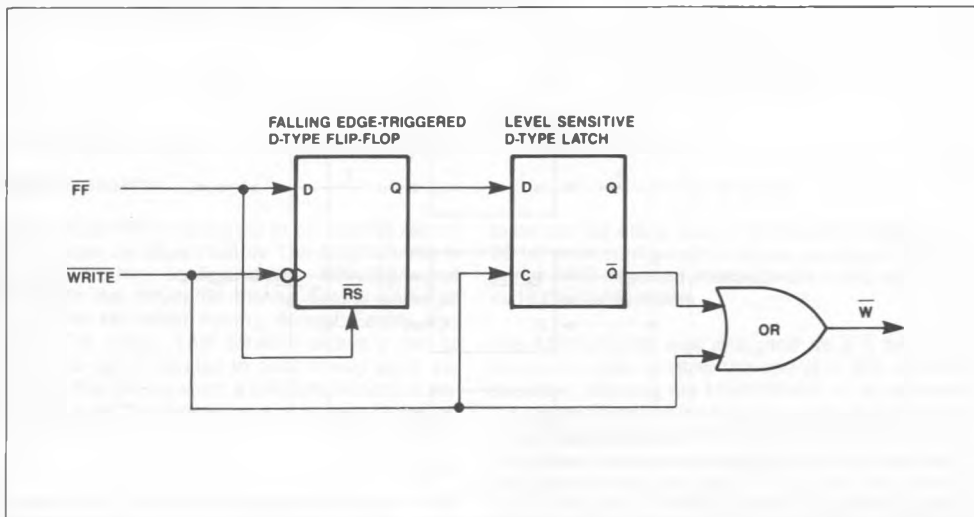
When the flag goes active (low) the falling-edge triggered flop is reset. The reset flop, in concert with the level-sensitive latch and the OR gate block the write strobe.

Tying the Flag to the Reset input of the edge-triggered flop assures that the Write strobe is blocked on the first write attempted after the flag falls. The level-sensitive latch also prevents transitions in the flag from disturbing cycles that are already in progress. In the event that a write is begun just as the flag is going inactive (high) the falling edge-triggered flop will latch its interpretation of the metastable flag. If it interprets the metastable input as being low, the present and next cycle are blocked, as were their predecessors. If it interprets the flag as being high, the present cycle is still blocked, because the level-sensitive latch was still seeing an active flag as the cycle began. However, the next attempted cycle is passed through.

Although "throwing away" write cycles goes against the grain conceptually, it does not actually present a problem in this situation. It must be assumed that Writing while Full or Reading while Empty would only be allowed in applications where the write and/or read strobes are proceeding regardless of FIFO status anyway. "Throwing away" reads or writes cannot, by definition, be considered an error.

Remember, overall signal timing must comprehend the delays of the particular components chosen to implement the external circuit.

FIGURE 24. EXTERNAL ANTI-WORD-SKEW CIRCUIT



Overlapping Read and Write Strokes

Overlapping Read and Write strobes on a given port is neither tested nor recommended. The following timing diagrams are provided only to illustrate the relationship between the control functions.

FIGURE 25. OVERLAPPING READ/WRITE TIMING

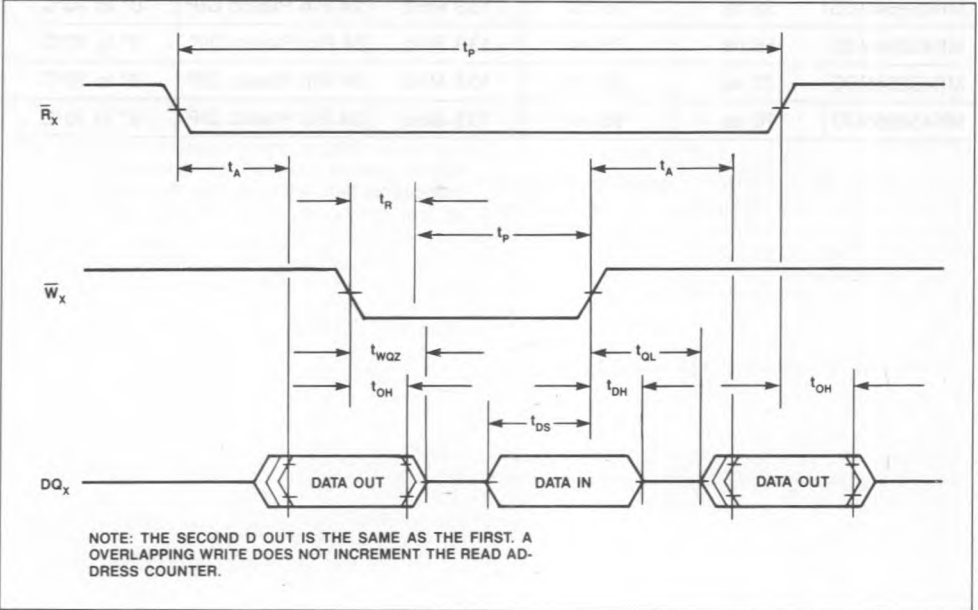
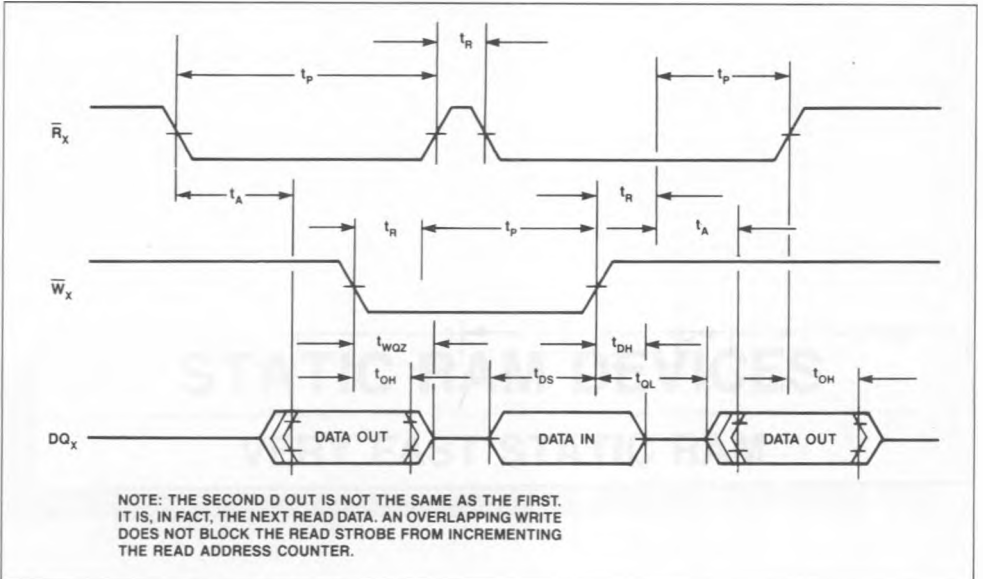


FIGURE 26. OVERLAPPING READ/WRITE TIMING



ORDERING INFORMATION

PART NO.	ACCESS TIME	R/W CYCLE TIME	CLOCK FREQ.	PACKAGE TYPE	TEMPERATURE RANGE
MK45264N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-55	55 ns	75 ns	13.3 MHz	24 Pin Plastic DIP	0° to 70°C
MK45264N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C
MK45265N-70	70 ns	95 ns	10.5 MHz	24 Pin Plastic DIP	0° to 70°C