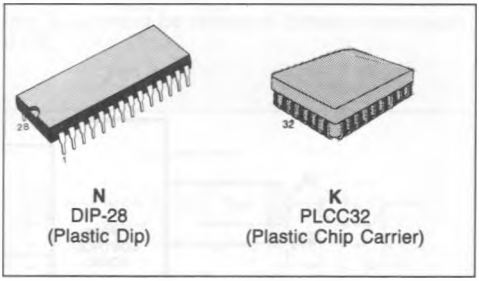
SGS-THOMSON MICROELECTRONICS

MK4511(N,K)-12/15/20

512 × 8 CMOS BiPORT™ RAM

- SINGLE CHIP BI-DIRECTIONAL MESSAGE PASSING
- SOFTWARE CONTROLLED INTERRUPT OUTPUTS
- ADDRESSABLE STATUS/CONTROL FLAGS
- IDENTICAL PORTS, 3-WIRE CONTROLLED I/O



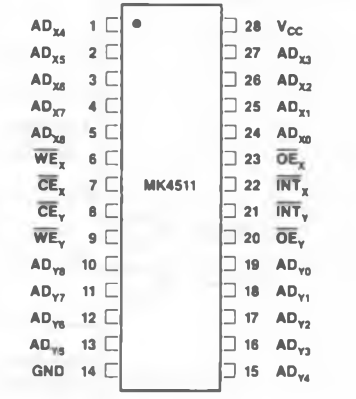
N
DIP-28
(Plastic Dip)

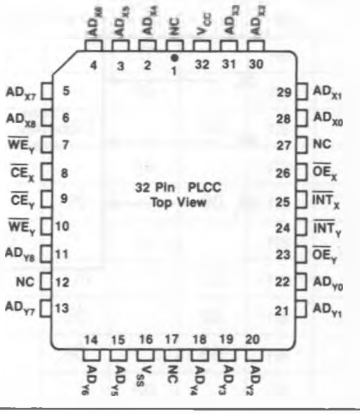
K
PLCC32
(Plastic Chip Carrier)

PIN NAMES

AD - Address/Data I/O	$\overline{INT}$ - Interrupt Output
$\overline{CE}$ - Chip Enable	GND - Ground
$\overline{OE}$ - Output Enable	V_{CC} - +5 Volts
$\overline{WE}$ - Write Enable	NC - No Connection

Part Number	Access Time	Cycle Time	Cycle Rate
MK4511-12	120 ns	150 ns	6.67 MHz
MK4511-15	150 ns	190 ns	5.26 MHz
MK4511-20	200 ns	250 ns	4.00 MHz





DESCRIPTION

The MK4511 dual port RAM contains a single 512 x 9 CMOS memory matrix that can be accessed simultaneously from both of the input/output ports. Dual port operation is achieved through the use of a memory array composed of BiPORT memory cells. Each memory cell is accessible from both ports at all times.

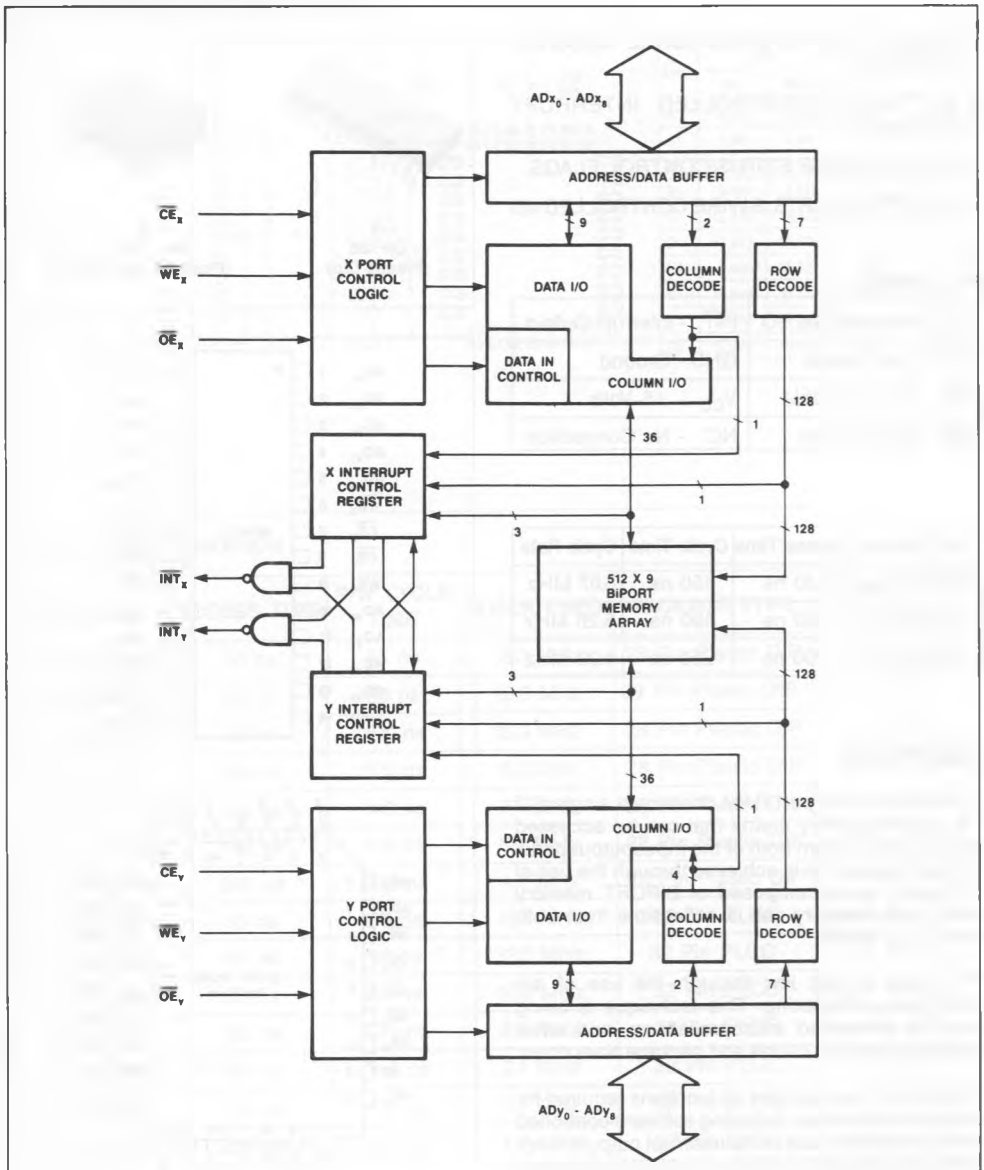
Pin count is kept low through the use of address/data multiplexing. This technique is being used on advanced microprocessors and other devices to keep pin counts and package sizes down.

The MK4511 incorporates all functions required for dual port operations, including software controlled interrupt outputs. Use of the interrupt outputs is optional, allowing both polled and interrupt controlled applications.

SINGLE PORT OPERATIONS

The MK4511 may be viewed from either port as an ordinary three wire controlled 512 x 9 static RAM. Timing of read and write operations is altogether conventional; the presence of the other port is effectively transparent to the accessing processor. Therefore, all timing parameters are specified without references that differentiate between the ports.

FIGURE 2. MK4511 BLOCK DIAGRAM

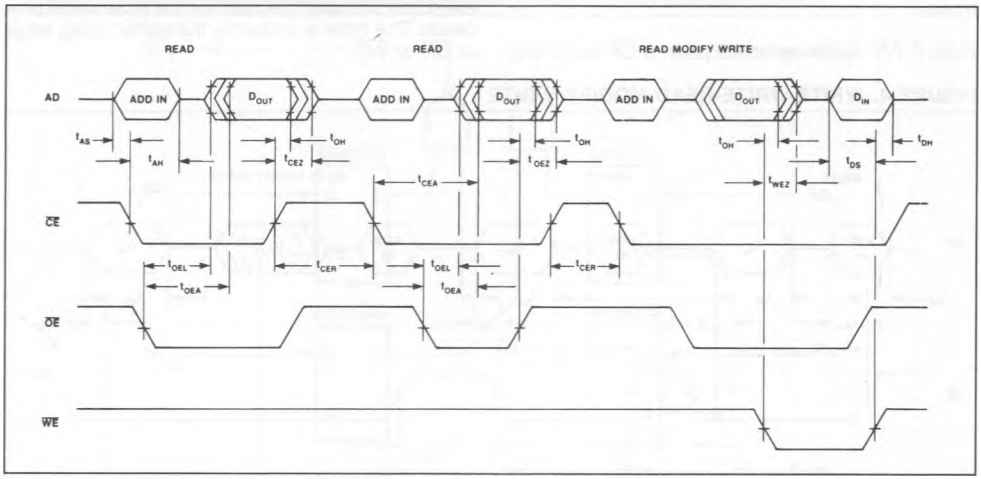


READ MODE

The MK4511 is in Read Mode whenever Chip Enable ($\overline{CE}$) is low and Write Enable ($\overline{WE}$) is high. A stable address must be placed onto the AD lines t_{AS} prior to Chip Enable becoming active. The address must be held valid for t_{AH} following the falling edge of $\overline{CE}$.

In Read Mode the bi-directional AD lines are driven alternately by the user and the MK4511. Bus contention will occur if the user's address driver remains active too long. An Output Enable input ($\overline{OE}$) is provided, offering an improved ability to avoid bus contention. The $\overline{OE}$ control keeps the AD lines in a high impedance state while held high and for t_{OEL} after it goes low. Output data will be valid at the latter of t_{OEA} or t_{CEA}. A Chip Enable recovery time (t_{CER}) must be observed between assertions of $\overline{CE}$.

FIGURE 3. READ-READ-READ MODIFY WRITE



READ CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	150		190		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{AH}	Address Hold Time	20		25		35		ns	
t_{CEA}	Chip Enable Access Time		120		150		200	ns	1
t_{OEL}	Output Enable to Lo-Z	15		15		15		ns	
t_{OEA}	Output Enable Access Time		55		70		90	ns	1
t_{OH}	Valid Data Out Hold Time	5		5		5		ns	1
t_{CEZ}	Chip Enable Hi to Hi-Z		90		110		150	ns	
t_{OEZ}	Output Enable Hi to Hi-Z		40		50		65	ns	
t_{WEZ}	Write Enable Lo to Hi-Z		40		50		65	ns	
t_{CER}	Chip Enable Recovery Time	30		40		50		ns	

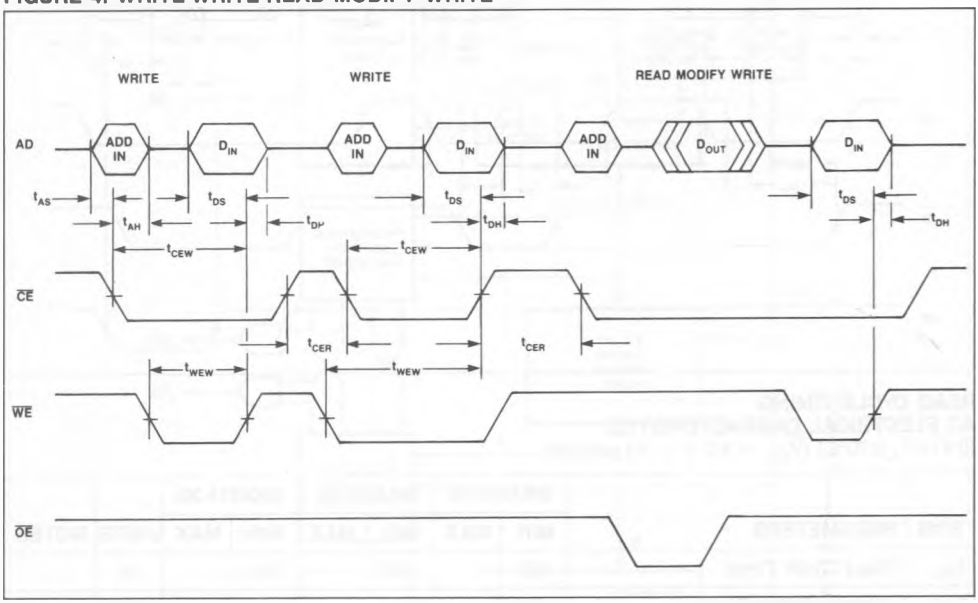
WRITE MODE

The MK4511 is in Write Mode whenever Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) are active low. As in Read Mode, the falling edge of $\overline{CE}$ latches the addresses present at the AD lines. The same addresses set-up and hold times apply. Input to the AD pins must then change from the address to input data. Input data present on the AD lines must be stable for t_{DS} prior to the end of write and must remain valid for t_{DH} afterward. A write cycle may be ended by the rising edge of $\overline{WE}$ or $\overline{CE}$. Chip Enable recovery time must also be observed in write mode.

Even if $\overline{WE}$ becomes active prior to $\overline{CE}$ becoming active, $\overline{CE}$ falling actually begins the cycle, latching the address present on the AD lines. Such cycles must reference t_{WEW}, t_{DS} and t_{DH} to the rising and falling edges of $\overline{CE}$ and $\overline{WE}$.

Read-Modify-Write cycles are possible if the outputs are enabled and the assertion of $\overline{WE}$ is delayed through t_{CEA}. The write cycle will begin when $\overline{WE}$ goes low. $\overline{WE}$ going low or $\overline{OE}$ going high will return the output drivers to high-Z within t_{WEZ} or t_{OEZ} respectively. The address latched when $\overline{CE}$ went low is still the valid address as the write cycle proceeds. The cycle is ended by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$.

FIGURE 4. WRITE-WRITE-READ MODIFY WRITE



WRITE CYCLE TIMING
AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WC}	Write Cycle Time	150		190		250		ns	
t_{CEW}	Chip Enable to End of Write	120		150		200		ns	
t_{WEW}	Write Enable to End of Write	80		105		130		ns	
t_{DS}	Data Setup Time	40		55		65		ns	
t_{DH}	Data Hold Time	10		10		10		ns	

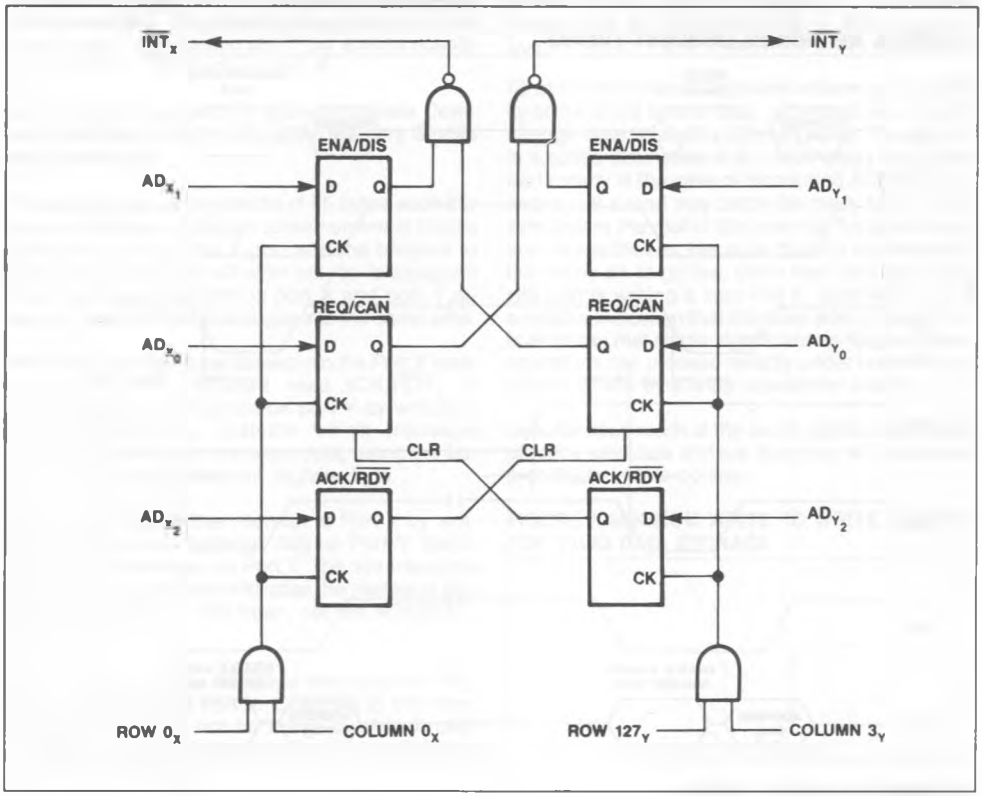
DUAL PORT OPERATIONS

INTERRUPT CONTROL

Although the Interrupt Control Registers for each port are accessed in parallel with RAM locations 000_H and $1FF_H$, they do not reside within the RAM array. They do not derive their control inputs from the RAM cells' status. In fact, changing the RAM location's contents via an opposite port will not affect a Interrupt Control Register at all. Therefore, for example, Port Y writing to address 000_H cannot affect the status of the Port X Interrupt Register.

The lower three bits of each byte written to the top and bottom addresses are the ones routed simultaneously to the Interrupt Control Registers. The Interrupt Control Registers consists of three flip-flops per port that serve as the Interrupt Request/Cancel flag (REQ/$\overline{CAN}$), Interrupt Output Enable/Disable flag (ENA/$\overline{DIS}$) and Interrupt Acknowledge/Ready flag (ACK/$\overline{RDY}$). As Figure 5 shows, the logic attached to the Interrupt Control Registers interprets interrupt status and drives the Interrupt Outputs.

FIGURE 5. MK4511 INTERRUPT CONTROL REGISTERS AND INTERRUPT LOGIC



INTERRUPT BYTE STRUCTURE

Because only the lower 3 bits of each interrupt byte are used to control the interrupt logic, the six MSBs written to the RAM have no affect on the state of the interrupt outputs, and may be used for any other purpose. The functions of the three control bits are:

Interrupt Output Enable/Disable ENA/$\overline{DIS}_X$ (AD_{X1}) and ENA/$\overline{DIS}_Y$ (AD_{Y1})

Each port can disable its own interrupt outputs by writing a 0 ($XXXXXXOX_2$) into its ENA/$\overline{DIS}$ bit. If disabled, the interrupt pin will remain high regardless of interrupt requests from the other port. If an interrupt is requested of a disabled port, and an enabling 1 is later written into ENA/$\overline{DIS}$ of the disabled port, the interrupt output will go low t_{WIL} following the rising edge of the enabling write. Disabling a port with an active interrupt output pin will result in the output going high t_{WIH} after the end of the disabling write.

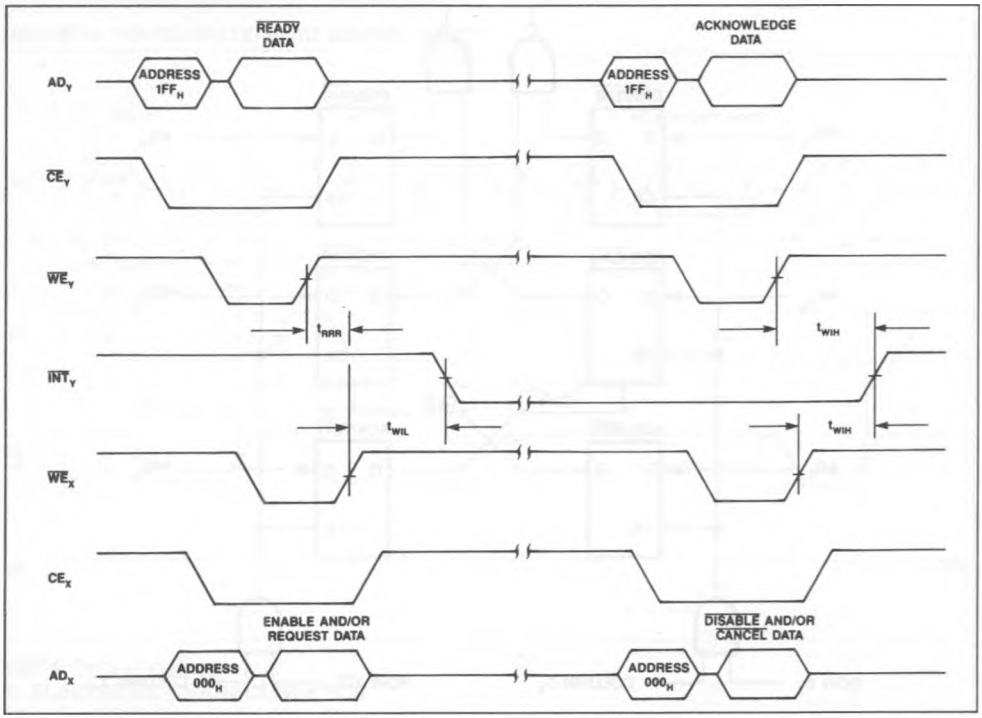
Interrupt Request/Cancel REQ/$\overline{CAN}_X$ (AD_{X0}) and REQ/$\overline{CAN}_Y$ (AD_{Y0})

Assuming that the Enable and Ready flags are set, writing a 1 into a REQ/$\overline{CAN}$ bit drives an enabled interrupt output pin on the opposite port low. The interrupt line will be driven low t_{WIL} following the end of the write that places a 1 in the REQ/$\overline{CAN}$ bit. For example, when $XXXXXXXX1_2$ is written into location 000_H setting REQ/$\overline{CAN}_X$, $\overline{INT}_Y$ will go active low within t_{WIL}. Writing a 0 into the REQ/$\overline{CAN}$ bit cancels the interrupt request, returning the $\overline{INT}$ output to a high state t_{WIH} after the end of write.

Interrupt Acknowledge/Ready ACK/$\overline{RDY}_X$ (AD_{X2}) and ACK/$\overline{RDY}_Y$ (AD_{Y2})

Once an interrupt has been received at a port, the interrupt can be turned off by writing a 1 ($XXXXXX1XX_2$) into the ACK/$\overline{RDY}$ bit of the receiving port. Writing an acknowledge will cause the interrupt output to go high t_{WIH} after the end of the write. The interrupt request flag cannot be set while the acknowledge flag is active. An acknowledge must always be followed with a ready (writing a 0 over the 1) before requests from the other port can be recognized. Interrupt requests can be recognized t_{RRR} after a ready.

FIGURE 6. INTERRUPT REQUEST TIMING



INTERRUPT OUTPUT TIMING AC ELECTRICAL CHARACTERISTICS

($0°C \le T_A \le 70°C$) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{WIL}	End of Write to $\overline{INT}$ Low		50		60		85	ns	
t_{WIH}	End of Write to $\overline{INT}$ High		50		60		85	ns	
t_{RRR}	Ready to Request Recognized		10		10		15	ns	

IMPLEMENTATION

Use of the interrupt feature is completely optional, allowing simple implementation of either interrupt driven or polled inter-processor communications applications. Either port can read or write any of the 512 bytes without restriction. Users who choose not to utilize the interrupt feature should leave the interrupt pins unconnected.

Any inter-processor communications application will doubtless employ some type of semaphore scheme. The use of the REQ/$\overline{CAN}$, ENA/$\overline{DIS}$ and ACK/$\overline{RDY}$ bits allow for each port to follow the exact status of the other port. The following example covers the case of port X interrupting port Y but applies equally well for port Y interrupting port X.

An Example Approach to Inter-processor Communications Using Pre-Allocated Memory Blocks and Interrupts

Pre-define six memory blocks of 85 bytes each (for a total of 510 bytes). Assign some number of blocks (probably three) to the X port and the balance to the Y port. Each port will write only to its assigned memory blocks, preventing port X and port Y attempting to load their messages into the same area.

Write the message to be passed into the Port X message area. When finished, read ACK/$\overline{RDY}_Y$. If ready, request an interrupt on port Y by writing a 1 into REQ/$\overline{CAN}_X$. Indicate which message block(s) contain valid message data, using the upper six bits of the interrupt register byte.

Now, acknowledge the interrupt to Port Y by writing a 1 to the acknowledge flag on Port Y. Begin reading the message via Port Y. The acknowledge should not be removed until after the message has been read. When it has been, set the ACK/$\overline{RDY}_Y$ flag to ready.

Check to see that the message was received. Monitor ACK/$\overline{RDY}_Y$ via Port X. Changes to the message block should not be made by Port X until ACK/$\overline{RDY}_Y$ is zero, indicating Port Y has finished reading its message.

COLLISION

The central objective of the MK4511 design effort was to produce a component that makes implementation of asynchronous, random access dual port memory applications, that can assure data integrity, as simple and inexpensive to design and implement as possible.

Data integrity can be called into question if port to port collision occurs. A collision is defined as both ports attempting to write at the same address or one port reading and one writing at the same address at the same time.

While a collision is generally considered undesirable, the conditions that can lead to ill-defined results are definable and manageable. In the case of a write/write collision, the data stored at the address in question may or may not have any similarity to either write attempted or the previously resident data if the delay between the ends of the writes (t_{WWL})is not long enough. On the other hand, write/read collisions do not affect the integrity of data storage, but do have an impact on the validity of output data at definable points in time (t_{ODI} and t_{ODV}). Figures 7 and 8 describe these conditions.

All of the parameters indicated reference the validity of the entire byte of data. Individual bits of a byte change state at slightly different rates. Though this is a subtle distinction, it is nonetheless important, particularly in the case of monitoring ACK/$\overline{RDY}$. Be aware that a read may catch the ready bit at a valid zero before the rest of the byte has finished transition. Nevertheless, because there is no reason for the ready bit to go low, other than that the opposite port is writing a zero into it, catching it low is a reliable indication that the other port is ready. This is all to say that single significant bit flag write/read operations can proceed reliably under collision conditions where byte wide operations cannot.

Simultaneous reads at the same address will always produce valid data and are therefore not considered a collision in this context.

FIGURE 7. MINIMUM WRITE TO WRITE LATENCY FOR VALID DATA STORAGE

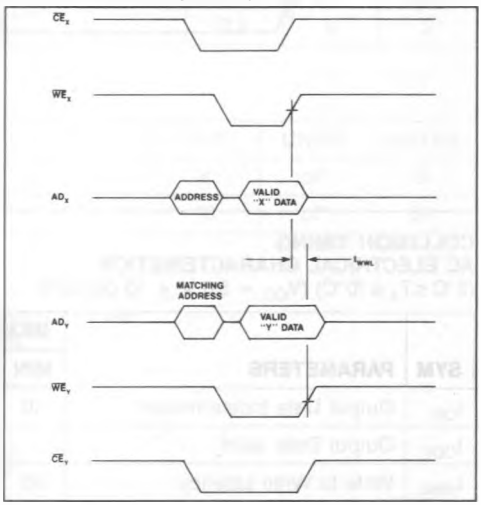
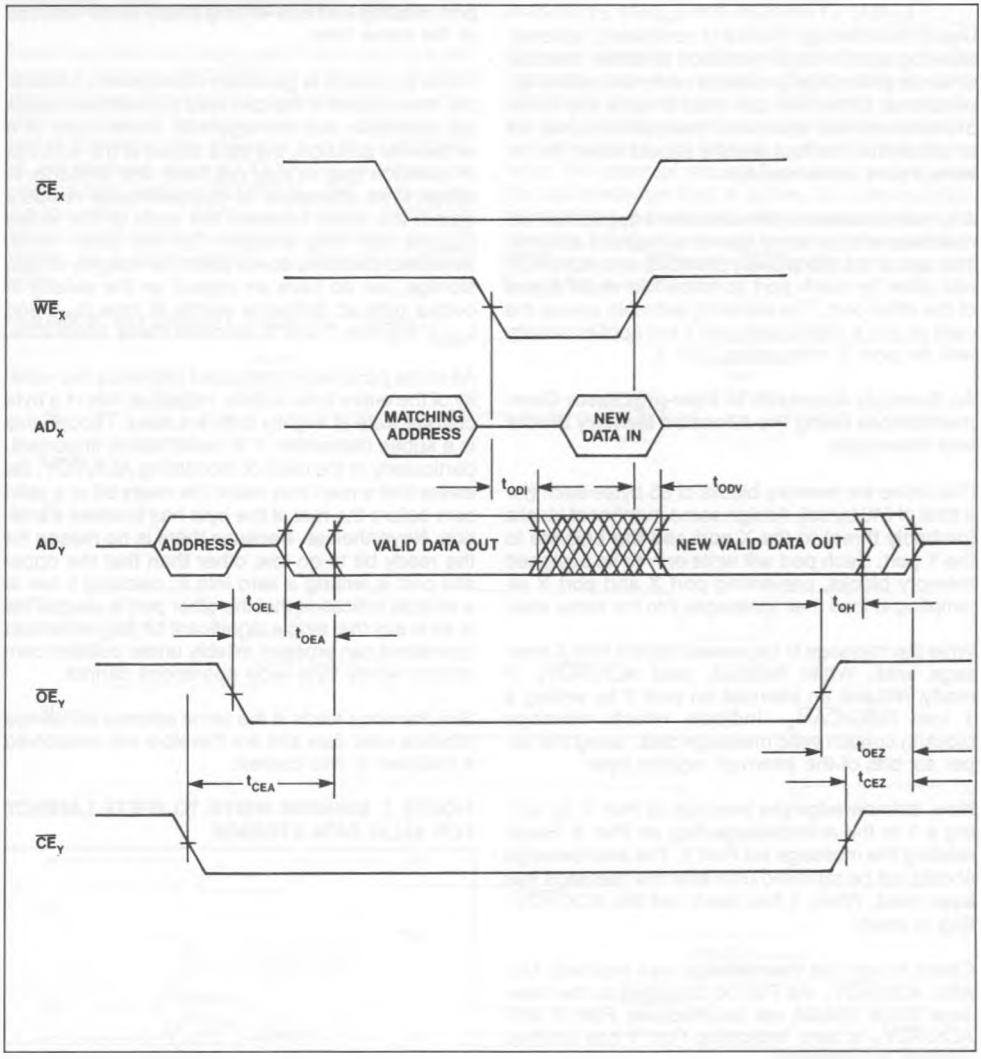


FIGURE 8. SIMULTANEOUS READ WRITE TIMING



COLLISION TIMING
AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MK4511-12		MK4511-15		MK4511-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{ODI}	Output Data Indeterminant	10		10		10		ns	
t_{ODV}	Output Data Valid		90		115		150	ns	
t_{WWL}	Write to Write Latency	80		105		130		ns	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND . . . . . −0.3 V to +7.0 V
Ambient Operating Temperature (T_A) . . . . . 0°C to +70°C
Ambient Storage Temperature . . . . . −55°C to +125°C
Total Device Power Dissipation . . . . . 1 Watt
Output Current per Pin . . . . . 20 mA

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETERS	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
GND	Supply Voltage	0	0	0	V	
V_{IH}	Logic 1 Voltage, All Inputs	2.2		V_{CC} + 0.3	V	2,3
V_{IL}	Logic 0 Voltage, All Inputs	−0.3		0.8	V	2,3

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10 percent)

SYM	PARAMETERS	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Power Supply Current per Port		25	mA	4
I_{CC2}	TTL Standby Current per Port		2.5	mA	5
I_{CC3}	CMOS Standby Current per Port		1	mA	6
I_{IL}	Input Leakage Current	−1	+1	μA	7
I_{OL}	Output Leakage Current (Any Output Pin)	−5	+5	μA	7
V_{OH}	Output Logic 1 Voltage (I_{OUT} = −1 mA)	2.4		V	2
V_{OL}	Output Logic 0 Voltage (I_{OUT} = 2.1 mA)		0.4	V	2

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz)

SYM	PARAMETERS	TYP	UNITS	NOTES
C_I	Capacitance on any Input Pin	4	pF	8
C_O	Capacitance on any Output Pin	10	pF	8,9

NOTES

1. Measured with load shown in Figure 9.
2. All voltages referenced to GND.
3. No more than one negative undershoot or positive overshoot of 1.5 V with a maximum pulse width of 10 ns is allowed once per cycle.
4. Output buffer is deselected, both ports are active.
5. All inputs = V_{IH}.
6. All inputs ≥ V_{CC} − 0.2V
7. Measured with GND ≤ V_I ≤ V_{CC} and outputs deselected.
8. Effective capacitance is calculated as follows: $C = \frac{\Delta Q}{\Delta V}$ ΔV = 3 V
9. Output buffer is deselected.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Times	5 ns
Input Signal Timing Reference Level	1.5 V
Output Signal Timing Reference Levels	0.8 V and 2.2 V
Ambient Temperature	0°C to 70°C
V_{CC}	5.0 V ± 10 percent

FIGURE 9. EQUIVALENT OUTPUT LOAD CIRCUIT

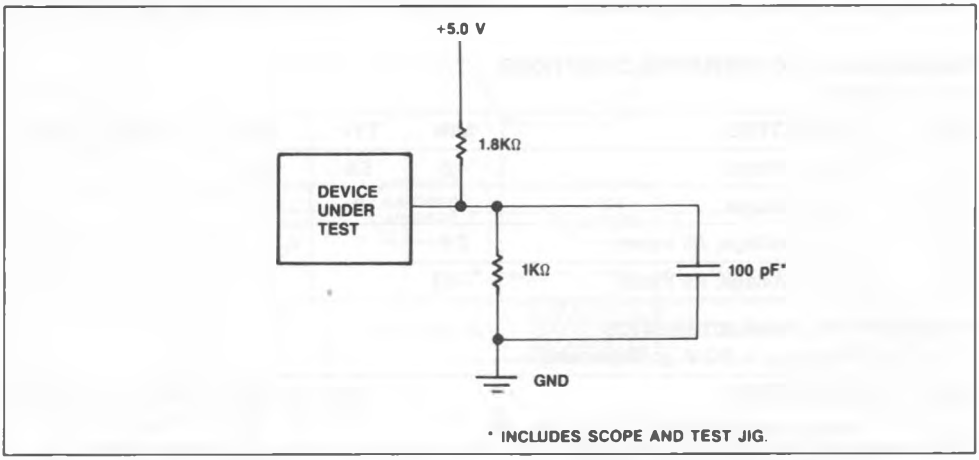
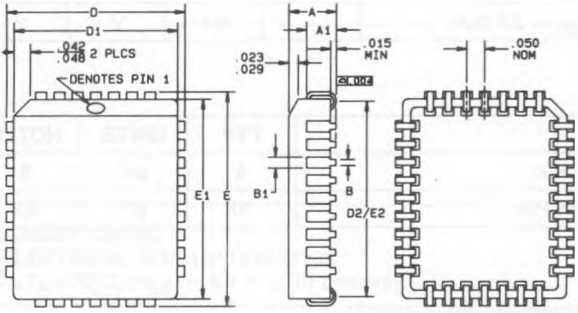
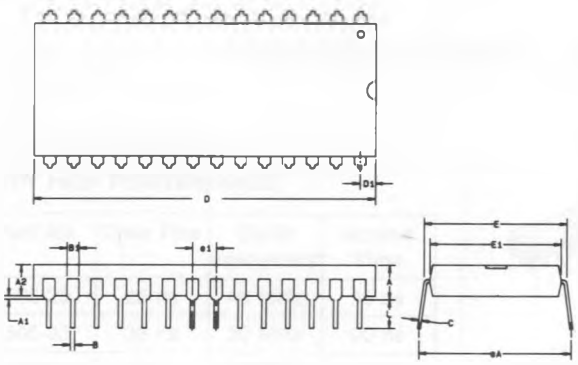


FIGURE 10. MK4511 PLASTIC LEADED CHIP CARRIER, 32 PIN (K TYPE)



Dim.	mm		inches	
	Min	Max	Min	Max
A	3.048	3.556	.120	.140
A1	1.981	2.413	.078	.095
B	0.330	0.533	.013	.021
B1	0.660	0.812	.026	.032
D	12.319	12.573	.485	.495
D1	11.353	11.506	.447	.453
D2	9.906	10.922	.390	.430
E	14.859	15.113	.585	.595
E1	13.893	14.046	.547	.553
E2	12.446	13.462	.490	.530

FIGURE 11. MK4511 28 PIN PLASTIC DIP (N TYPE)



Dim.	mm		inches		Notes
	Min	Max	Min	Max	
A	—	5.334	—	.210	2
A1	0.381	—	.015	—	2
A2	3.556	4.064	.140	.160	
B	0.381	0.533	.015	.021	3
B1	1.27	1.778	.050	.070	
C	0.203	0.304	.008	.012	3
D	36.576	37.338	1.440	1.470	1
D1	1.651	2.159	.065	.085	
E	15.24	15.875	.600	.625	
E1	13.462	14.224	.530	.560	
e1	2.286	2.794	.090	.110	
eA	15.24	17.78	.600	.700	
L	3.048	—	.120	—	

NOTES

1. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
2. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
3. THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN. WHEN SOLDER LEAD FINISH IS SPECIFIED.

ORDERING INFORMATION

MK4511 — X — −XX — _____

ROOT PART NUMBER | PACKAGE | SPEED | TEMP RANGE

BLANK 0° TO 70°C

-12 120 NS ACCESS TIME
-15 150 NS ACCESS TIME
-20 200 NS ACCESS TIME

N 28 PIN DIP
K 32 PIN PLCC