

### **FEATURES**

Combination static storage cells and dynamic control circuitry for truly high performance

| PART NUMBER  | ACCESS TIME | CYCLE TIME |
|--------------|-------------|------------|
| MK4104-3/-33 | 200ns       | 310ns      |
| MK4104-4/-34 | 250ns       | 385ns      |
| MK4104-5/-35 | 300ns       | 460ns      |
| MK4104-6     | 350ns       | 535ns      |

- □ Low Active Power Dissipation: 150mW (Max)
- Battery backup mode (3V/10mW on -33, -34 and -35)

### DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static\_the device may be stopped indefinitely with the CE clock in the off (Logic 1) state.

All input levels, including write enable ( $\overline{WE}$ ) and chip enable ( $\overline{CE}$ ) are TTL compatible with a one level of

#### FUNCTIONAL DIAGRAM

- □ Standby Power Dissipation less than 28 mW (at V<sub>CC</sub> = 5.5V)
- $\Box$  Single +5V Power Supply ( ± 10% tolerance)
- Fully TTL Compatible
  Fanout: 2 Standard TTL
  - 2 Schottky TTL
    - 12 Low Power Schottky TTL
- Standard 18-pin DIP
- MKB version screened to MIL-STD-883

2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils ( $\frac{1}{2}$  the area of previous cells) and dissipates power levels comparable

**PIN CONNECTIONS** 



### **ABSOLUTE MAXIMUM RATINGS\***

| Voltage on any pin relative to VSS      | –1.0V to +7. <b>0</b> V |
|---|-------------------------|
| Operating Temperature TA (Ambient)      | 0° C to + 70° C         |
| Storage Temperature (Ambient) (Ceramic) | –65°C to +150°C         |
| Storage Temperature (Ambient) (Plastic) | –55° C to +125° C       |
| Power Dissipation                       | 1 Watt                  |
| Short Circuit Output Current            |                         |

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

# **RECOMMENDED DC OPERATING CONDITIONS<sup>6</sup>**

# $(0^{\circ} C \le T_{A} \le + 70^{\circ} C)$

|     | PADAMETED                    | MK4  | 104 S | LINITS | NOTES |       |  |
|-----|------------------------------|------|-------|--------|-------|-------|--|
|     | FARAMETER                    | MIN  | TYP   | MAX    | UNITS | 10123 |  |
| VCC | Supply Voltage               | 4.5  | 5.0   | 5.5    | Volts | 1     |  |
| VSS | Supply Voltage               | 0    | 0     | 0      | Volts | 1     |  |
| νін | Logic "1" Voltage All Inputs | 2.2  |       | 7.0    | Volts | 1     |  |
| VIL | Logic "0" Voltage All Inputs | -1.0 |       | .8     | Volts | 1     |  |

# DC ELECTRICAL CHARACTERISTICS<sup>1</sup>

 $(0^{\circ}C \le T_A \le + 70^{\circ}C) (V_{CC} = 5.0 \text{ volts} \pm 10\%)$ 

|      | PARAMETER                                    | MIN | MAX | UNITS | NOTES |
|------|--|-----|-----|-------|-------|
|      | Average VCC Power Supply Current             |     | 27  | mA    | 2     |
| ICC2 | Standby V <sub>CC</sub> Power Supply Current |     | 5   | mA    | 3     |
| ΊL   | Input Leakage Current (Any Input)            | 10  | 10  | μA    | 4     |
| IOL  | Output Leakage Current                       | -10 | 10  | μA    | 3, 5  |
| √он  | Output Logic "1" Voltage IOUT=-500µA         | 2.4 |     | Volts |       |
| VOL  | Output Logic "0" Voltage IOUT= 5mA           |     | 0.4 | Volts |       |

# AC ELECTRICAL CHARACTERISTICS<sup>1</sup>

 $(0^{\circ} C \le T_{A} \le +70^{\circ} C) (V_{CC} = +5.0 \text{ volts } \pm 10\%)$ 

|                | PARAMETER          | ТҮР | MAX | NOTES |
|----------------|--------------------|-----|-----|-------|
| Cı             | Input Capacitance  | 4pF | 6pF | 14    |
| C <sub>0</sub> | Output Capacitance | 6pF | 7pF | 14    |

NOTES:

- 1. All voltages referenced to V<sub>SS</sub>.
- I<sub>CC1</sub> is related to precharge and cycle times. Guaranteed maximum values for I<sub>CC1</sub> may be calculated by: Locs (mod 2) = (5: + 15(4), + 15(4)) = (4)

 $I_{CC1}$  [ma] = (5t<sub>p</sub> + 15(t<sub>C</sub> - t<sub>p</sub>) + 4720) ÷ t<sub>C</sub> where t<sub>p</sub> and t<sub>C</sub> are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve. Data outputs open.

- 3. Output is disabled (open circuit), CE is at logic 1.
- 4. All device pins at 0 volts except pin under test at 0  $\leqslant$  V  $_{IN}$   $\leqslant$  5.5 volts. (V\_{cc} = 5V)
- 5. 0V≤V<sub>OUT</sub>≤+ 5.5V. (V<sub>cc</sub> = 5V)
- During power up, CE and WE must be at V<sub>IH</sub> for minimum of 2ms after V<sub>CC</sub> reaches 4.5V, before a valid memory cycle can be accomplished.
- 7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

- If WE follows CE by more than t<sub>WS</sub> then data out may not remain open circuited.
- 9. Determined by user. Total cycle time cannot exceed t<sub>CE</sub> max.
- 10. Data-in set-up time is referenced to the later of the two falling clock edges CE or WE.
- 11. AC measurements assume  $t_T = 5ns$ . Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
- 12.  $t_{C} = t_{CE} + t_{P} + 2t_{T}$ .
- 13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output isguaranteed to be open circuit within t<sub>OFF</sub>.
- 14. Effective capacitance calculated from the equation C =  $I \frac{\Delta t}{\Delta v}$  with  $\Delta V$  equal to 3V and V<sub>CC</sub> nominal.
- 15.  $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$

# AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS6.11 (0° C< $T_A \le +70^\circ$ C) (V<sub>CC</sub> = + 5.0 volts ± 10%)<sup>1</sup>

|                  |                              | MK4 | 104-3/33 | MK41 | 04-4/34 | MK41 | 04-5/35 | MK4 | 104-6  |       |       |
|------------------|------------------------------|-----|----------|------|---------|------|---------|-----|--------|-------|-------|
| SYMBOL           | PARAMETER                    | MIN | MAX      | MIN  | MAX     | MIN  | MAX     | MIN | MAX    | UNITS | NOTES |
| tC               | Read or Write Cycle Time     | 310 |          | 385  |         | 460  |         | 535 |        | ns    | 12    |
| tAC              | Random Access                |     | 200      |      | 250     |      | 300     |     | 350    |       | 7     |
| <sup>t</sup> CE  | Chip Enable Pulse Width      | 200 | 10,000   | 250  | 10,000  | 300  | 10,000  | 350 | 10,000 |       |       |
| tp               | Chip Enable Precharge Time   | 100 |          | 125  |         | 150  |         | 175 |        |       |       |
| <b>t</b> AH      | Address Hold Time            | 110 |          | 135  |         | 165  |         | 190 |        |       |       |
| tAS              | Address Set-Up Time          | 0   |          | 0    |         | 0    |         | 0   |        |       |       |
| tOFF             | Output Buffer Turn-Off Delay | 0   | 50       | 0    | 65      | 0    | 75      | 0   | 100    |       | 13    |
| tRS              | Read Command Set-Up Time     | 0   |          | 0    |         | 0    |         | 0   |        |       | 8     |
| tws              | Write Enable Set-Up Time     | -20 |          | -20  |         | -20  |         | -20 |        |       | 8     |
| <sup>t</sup> DHC | Data Input Hold Time         |     |          |      |         |      |         |     |        |       |       |
|                  | Referenced to CE             | 170 |          | 210  |         | 250  |         | 285 |        |       |       |
| tDHW             | Data Input Hold Time         |     |          |      |         |      |         |     |        |       |       |
|                  | Referenced to WE             | 70  |          | 90   |         | 105  |         | 125 |        |       |       |
| tww              | Write Enabled Pulse Width    | 60  |          | 75   |         | 90   |         | 105 |        |       |       |
| tMOD             | Modify Time                  | 0   | 10,000   | 0    | 10,000  | 0    | 10,000  | 0   | 10,000 |       | 9     |
| tWPL             | WE to CE Precharge Lead Time | 70  |          | 85   |         | 105  |         | 120 |        |       |       |
| tDS              | Data Input Set-Up Time       | 0   |          | 0    |         | 0    |         | 0   |        |       | 10    |
| twn              | Write Enable Hold Time       | 150 |          | 185  |         | 225  |         | 260 |        |       |       |
| tŢ               | Transition Time              | 5   | 50       | 5    | 50      | 5    | 50      | 5   | 50     |       |       |
| tRMW             | Read-Modify-Write Cycle Time | 385 |          | 475  |         | 570  |         | 660 |        |       | 16    |

# STANDBY CHARACTERISTICS

 $(T_A = 0^\circ C \text{ to } 70^\circ C)$ 

|                |                          | MK  | 4104-33 | MK4 | 104-34 | MK4 | 104-35 |       |  |
|----------------|--------------------------|-----|---------|-----|--------|-----|--------|-------|--|
| SYMBOL         | PARAMETER                | MIN | MAX     | MIN | MAX    | MIN | MAX    | UNITS |  |
| VPD            | VCC In Standby           | 3.0 |         | 3.0 |        | 3.0 |        | Volts |  |
| IPD            | Standby Current          |     | 3.3     |     | 3.3    |     | 3.3    | mA    |  |
| tF             | Power Supply Fall Time   | 100 |         | 100 |        | 100 |        | μsec  |  |
| t <sub>R</sub> | Power Supply Rise Time   | 100 |         | 100 |        | 100 |        | μsec  |  |
| tCE            | Chip Enable Pulse Width  | 200 |         | 250 |        | 300 |        | μsec  |  |
| tPPD           | Chip Enable Precharge To |     |         |     |        |     | _      |       |  |
|                | Power Down Time          | 100 |         | 125 |        | 150 |        | nsec  |  |
| VIH            | Min CE High "I" Level    | 2.2 |         | 2.2 |        | 2.2 |        | Volts |  |
| tRC            | Standby Recovery Time    | 500 |         | 500 |        | 500 |        | μsec  |  |

# POWER DOWN WAVEFORM



### DESCRIPTION (Cont'd)

to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirements of  $+5V \pm 10\%$  tolerance combined with TTL compatability on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's MK3880 (Z80). The early write mode (WE active prior to CE) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

The MK4104-3X series has the added capability of retaining data in a reduced power mode. V<sub>CC</sub> maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at  $8^{\circ}$ C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.





# OPERATION

# **READ CYCLE**

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ( $\overline{CE}$ ) clock. A read cycle is accomplished by holding the 'write enable' (WE) input at a high level (V<sub>1</sub>H) while clocking the CE input to a low level (V<sub>1</sub>L). At access time (t<sub>AC</sub>) valid data will appear at the output. The output is unlatched by a positive transition of CE and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when CE goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

### WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of CE or WE. If the negative transition of WE occurs prior to the leading edge of CE as in an "early" write cycle then the CE input serves as the strobe for data-in. If CE leading edge occurs prior to the leading edge of WE as in a read-modifywrite cycle then data-in is strobed by the WE input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, tDHW and tDHC. For a R/W or RMW cycle tDHC is automatically satisfied making tDHW the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of WE relative to CE. In any event both parameters must be satisfied.

In an early' write cycle the output will remain in an open or high impedance state. In a read-modify

write operation the output will go active through the modify and write period until  $\overrightarrow{CE}$  goes to precharge. If the cycle is such that  $\overrightarrow{WE}$  goes active after  $\overrightarrow{CE}$  but before valid data appears on the output (prior to tAC) then the output may not remain open. However, if data-in is valid on the leading edge of  $\overrightarrow{WE}$ , and  $\overrightarrow{WE}$  occurs prior to the positive transition of  $\overrightarrow{CE}$  by the minimum lead time tWPL, then valid data will be written into the selected cell. The Data in hold time parameters tDHW and tDHC must be satisfied.

### READ-MODIFY-WRITE CYCLE

The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between WE active (Iow) and the rising edge of  $\overline{CE}$  (twpL). Data out will remain valid until the rising edge of  $\overline{CE}$ . A minimum RMW cycle time can be approximated by the following equation (tRMW = RMW cycle time and tp =  $\overline{CE}$  precharge time).

 $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_{P} + 3t_{T}$ 

### POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V<sub>CC</sub> at +3V. However, prior to V<sub>CC</sub> going below V<sub>CC</sub> minimum ( $\leq$ 4.5V) CE must be taken high (V<sub>IH</sub> = 2.2V) and held for a minimum time period tPPD and maintained at V<sub>IH</sub> for the entire standby period. After power is returned to V<sub>CC</sub> min or above, CE must be held high for a minimum of t<sub>RC</sub> in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t<sub>CE</sub> min is not violated.

# **OPERATING POWER VS CYCLE TIME**



Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

- Curve 1 Clock on time (low level) is bottom scale minus 100 NSEC
- Curve 2 Clock off time (high level) is bottom scale minus 200 NSEC